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Original
Low power GaAs digital and analog functionalities for microwave signal conditioning in AESA systems / Ramella, C.; Longhi, P. E.; Nasri, A.; Pace, L.; Ciccognani, W.; Estebsari, M.; Pirola, M.; Limiti, E.. - (2020), pp. 1-3. (Intervento presentato al convegno 2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits, INMMiC 2020 tenutosi a Cardiff, UK (virtual event) nel 2020) [10.1109/INMMiC46721.2020.9160147].

Availability:
This version is available at: 11583/2854410 since: 2020-12-15T13:14:24Z

Publisher:
Institute of Electrical and Electronics Engineers Inc.

Published
DOI:10.1109/INMMiC46721.2020.9160147

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18 April 2024

Low Power GaAs Digital and Analog Functionalities for Microwave Signal Conditioning in AESA Systems

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***Abstract*—A MMIC demonstrator for RF phase and amplitude control with on board 18-bit serial to parallel conversion (Multi-Functional Chip) is presented. Thanks to an alternative digital building block topology, the DC power consumption of the digital serial to parallel converter is noteworthy: less than 43 mW (2 mW/bit). The main RF performances are 0° − 360° phase coverage and 0 dB − 31.5 dB attenuation setting, in the 7.6 GHz − 9.1 GHz operating bandwidth. The circuit, whose area is 6 mm², is realised in an industrial and commercially available GaAs technology. This component can be used in active electronically scanned arrays for beam steering.**

Keywords— Mixed Analog-Digital Integrated Circuits, Gallium Arsenide, Attenuators, Phase Shifters, Transceivers, Beam Steering.

I. Introduction

Active Electronic Scanned Arrays (AESAs) are becoming more compact and less power hungry thanks to advanced architectures enabled by the evolution of GaN and GaAs technologies. The trend is to realize the entire microwave transceiver with only two MMICs. The first MMIC, directly connected to the radiating element, is a GaN Single Chip Front End [1]. This circuit amplifies the transmit signal to the maximum power level and provides robust receiving functionality and signal duplexing between Tx and Rx paths. The second kind of circuit, topic of this paper, is a GaAs signal conditioning and routing MMIC. Usually this class of circuits features many operating states depending on the required phase shift, attenuation and selected path for the RF signal. Consequently, a huge number of control lines need to be routed inside the MMIC. Control signal routing issues at transceiver level can be greatly alleviated if a Serial Input - Parallel Output (SIPO) block is inserted on MMIC, therefore implementing either a Core-Chip or a Multi-Functional Chip (MFC when the circuits are only passive (no microwave amplifiers) [2]–[10].

II. Demonstrator Architecture and Technology

A. Architecture

The architecture selected for this functionality demonstrator is depicted in Fig. 1, and is usually referred to as MFC. The demonstrator circuit contains several key functionalities enabling future integration in a core-chip MMIC. In detail: a 18-bit SIPO block, described in section III-A and a 12-bit Phase and Amplitude Control (PAC) circuit described in section III-B. 6 bits are used for phase setting and another 6 bits for attenuation setting. Therefore 4096 (= 2^{12}) states are possible. The SIPO contains also an extra 6 bits targeting a possible future integration at core-chip level. The additional 6 bits are not connected to any microwave circuit in this demonstrator. Moreover, the PAC contains switching circuits (namely SPDTs) that will be also relevant at core-chip level for signal duplexing between Tx and Rx paths. Consequently, all the analog and digital functionalities developed and tested for this demonstrator represent the fundamental building blocks of a core chip MMIC. Finally, the operating frequency band for the PAC is 7.6 GHz – 9.1 GHz.

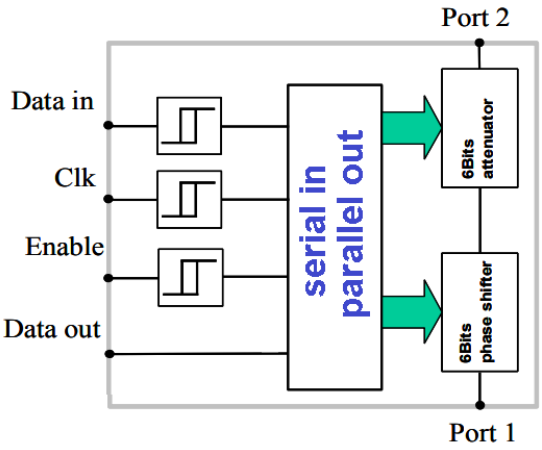

Fig. 1. Architecture of the MFC demonstrator MMIC

B. Technology

The selected technology for this demonstrator is necessarily in GaAs and featuring enhancement and depletion (E/D) transistors. GaAs is selected to reduce PAC circuit losses at microwave frequencies that would be much higher if a Silicon transistor were employed. E/D transistors can provide more design flexibility for the logic functions. The choice falls upon WIN's 0.25µm E/D-mode pHEMT technology platform, PD25-00, representing an interesting trade-off between technology maturity and RF performance. A quarter-micron optical gate, (E/D)-mode pseudomorphic high electron mobility transistor (pHEMT) is available. The E-mode FET shows high extrinsic trans-conductance (830

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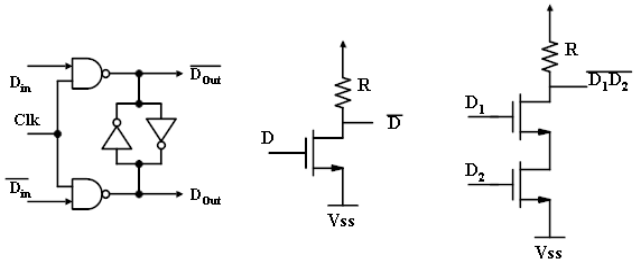
mS/mm) and high cut-off frequency (75 GHz). The D-mode FET exhibits a low R_{ON} of 1.3 ohm.mm, a low gate leakage current of 0.02 mA/mm and a switching time slightly above 100 ns at $V_G = -5$ V, which is suitable for RF switching and digital applications.

III. Functionality Design

A. 18-bit SIPO

The 18-bit SIPO system interfaces the several internal MMIC control signals to the external serial control/setting stream, thus relaxing routing complexity of the chip. This digital system is based on a synchronously clocked shift register together with a latch array unit to flush the parallelized bits to all the controlled RF cells [11], [12]. The realized digital interface is modular so that the number of parallelized bits could be increased or reduced according to the desired functionalities. Two external control signals acting as chip-select and data flush enable are required. External TTL/CMOS level compatibility is provided through on board level shifters, for data, clock and control signals. Level shifters are not only required for the voltage level compatibility but also to ensure fast internal level transition avoiding spurious multiple bit shifting that could be induced by the high speed (GHz) of the adopted active devices. The basic building block of the SIPO is the level-controlled latch shown in Fig. 2 (L). The NOT (C) and NAND (R) gate implementation with E-mode transistors is also reported. To further enforce spurious transition rejection and to ensure accurate clock transition synchronization, two basic latch cells, driven respectively by the "clock" and "inverted clock" signals, have been combined in a master-slave D-flip-flop cell to implement the transition-controlled shift register, as shown in Fig. 3 (top). On the other hand, to store and flush the bits to the output buffers interfacing the RF parts, a latch cell is sufficient and has been thus preferred to a master-slave cell in order to reduce current consumption. The selected process features both enhancement and depletion HEMT devices, thus normally-off (depleted) active pull-up could in principle be used. However, an approach based on resistive pull-up has been preferred, considering the higher yield of passive components together with the extremely low power dissipation design constraints, (max. 3.5 mW/bit).



(L) (C) (R)

Fig. 2. Logic-port-level implementation of the latch cell (L) and of the NOT (C) and NAND (R) gates.

Fig. 3 (bottom) reports the complete block diagram of the 18-bit SIPO module. An ad-hoc simplified and scalable HEMT model has been extracted from the PDK library in order to speed-up the design and simulation of the digital parts, requiring fast-convergence time-domain simulations. Using this model, a complete 18-bit loading sequence at the operating frequency of 25 MHz (asking for a time domain simulation up to 1 μs), of the complete SIPO (input level shifters, 18 bit shifter and output buffer) can be carried out in less than 1 min in ADS CAD, running on a personal computer.

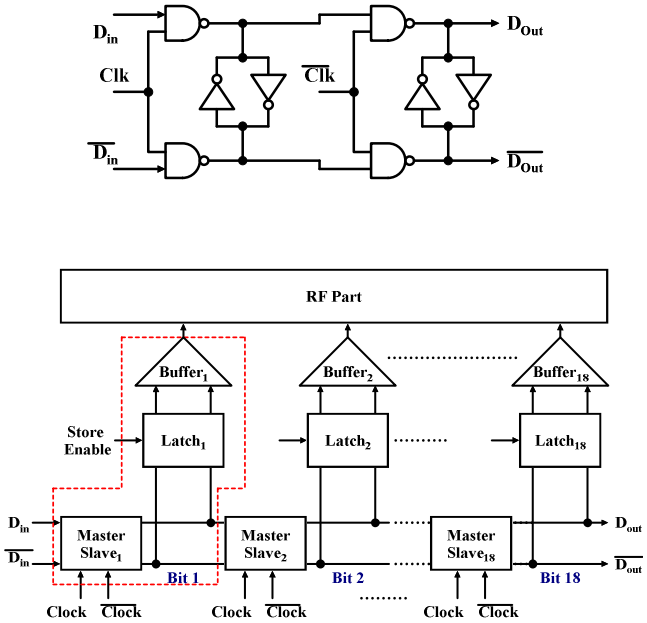


Fig. 3. Logic-port-level implementation of the master-slave shifter cell (top) and complete SIPO interface scheme (bottom)

CAD simulations show the correct SIPO behaviour, with well-shaped sharp-edge waveforms and margins for clock frequency well above the nominal 25 MHz, together with a remarkably low current consumption of only 12.5 mA, achieved thanks to the optimized pull-up resistors. These simulation results have been experimentally confirmed up to 50 MHz (limit of the experimental set-up). In fact, at the nominal 25 MHz clock frequency, the SIPO current consumption is around 13 mA, as expected, which corresponds, considering the -3.3 V feeding for the digital kernel, to roughly 43 mW power consumption. According to simulations, the input level shifters show roughly 2 mA current consumption. Thus a per bit current consumption of 0.6 mA/bit, corresponding to 2 mW/bit is achieved. These results are aligned, or even better than those proposed in [5].

B. 12-bit PAC circuit

The 12-bit PAC circuit is realized by cascading a 6-bit phase shifter (PS) and a 6-bit attenuator (ATT). The single cells are designed using standard techniques. The four higher phase shift values (180°, 90°, 45°, and 22.5°) are realized by switching from a high-pass (HP) filter to a low-pass (LP) filter. The two lower phase shift values (11.25° and 5.625°) are realized with a bridged-T "all-pass" topology. Similarly, the three higher attenuation values (16 dB, 8 dB, and 4 dB) are realized by switching from a reference path to an attenuated path realized in a Π topology. Finally, the three lower attenuation values (2 dB, 1 dB, and 0.5 dB) are realized with a switched bridged-T topology [13]. All these choices represent an acceptable trade-off between cell size/complexity and uniform performance over the operating bandwidth.

IV. MMIC Layout and Test

The demonstrator layout and corresponding sections microphotograph are reported in Fig. 4. Overall MMIC size is 3- mm x 2- mm. PS is on top side, ATT on bottom side while SIPO in the middle.

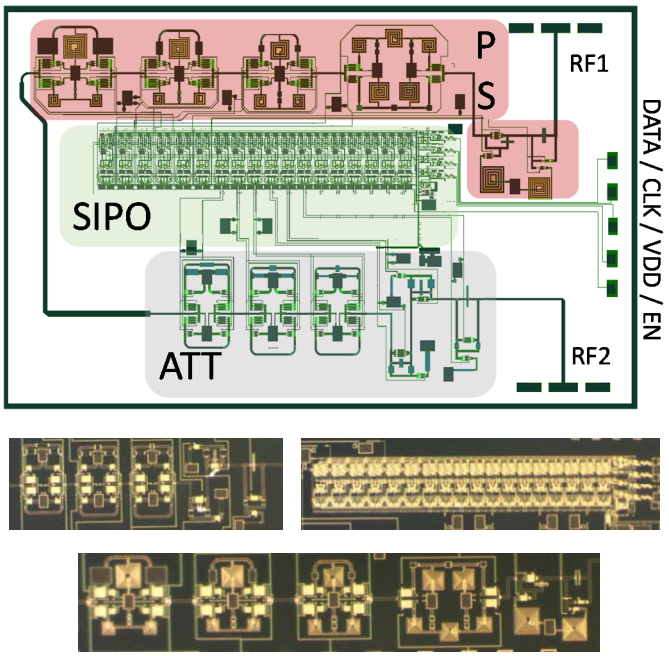


Fig. 4. MFC layout (3 mm x 2 mm) and micro-photo of the three functional blocks

Fig. 5 reports the measured phase shift of the 3 higher bits and the measured attenuation of the 3 lower ATT cells. The circuits were tested on wafer with a 25 MHz clock applied to the SIPO. When The PS is tested, the ATT is set in '00000' state and vice versa.

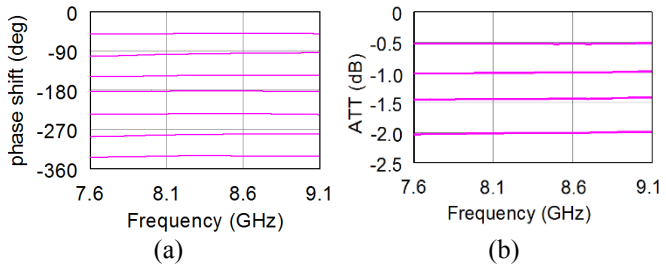


Fig. 5. Measured (a) phase shift and (b) attenuation.

The ATT behaviour is practically ideal while the PS showed some deviation probably due to limited accuracy of the models of the reactive elements employed for circuit simulations. Some minor tuning is thus required to correctly centre the performance of the phase shifter. PAC circuit measured insertion loss is 16 dB, while return loss at I/O port is typically 17 dB, being slightly better at attenuator port side. Expected IP1dB at PS input is +10 dBm.

V. Conclusions

In this paper, we present the design and initial tests of a GaAs 12-bit MFC operating at 7.6 GHz – 9.1 GHz. The key feature of this demonstrator is the ultra-low power consumption of the 18-bit SIPO system, which is only 45 mW (2.5 mW/bit). This feature is obtained through an approach based on resistive pull. The main RF performances are 0° - 360° phase coverage, 0 dB - 31.5 dB attenuation setting, and 16 dB insertion loss.

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