Three-phase Inverter for Formula SAE Electric with Online Junction Temperature Estimation of all SiC MOSFETs

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***Abstract*— The ability to monitor the junction temperature of power devices during the operation of a power converter will be the key enabler towards combined higher performance and higher reliability of power electronics. Starting from the well-known dependency of the R_{ON} with the junction temperature of SiC power MOSFETs, an innovative solution is proposed to obtain the high-dynamic estimation of the junction temperature of all the power devices. This work focuses on the commissioning stage of a three-phase, 2-level voltage source inverter, enabling the real-time temperature feedback of all six power devices of the bridge during operation. A selection of experimental results is reported.**

Keywords—SiC, junction temperature estimation, ON resistance, formula SAE electric, 3-phase inverter, TSEP.

I. INTRODUCTION

SiC power MOSFETs offer a series of advantages compared to their silicon counterpart. They allow lower switching and conduction losses, improved thermal stability and conductivity, higher operating temperatures and higher operating voltages [1]-[6]. All such advantages enable the realization of power converters with increased efficiency and power density. Despite these benefits, almost a decade has passed since the introduction of the first 1200 V SiC power MOSFET and there are still obstacles in terms of market penetration. This is mainly due to the high cost of such devices and to many unsolved challenges related to high dv/dt, EMI and low reliability.

Junction temperature plays a key role in the life and reliability of the power semiconductors and must always be maintained under appropriate safety limits. Providing accurate thermal management can be even more challenging for SiC devices due to low thermal inertia combined with high power density. Most of the time, the actual junction temperature during operation is unknown or estimated very roughly, thus forcing the power converter designer to keep huge safety margins while sizing the power components. Over time different techniques have been investigated to measure or estimate the junction temperature of power devices. Direct measurement technique like the use of a thermal camera [7]-[8] are not viable for industrial applications. Alternative methods including the use of thermistors in direct contact with the die have proven to be critical due to insulations problems and measurement delay [9]. Up to date the only viable solution is the use of electro-thermal models joint with the temperature measurement of the Direct Bonded Copper (DBC) substrate or of the heatsink through a thermistor [10] -[12]. The models used for such estimation are typically rough, resulting in significant temperature estimation errors. Therefore, the need for huge safety margins is not completely avoided. In the last years TSEPs (Thermo-Sensitive Electrical Parameters) based techniques have gained importance and they are now widely adopted as an indirect indicator of the junction temperature. Depending on the semiconductor and the test conditions, various TSEP techniques have been developed [13]-[16]. However, most of TSEP based methods cannot be used in real case scenarios and their use is currently limited to laboratory environment, relying on dedicated equipment and controlled test conditions. Among the other TSEPs, the well know relationship between the conduction resistance and the junction temperature of a semiconductor is typically used for in laboratory for testing purposes, i.e. for datasheet compilation.

This work introduces innovative solutions to use this technique in a real case scenario directly on the converter, without dedicated equipment. The goal of this work is to present a methodology and a power converter hardware configuration capable of obtaining a precise and reliable estimation of the MOSFETs junction temperature in a three-phase voltage source inverter. A very basic proof of the concept test rig was previously described in [16] and [17]. Following the good results obtained from the first POC converter, the new three phase inverter prototype has been realized, referring to the final application of the racing car of the Squadra Corse of Politecnico di Torino, competing in Formula SAE Electric students' championship.

II. PROPOSED SETUP

The overview of the prototype power converter is shown in Fig. 1. The schematic of the power section of the converter is reported in Fig. 2, where the sampled quantities are indicated in red. **Respect to a standard converter, the additional measurement of the conduction voltage (V_{ON}) of the six switches is introduced, both for positive and negative current values.** The converter uses three BSM180D12P3C007 SiC power modules by ROHM Semiconductor, having breakdown voltage of 1.2 kV and rated RMS current of 180 A (@ case temperature of 60°C). Each half bridge module contains two SiC MOSFETs and two antiparallel diodes. This power module has been chosen because of his favourable pinout permitting to realize a high-power density inverter. Nevertheless, the proposed technique can also be implemented for discrete components and virtually for any kind power module regardless the geometry. The

liquid cooled heatsink has been preliminarily replaced with an aluminium block visible at the bottom of Fig. 1. Its temperature is monitored using two PTC thermistors. The hardware control system is based on a hybrid architecture using an industrial microcontroller STM32H7 and a Spartan 6 FPGA, permitting great flexibility of development of the control algorithm and the modulation strategy. Furthermore, the converter integrates all the additional peripherals needed by the race car, such as CAN interface, data logging uSD, two encoder interfaces, debugging interfaces and analog measurement interfaces. The Squadra Corse race car houses four inverters, one per motorized wheel. Fig. 3 shows the previous version of the race car, while the new version for the season 2020 is currently under design. The working DC bus voltage is 600 V provided directly from the on-board car battery and the switching frequency is 20 kHz.

TABLE I - RATINGS OF THE PROTOTYPAL INVERTER

Peak output current	240 A
Maximum DC Voltage	700 V
Maximum Switching Frequency	200 kHz
Nominal Switching Frequency	20 kHz
DC-link film capacitors	5x 20 µF
DC-link ceramic capacitors (SMD)	3x 220 nF
Microcontroller	STM32H743ZI
FPGA	Spartan6-XC6SLX75
N° A/D channels of the MCU	3
N° 14-bit external A/D converters	10
CAN	CAN bus 2.0
Encoder interface 1	Absolute (EnDat 2.2)
Encoder interface 2	Incremental
Power Module, type #1 (from datasheet)	
Rated current (Tcase=60°C)	180 A
Breakdown voltage	1200 V
R_{ON} @ 25°C, 20A	10 mΩ
Stray Inductance	25 nH
Max Junction Temperature	175°C

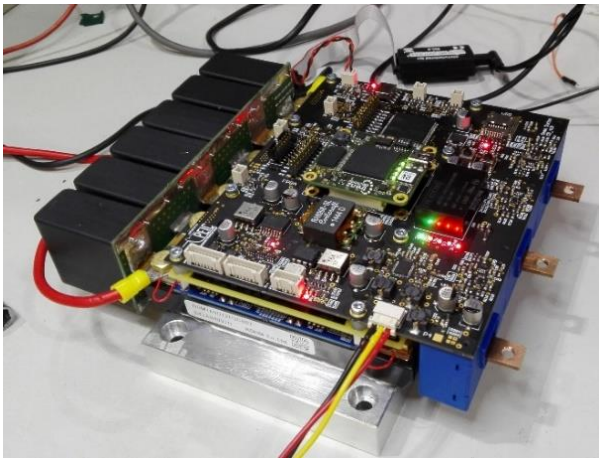

Fig. 1. Power converter overview.

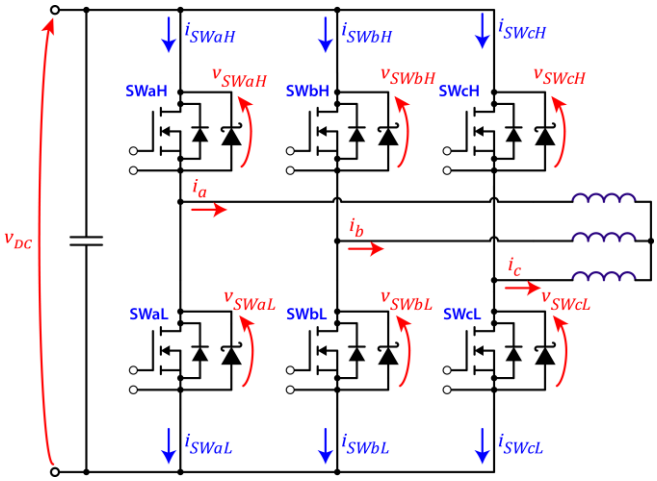

Fig. 2. Inverter schematic, red quantities are measured at each PWM period.

Fig. 3. Squadra Corse race car prototype, year 2019.

III. V_{ON} MEASUREMENT SYSTEM

Special care must be given to the design of the measurement system used for acquiring the conduction voltage of the MOSFET. The measurement system must acquire the voltage drop of the MOSFET working in PWM mode also when the conduction time is short, i.e. when the duty-cycle of one converter phase approaches its upper or lower limits. Fig. 5 shows the schematic of the analog conditioning circuitry used for measuring voltage between drain and source of the MOSFET. A high bandwidth operational amplifier in differential configuration is used. When the MOSFET is OFF its v_{ds} equals the DC link voltage, 600 V in this case. In turn, the diode D6 protects the measurement circuitry from the DC-link voltage during OFF state. During the conduction state of the MOSFET, v_{ds} drops to few volts and the diode D6 is polarized at constant current provided by Q1. The diode D4 in series to D6 conducts the same current. The voltage drop of D4 compensates the voltage drop of D6. Any small difference in the forward voltage of the two diodes does not affect the temperature estimation if it is constant over time. In fact, the two diodes can be considered at the same temperature thanks to their proximity, so that the variation of the forward voltage drop due to the temperature is automatically compensated. The MOSFET Q2 further improves the bandwidth of the measurement system. When the power MOSFET is OFF, the respective Q2 avoids the saturation of the operational amplifier by shorting its input. During the tests presented in this paper Q2 was left open,

however it will be used in the future to increase the bandwidth of the acquisition system and minimize acquisition latency.

SPICE simulations have been performed to test the performance of the measurement system. The results of the small signal AC analysis are shown in Fig. 6, the obtained bandwidth is 40 MHz circa. In Fig. 7 v_{DS} is step-varied between 600 V and -3.5V (top of the figure) to analyse the response of the analog conditioning system (bottom subplot). The settling time is around 0.07 µs, thus enabling the v_{ON} sampling also when the conduction time is short, in the order of the microsecond.

The output of the analog conditioning system is connected to a dedicated 14-bit ADC that transmits the data to the FPGA using a SPI communication. The overview of the driver board (one for each inverter leg) embedding the v_{DS} measurement system is shown in Fig. 4. Each driver board hosts two such dedicated ADCs.

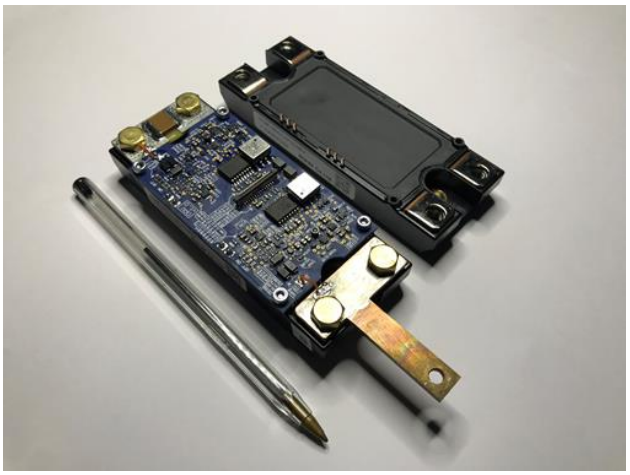

Fig. 4. Custom design driver board with v_{DS} measurment system.

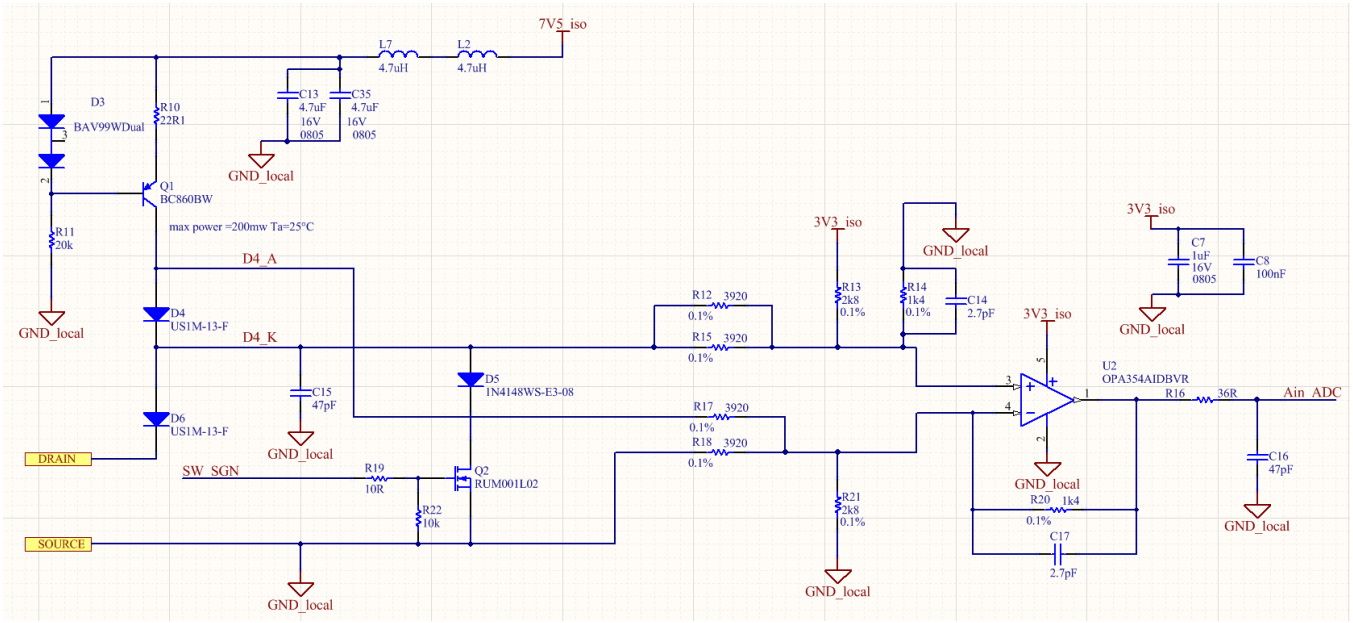

Fig. 5. Schematic of the analog conditionin system for measuring the conduction voltage of the MOSFET.

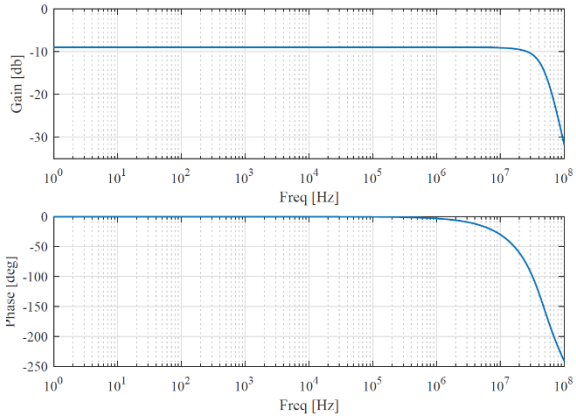

Fig. 6. Bode diagram of the $v_{Ain\ ADC}/v_{DS}$ transfer function.

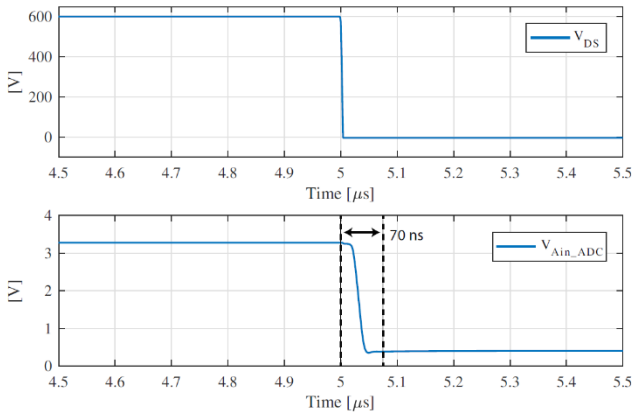

Fig. 7. v_{DS} step changed from 600 V to -3.5 V.

IV. Commissioning Test

The junction temperature estimate functional block description is shown in Fig. 8, where SWx stands for any of the switches, with x = aH, aL, bH, bL, cH, cL. The identification of the temperature look-up tables $\theta_{j,est,SWx}\left(R_{ON,SWx}, i_{SWx}\right)$ is addressed in the following. The letter *a,b* or *c* indicate the inverter phase (i.e. power module), whereas *H* and *L* stand for high side and low side switches, respectively.

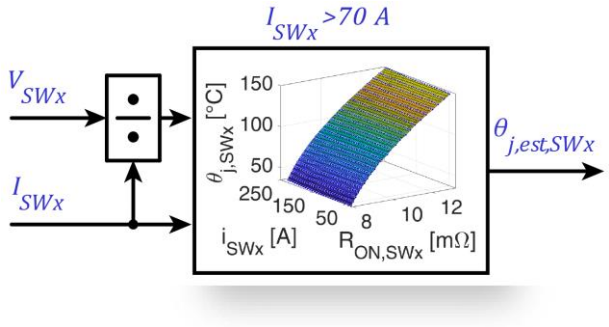

Fig. 8. Functional block of the temperature estimator.

A. *Commissioning test proceure*

The commissioning test procedure determines the temperature look-up tables of the six MOSFETs later used for temperature estimate according to Fig. 8.

The commissioning is performed directly on the converter without additional laboratory equipment, with the exception of an external heat source (hot plate underneath the aluminium base of Fig. 1). For simplicity, the aluminium block will be called heatsink in the following. As said, two thermistors measure the heatsink temperature. The key assumption is that with current pulses of appropriate time length (i.e. very short and sparse), the junction temperature and the heatsink temperature do not vary from each other.

The converter supplies a star-connected 3-phase inductor, phase inductance is 33 µH. The commissioning steps are:

1. The heatsink is heated to 150 °C, according to the two said thermistors. The heater is turned-OFF and the heatsink cools naturally (i.e. slowly).
2. At this temperature, short current pulses from 10 A to 240 A with step of 10 A circa are commanded for each of the six inverter axes as shown in Fig. 9 and Fig. 11. The v_{ON} of the switches is measured and logged. Six current sequences are repeated along each direction in the phase space as shown in Fig. 11. **This permits to map all six switches within 240 A pk, for both positive and negative currents at this temperature.** At the end of this sequence the converter remains idle, waiting for the temperature to diminish.
3. Every time the temperature drops by 5 °C a new current sequence is commanded as shown in Fig. 10.
4. The identification stops when the hot plate reaches 35°C.

The short duration of the current pulses (100 µs) combined to a time separation of 200 ms from pulse to pulse ensures that the junction temperature of the MOSFETs equals the heatsink temperature measured by the PTC thermistors. The 6-switches identification sequence takes 30 seconds circa (200 ms times 24 currents times 6 directions) and the commissioning test takes 90 minutes altogether, dictated by the slow natural cooling of the heatsink. The duration of the commissioning test could be substantially reduced with active cooling of the heatsink from one temperature level to the other. The collected data from the commissioning test are shown in Fig. 10.

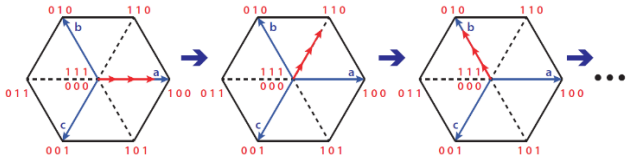

Fig. 9. Current pulses of growing aplitude on each of the six inverter axis.

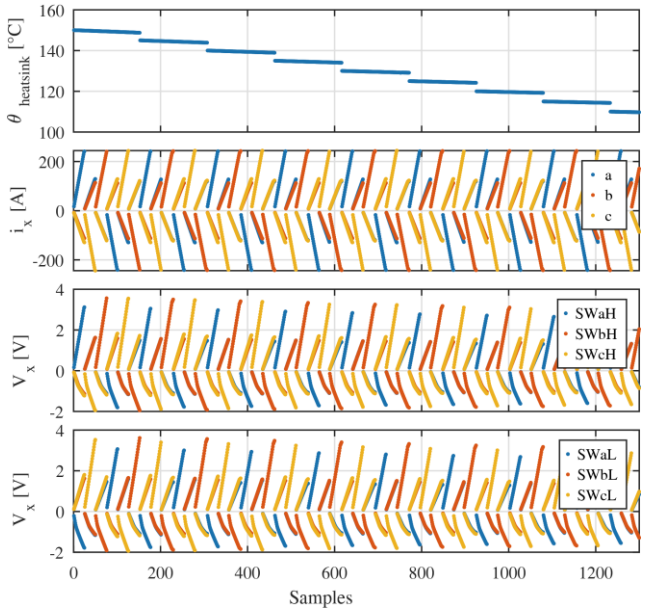

Fig. 10. Data sampled during the commission test. Wait time between temperature levels is not represented.

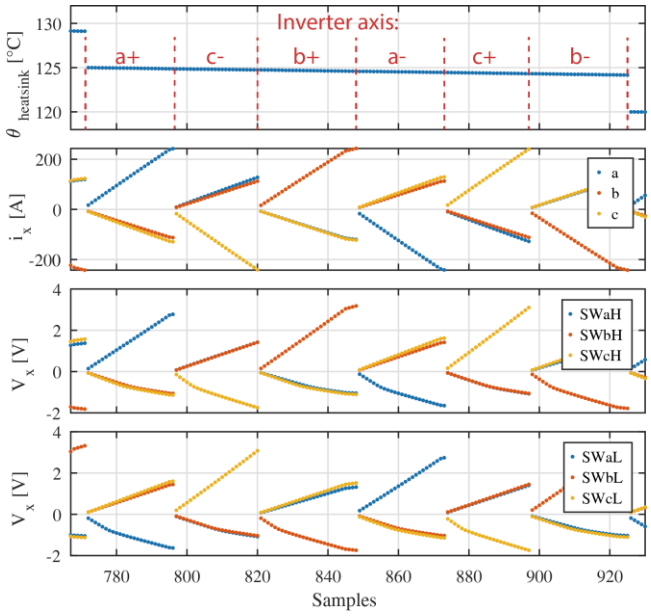

Fig. 11. Detail of the data sampled during the commission test higlining the the six inverter axes. Wait time between temperature levels is not represented.

B. *Description on one current pulse*

For the sake of example, Fig. 13 shows the 240 A current pulse along the a (positive) axis. The bottom of the figure shows the 20 kHZ PWM carrier and the reference duty cycles of phases a,b,c of the converter. The top of the figure shows the state of the three inverter legs. The state of the inverter leg is "1" when the high side switch is ON and "0" when the low side switch in ON. E.g. "100" indicates that phase "a" is connected to the positive terminal of the DC-link and phases "b" and "c" are connected to the negative terminal. In Fig. 13 the switches states alternate between the active state "100" and the two zero states "000" and "111" represented in Fig. 12 to impose current along the direction *a* positive. Fig. 13 shows that the total current pulse duration is two PWM periods, or 100 µs. During the first PWM period the current rises to the target value of 240 A. Conduction voltages, currents and temperatures are sampled during the second PWM period in correspondence of the positive and negative updates of the triangle, labelled respectively as SP1 and SP2. At the sampling time SP1 the leg state is "111", so according to Fig. 12 the current flowing in SWaH is i_a while the currents flowing in SWbH and SWcH are $-i_a/2$. At the sampling time SP2 the current flowing is SWaL is $-i_a$ while the currents flowing in SWbL and SWcL are $i_a/2$. In turn, imposing current pulses along the a+ axis permits to map the MOSFET SWaH for positive currents and the MOSFET SWaL for negative currents. If the current pulse injection is repeated for all the six axes, all the switches are mapped for positive and negative values of current. Another aspect to take into consideration is the limited bandwidth of the current sensor. The inverter uses three industrial hall sensors LEM LA200P with an attenuation of -1 db at 100 kHz. In turn, care must be taken when high di/dt occurs. E.g. in Fig. 13 anticipating SP2 on the previous triangle positive vertex would have resulted in inaccuracy in the current measurement.

One of the main assumptions is that during the commissioning test the junction temperature of the MOSFETs equals the temperature measured by the thermistors placed on the aluminum plate. Thanks to the slow natural cooling of the aluminium the system can be considered isothermal. Furthermore, the short duration of the current pulses ensures that during the test the temperatures of the MOSFETs do not vary significantly respect to the temperature of the aluminum plate. It is possible to compute in the first approximation the temperature rise due to one current pulse in the worst case condition. The worst case condition for SWaH is for a positive current of 240 A and a junction temperature of 150 °C. It can be computed that the temperature rise in the worst case condition is below 2°C. To further reduce the commutation losses the commissioning test has been performed at a reduced voltage of 340 V.

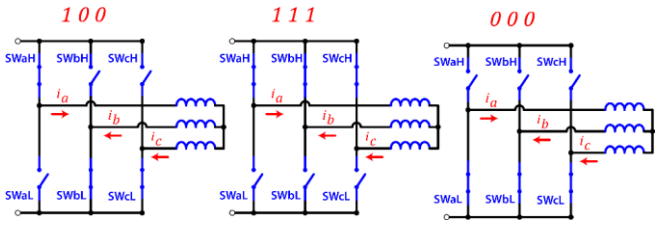

Fig. 12. Inverter switches configurations and phase currents during the commissionig alog a+ axis.

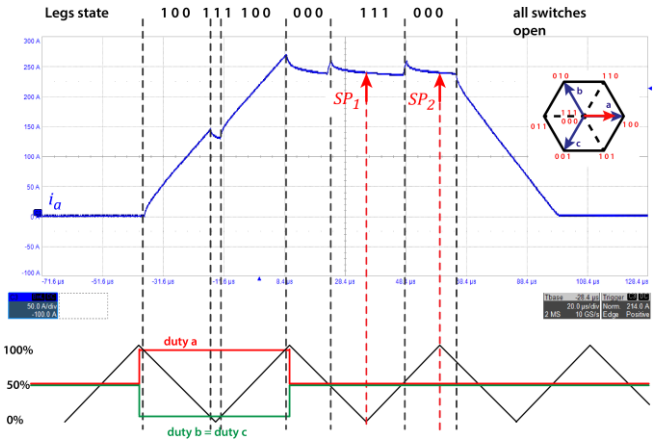

Fig. 13. Current pulse of 240 A for a+ axis during the commissioning test. Phase current i_a (50 A/div), t=20 us/div.

C. *Commissioning test results*

The data obtained from the commissioning test can be organized in the form $\theta_{j,SWx}\ (V_{SWx},\ i_{SWx})$ or equivalently in the form $\theta_{j,SWx}\ (R_{ON,SWx},\ i_{SWx})$. The LUT of the switch SWaH in the form $\theta_{j,SWaH}\ (R_{ON,SWaH},\ i_{SWaH})$ is shown in Fig. 14 for $i_{SWaH} > 30\ A$ and in Fig. 15 for $i_{SWaH} < -30\ A$. The data obtained at low currents, in this case less than 30 A, are not reported due to the difficulty of accurately measuring the low condition voltage of the MOSFET. The LUT obtained for positive currents is directly used for junction temperature estimation, whereas the negative current LUT is pointless for temperature estimation, since it is not possible to compute the current sharing between the MOSFET and the antiparallel diode. Further investigations are ongoing on how to decouple the diode and MOSFET currents. The data collected may also be analysed using a 2D representation. The results obtained for positive drain current are reported in Fig. 16 and Fig. 17. Fig. 16 shows the R_{ON} as a function of the junction temperature for different values of drain currents. The R_{ON} increases by 62% when the junction temperature rises from 30°C to 150°C at a current of 240 A. Fig. 17 shows the R_{ON} as a function of the drain current for different values of junction temperature. The R_{ON} increases only by 3% when the current varies from 30 to 240 A at a junction temperature of 150°C. To obtain a good temperature estimate both dependencies must be taken into account. The obtained results for negative values of drain current are reported in Fig. 18 and Fig. 19. These plots are less significative, however the plot of Fig. 19 clearly shows that the current sharing between the MOSFET and the antiparallel diode is strongly affected by their junction temperatures. As the current becomes more negative the diode begins to conduct part of the current of the MOSFET, this causes an "apparent" reduction of the conduction resistance.

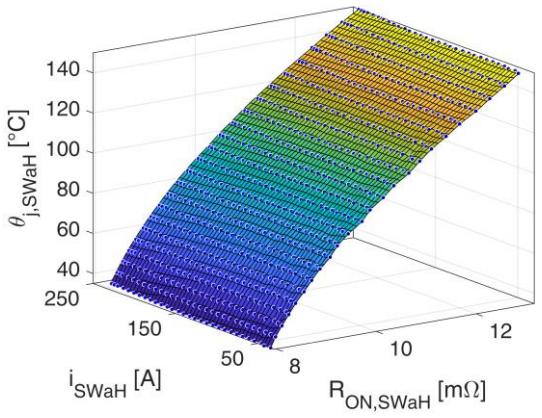

Fig. 14. Look-up table obtained from the current pulse test for the MOSFET SWaH for i_{SWaH} > 30 A.

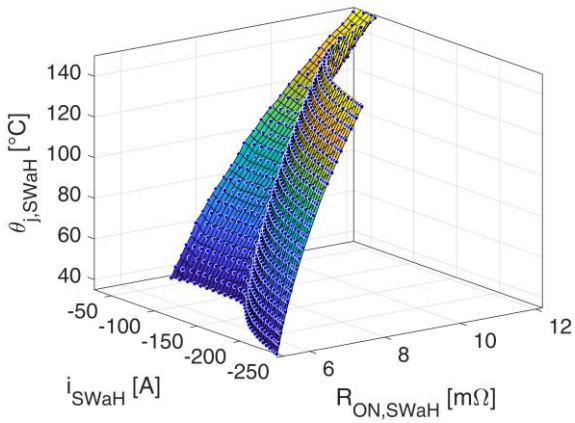

Fig. 15. Look-up table obtained from the current pulse test for the MOSFET SWaH for i_{SWaH} < 30 A.

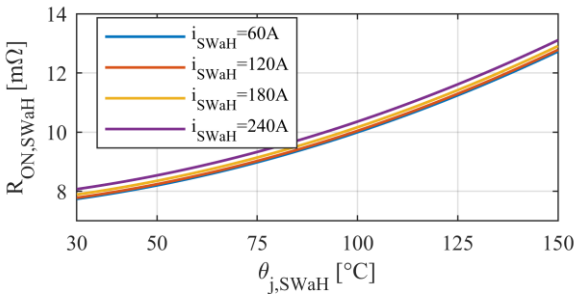

Fig. 16. R_{ON} as a function of the juntion temperature for positive drain currents.

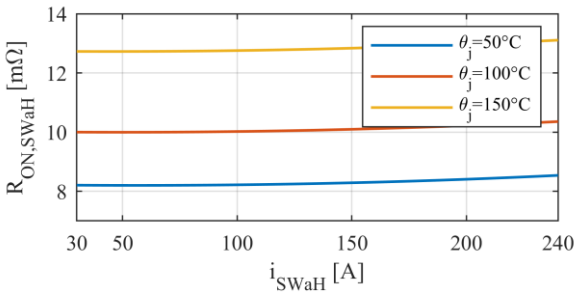

Fig. 17. R_{ON} as a function of the drain current at different juntion temperatures.

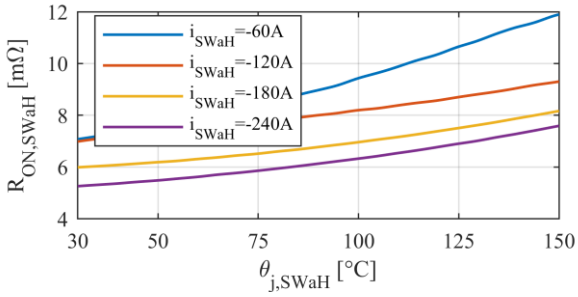

Fig. 18. R_{ON} as a function of the juntion temperature for negative drain currents.

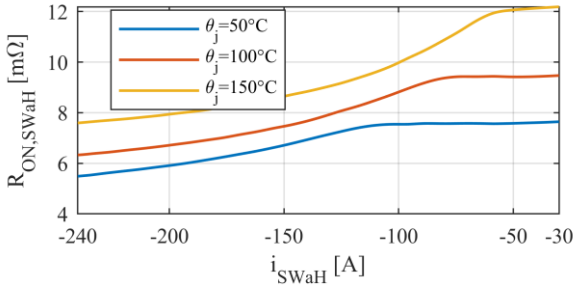

Fig. 19. R_{ON} as a function of the drain current at different juntion temperatures.

V. On line juntion temperature estimation

The temperature of the six switches is real-time estimated for i_{SWx} >70 A using the functional block diagram of Fig. 8. An example of experimental results is provided in Fig. 20 where the inverter imposes 210 A pk at 0.5 Hz to the three phase load consisting of the already introduced 33 µH inductor. The bottom plot shows the estimated junction temperature for the six MOSFETs and the measured heatsink temperature (dashed black line). During the test the temperature of the heatsink remains circa constant at 50°C while the junction temperature of the MOSFETs show large thermal swings.

Fig. 21 reports a similar test, with 210 A pk at 10 Hz. The comparison between Fig. 20 and Fig. 21 shows that the temperature swing and peak value expectedly lower at higher fundamental frequency.

A. *Adaptive current limit*

Consequently, the temperature feedback can avoid the usual risk of failure around dc output conditions, by direct limitation of the output current or, conversely, to extend the output current limit of the converter at higher fundamental frequency. Fig. 20 show that the estimated temperatures for the MOSFETs SWaH and SWaL are sensibly lower respect to other temperatures. This is due to the parametric dispersion of the components, in fact the characterization results confirmed that the MOSFETs SWaH and SWaL have a considerably lower conduction resistance.

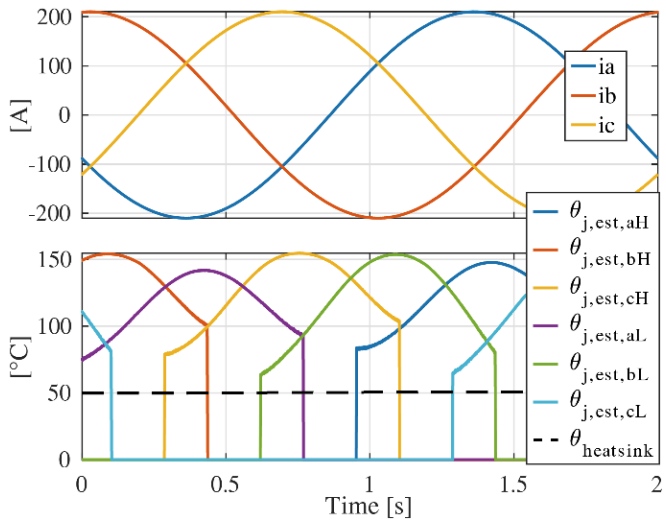

Fig. 20. Top: Synusoidal output phase current at **0.5 Hz**. Bottom: $\theta_{j,est}$ of the six MOSFETs and measured heatsink temperature.

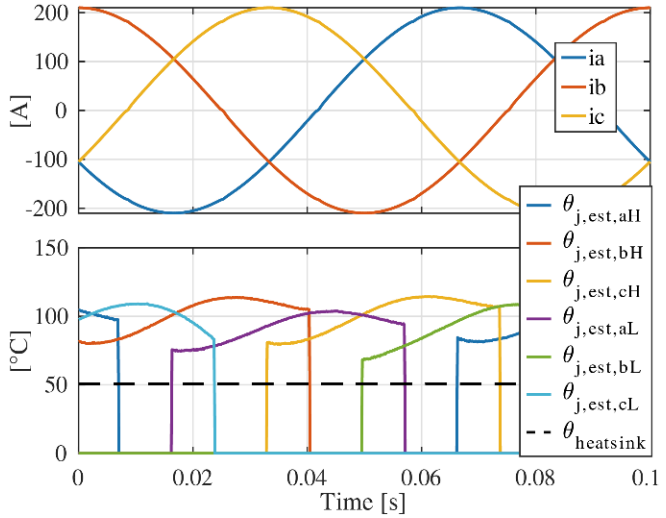

Fig. 21. Synusoidal output phase current at **10 Hz**. Bottom: $\theta_{j,est}$ of the six MOSFETs and measured heatsink temperature.

VI. Conclusions

A. Strengts and limitations

The main strengths of the proposed methodology are:

- Temperature detection does not affect the operation of the converter.
- The identification is performed directly on the converter without additional equipment. The same measurement system used to build the temperature map of the semiconductor is later used to for temperature estimate, coherently. Any systematic offset and nonlinearity of the v_{ON} measurement system not varying over time do not introduce any error in the temperature estimation.
- The additional circuitry for the v_{ON} measurement is standard and low cost, and not prone to EMC issues. In the future, the v_{ON} measurement circuitry might be embedded in the gate driver chip. In fact, most of the gate driver commercially available already integrate desaturation protection that is based on v_{ON} inspection.
- The v_{ON} measurement system does not require any tuning, if it is stable over time.
- No complex computation is involved.
- The temperature estimation can be implemented using an industrial MCU. The converter embeds an FPGA only for development purposes, although it is not necessary for the commissioning and for the online temperature estimation. The computational time required to estimate θ_j is modest, and it is not necessary to estimate the junction temperature at every PWM period because of the relatively large thermal constant of the die.

To date, the limitations of the methods are:

- The junction temperature of the MOSFET cannot be estimated for negative values of i_{DS}, due to the presence antiparallel diodes that conduct part of the negative current during identification. However, this case tends not to be thermally critical, as the losses are shared between the diodes and the MOSFET during the negative half wave. Furthermore, when $i_{DS} < 0$ the commutation losses in the device are negligible compared to the case of $i_{DS} > 0$. If no antiparallel diode is present the temperature of the MOSFET can be estimated also for negative values of i_{DS} thanks to the symmetrical behaviour of the MOSFET. The same power module is also available without the antiparallel diode and it will be tested in the future.
- If the current in the device is too small (less than 70 A, absolute value), $\theta_{j,est}$ tends to be less accurate due to poor noise to signal ratio at low value of v_{ON}. However, also this case is not thermally critical.

B. Aging

It is well known from the literature that with the aging of the component the component R_{ON} increases [18] and [19]. The temperature estimator tends to overestimate the temperature of the component. However, in SIC devices the increment of the R_{ON} before failure is modest, thus the temperature over estimation is modest as shown in [20] where the same technique has been used on a power module subject to accelerated aging. If the temperature feedback is used to limit the maximum allowable current in the converter, this will lead to over limit the current and the converter will underperform. The user can run a new commissioning test or accept the derating that according to [20] is modest.

C. Squadra Corse race car

The Squadra Corse race car will be the testing platform to validate the proposed solution at a higher TRL (Technology Readiness Level). The main benefits of the proposed solution to the final application are the augmented reliability (no failure of power modules is expected) and the ability to adapt (i.e. possibly increase) the power converter maximum current limit according to real temperature readings, virtually without any risk of failure. This solution is well suited for such application where short overloads are expected and where the cooling system is down do the bare bones so to save space and weight.

D. Prospect Application

The proposed methodology can be implemented in all types of switching converters with limited extra complication and cost. The applications that would most benefit in using the proposed methodology are:

- Applications with frequent transient overload like automotive and servo-drives.
- Safety critical applications where failure or malfunction my result in damage to people.
- Applications where the downtime is costly such as oil and gas.
- High power applications where the safety margins on the component size are costly.
- High power density applications where the cooling system and components must be fully exploited.
- Cost critical applications where the cost of the power electronics represents a non-negligible fraction of the system cost.

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