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Investigation on the Stabilizing Effect of Titanium in HfO_2-Based Resistive Switching Devices With Tungsten Electrode

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Resistive switching (RS) devices, also referred to as resistive random access memories (ReRAMs), rely on a working principle based on the change of electrical resistance following proper external electrical stimuli. Since the demonstration of the first resistive memory based on a binary transition metal oxide (TMO) enclosed in a metal–insulator–metal (MIM) structure, this class of devices has been considered a key player for simple and low-cost memories. However, successful large-scale integration with standard complementary metal–oxide–semiconductor (CMOS) technologies still needs systematic investigations. In this work, we examine the beneficial effect titanium has when employed as a buffer layer between CMOS-compatible materials like hafnium dioxide and tungsten. Hindering the tungsten oxidation, Ti provides RS stabilization and allows getting faster responses from the devices. Through an extensive comparative study, the effect of both thickness and composition of Ti-based buffer layers is investigated. The reported results show how titanium can be effectively employed to stabilize and tailor the RS behavior of the devices, and they may open the way to the definition of new design rules for ReRAM–CMOS integration. Moreover, the gradual switching and the response speed tunability observed employing titanium might also extend the domain of interest of these results to brain-inspired computing applications.

Keywords: resistive switching, ReRAM, tungsten, titanium, buffer layer

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INTRODUCTION

Devices with tunable electrical resistance find application in information and communication technologies (ICTs) since the end of the 19th century, when the so-called coherer was employed as receiver in Marconi's wireless telegraph (Marconi, 1899) thanks to the possibility of changing, and retaining, its electrical conductivity upon external stimuli. Some decades later, in the 1960s, attention started focusing on oxide materials with similar properties (Gibbons and Beadle, 1964; Lamb and Rundle, 1967), opening the way for the wide class of devices nowadays identified as resistive memories. Also referred to as resistive random access memories (ReRAMs) or oxide RAMs (OxRAMs), these resistive switching (RS) devices typically rely on a simple metal–insulator–metal (MIM) structure composed of two metallic electrodes enclosing an insulating oxide layer (Waser and Aono, 2007), but similar stacks without metals have been demonstrated too (Yen et al., 2019). As for the coherer, their working principle is based on the change of electrical resistance

as a response to proper external electrical stimuli. The condition of low conductivity is defined as high-resistance state (HRS), and it can be turned into a more conductive low-resistance state (LRS) through the so-called SET process. The opposite transition, resulting in a resistance increase, namely the transition from LRS to HRS, is instead named RESET. When both the state transitions occur with the same polarity, RS devices are classified as unipolar, while they are defined as bipolar if SET and RESET require opposite polarities (Ielmini and Waser, 2016). In most cases, before exhibiting successful switching between these states, RS devices require the so-called forming process, which gives the first transition of the pristine device to a highly conductive state. Since the demonstration of the first resistive memory based on a binary transition metal oxide (TMO) (Baek et al., 2005), this class of devices has been considered a key player for simple and low-cost memories able to compete with the market-leading technologies (Wong et al., 2012; Meena et al., 2014). Such a perspective translated into an unceasing driving force for research efforts to continuously improve features like low power consumption, high density, fast switching, high endurance, long retention, and compatibility with complementary metal–oxide–semiconductor (CMOS) technologies (Cai et al., 2019; Tang et al., 2019; Xia and Yang, 2019; Wang et al., 2020). In seeking to fulfill these requirements, many studies have been carried out on subjects ranging from the physical behavior to the hardware implementation. As a result, it is now well-established that both interface-type (Celano et al., 2017; Govoreanu et al., 2017) and filamentary-type (Joshua Yang et al., 2009; Lee et al., 2009; Celano et al., 2014) resistive switching exist, and it is widely accepted that the formation of a conductive filament involves ion motion within the insulating layer of the MIM structure (Valov, 2014; Sun et al., 2019; Wang et al., 2020). In-memory computing systems have been shown (Zidan et al., 2018) and brain-inspired functionalities have been demonstrated (Xia and Yang, 2019). Despite these outstanding findings, successful large-scale integration with standard CMOS technologies is only just at the beginning and still needs further systematic investigations able to provide new design rules. In this context, many materials have been studied for both the insulating layer and the electrodes. Silver and copper have been employed in the so-called electrochemical metallization (ECM) memory cells, where they work as electrochemically active electrodes to release cations for metallic filament formation upon electromigration through the "I" layer (Valov et al., 2011). Platinum and titanium nitride have been shown to be suitable for inert electrodes (Tappertzhofen et al., 2014), while oxidizing metals like tungsten, titanium, hafnium, and tantalum have been studied as electrodes in valence change memory (VCM) devices (Chen et al., 2013; Lin et al., 2013; Shahrabi et al., 2019) and many oxides have been tested as an insulating layer. Among them, resounding success has been achieved by HfO_2 (Chen et al., 2009), Ta_2O_5 (Kim et al., 2016), TaO_x (Yang et al., 2010), TiO_2 (Chen et al., 2017), and ZnO (Conti et al., 2019). Moreover, it has been pointed out by different works that the whole material stack of each ReRAM cell, and not only the single layers, is the ultimate responsible for the device performances (Gilmer et al., 2011; Walczyk et al., 2012; Chen et al., 2013; Kim et al., 2016; Rahaman et al., 2017; Singh et al., 2018; Ambrosi et al., 2019; Kindsmüller et al., 2019; Lee et al., 2019; Shahrabi et al., 2019). Particularly, in the framework of VCM devices, a key role is played by the interaction between the metal oxide in the "I" layer and the oxidizing electrode. Such devices, indeed, rely on the formation and rupture of a conductive filament resulting from local valence changes of the metal within the oxide, which, in turn, results from the migration of O^{2-} ions and the subsequent formation of oxygen vacancies ($V_{\ddot{O}}$) under the action of an applied voltage (Celano et al., 2016). The motion of these species strongly depends on the oxygen exchange between the oxide film and the oxidizing electrode and can be described by the reaction:

$$M\,(\text{bulk}) + \text{TMO} \rightleftharpoons MO_x + \text{TMO}_{1-x} + x \cdot V_{\ddot{O}} + 2x{\cdot}e^{-} \quad (1)$$

where M is the oxidizing electrode and TMO is the oxide in the "I" layer.

In view of the upcoming CMOS integration, tungsten turns out to be a feasible choice for the oxidizing electrode due to its already established employment for vertical interconnect accesses (VIAs). However, when used in direct contact with an oxide, its multiple and metastable oxide forms introduce relevant instability in the memory cell performances, so that the insertion of a buffer layer becomes necessary (Shahrabi et al., 2019). In order to efficiently mitigate the effect of the non-stable oxides tungsten can form, a suitable candidate to play this role is titanium. Thanks to the lower energy it requires for reaction (1) with respect to tungsten (Guo and Robertson, 2014; Kim et al., 2016), titanium can indeed extract oxygen from the "I" layer more effectively, and so hinder the formation of metastable tungsten oxides. Furthermore, in the perspective of possible future applications and integrations, the strength of titanium as a suitable candidate for buffer layers comes from its capability to allow gradual RESET transitions for multiple resistance levels tuning (Shahrabi et al., 2019).

In this work, a systematic study of the effect of titanium-based buffer layers enclosed between a tungsten electrode and an oxide layer is carried out on RS devices exhibiting hafnium oxide (HfO_2) as the insulating layer of the MIM structure and platinum as the inert electrode. The role played by Ti in modulating the interaction between the oxidizing electrode and the oxide is investigated through an extensive, comparative investigation of devices with buffer layers having different thicknesses and different compositions. Devices without a buffer layer, namely with the tungsten electrode in direct contact with the HfO_2 film, are also tested and kept as performance references. A clear effect of thickness is observed in both static and dynamic operations, with lower and tunable forming, SET and RESET voltages, better endurance, and faster response achieved through a thicker Ti-based buffer layer. Especially, with respect to devices without any buffer layer, the early HRS failure is fixed and pulses down to three orders of magnitude shorter can be employed. These results, coupled with gradual RESET transitions, make the Ti buffer/W electrode stack a versatile candidate for CMOS-compatible ReRAM cells to be employed in brain-inspired applications.

MATERIALS AND METHODS

Device Fabrication

For our devices, a cross-point geometry was adopted, with VIA openings defining the active region of the ReRAM cells. Using a standard 4-in. Si wafer with a 500-nm-thick SiO_2 layer as a substrate, platinum electrodes were first defined, starting with sputtering deposition of a 5-nm-thick titanium adhesion layer and a 125-nm-thick Pt film by a Pfeiffer Spider 600. Patterning was then performed through photolithography and dry etching, carried out with an STS Multiplex ICP etcher. Afterwards, in order to assure electrical isolation between the electrodes, a 100-nm-thick low thermal oxide (LTO) was deposited at 425°C by means of low-pressure chemical vapor deposition (LPCVD). Once the Pt electrodes were patterned and isolated, VIA openings of different sizes were defined across the LTO passivation layer performing photolithography and buffer oxide etch (BOE). Thereafter, HfO_2 and the Ti-based buffer layers were deposited, the latter with thickness varying sample by sample (1, 3, and 5 nm) and the former always 5 nm thick. Concerning the oxide, atomic layer deposition (ALD) at 200°C was performed by means of a BENQ TFS200, while the buffer layers were deposited by room temperature sputtering, with an Alliance Concept DP650, employing two different targets: pure titanium (99.9995%) and mixed titanium–tungsten (99.99% of purity with 10% in weight of Ti). By means of the same sputtering tool, the tungsten electrode and a titanium nitride capping layer were then deposited, with thicknesses of 60 and 15 nm, respectively. Finally, to pattern the electrode and define the arrays of cross-point cells, photolithography and dry etching were performed, employing again the STS Multiplex ICP dry etcher.

Device Characterization

The device characterization was carried out through electrical tests in three different configurations, all of them performed in air at room temperature. DC sweeping mode was first adopted to evaluate the forming voltage and to inspect the cycling operation. To this aim, a parameter analyzer (Agilent B1500) was employed, applying voltage ramps at the tungsten electrode and keeping grounded the platinum one. During these measurements, a compliance current, I_{cc}, intended to prevent irreversible damages to the devices, was imposed through the internal modules of the characterization tool. Pulse measurements were instead performed to test the dynamic behavior in terms of endurance, response speed, and retention. In this case, since parameter analyzers generally suffer from pure accuracy in current limitation due to a certain delay with respect to the characteristic times of forming and SET processes (Tirano et al., 2011; Nafria et al., 2017), an external n-channel transistor (n-MOSFET) was used to control the compliance current. The device under test was connected in series to the drain of the transistor (bit line), while the source (source line) was grounded and voltages were applied at the gate (word line) to adjust the current limitation. Additionally, conductive atomic force microscopy (C-AFM), by an Asylum Research Cipher VRS, was employed to investigate the forming process directly probing the HfO_2 layer on top of the W/Ti buffer/HfO_2 stacks. Full-platinum AFM tips from Rocky Mountain Nanotechnologies were used as the top electrode in order to reproduce the same MIM structure as for the cross-point cells characterized by means of the parameter analyzer.

RESULTS

All the different stacks employed for the tested devices are summarized in **Table 1**. A 3D sketch of the device structure is then reported in **Figure 1A**, while the field emission scanning electron microscope (FESEM) image in **Figure 1B** shows the actual geometry with a top view of a single ReRAM cell. The micrograph in **Figure 1C** highlights the periodic arrangement of the devices adopted on each sample, with the different VIA diameters of 1.5, 2, 3, 5, and 10 μm. A topography image acquired by AFM in contact mode is also reported in **Figure 1D**, where a 10-μm VIA is shown.

In order to carry out a complete performance analysis suited to compare the material stacks and investigate the effect of the Ti-based buffer layers, 25 devices for each sample were first subjected to a systematic DC characterization made of forming and cycling steps. Pristine devices underwent positive voltage sweeps from 0 to 7 V with a compliance current of 1 mA; then, bipolar voltage ramps ranging from −1.5 V to 3 V were applied to the same devices to test the cycling behavior. Bipolar resistive switching, with SET and RESET occurring in positive and negative polarity, respectively, was observed for all the devices regardless of the material stack. The latter, conversely, turned out to play a role in the definition of the device performance. First of all, an impact of the titanium-based buffer layers on the forming process was observed, with a decrease of the forming voltage ($V_{FORMING}$) for thicker buffer layers (**Figure 2A**). Particularly, as presented

TABLE 1 | Material stacks of all the tested devices.

Sample name	Inert electrode		Oxide layer		Buffer layer		Oxidizing electrode	
	Material	Thickness (nm)	Material	Thickness (nm)	Material	Thickness (nm)	Material	Thickness (nm)
noBuffer	Pt	125	HfO_2	5	–	–	W	60
mixBuffer	Pt	125	HfO_2	5	W:Ti 10%	3	W	60
Buffer1	Pt	125	HfO_2	5	Ti	1	W	60
Buffer3	Pt	125	HfO_2	5	Ti	3	W	60
Buffer5	Pt	125	HfO_2	5	Ti	5	W	60

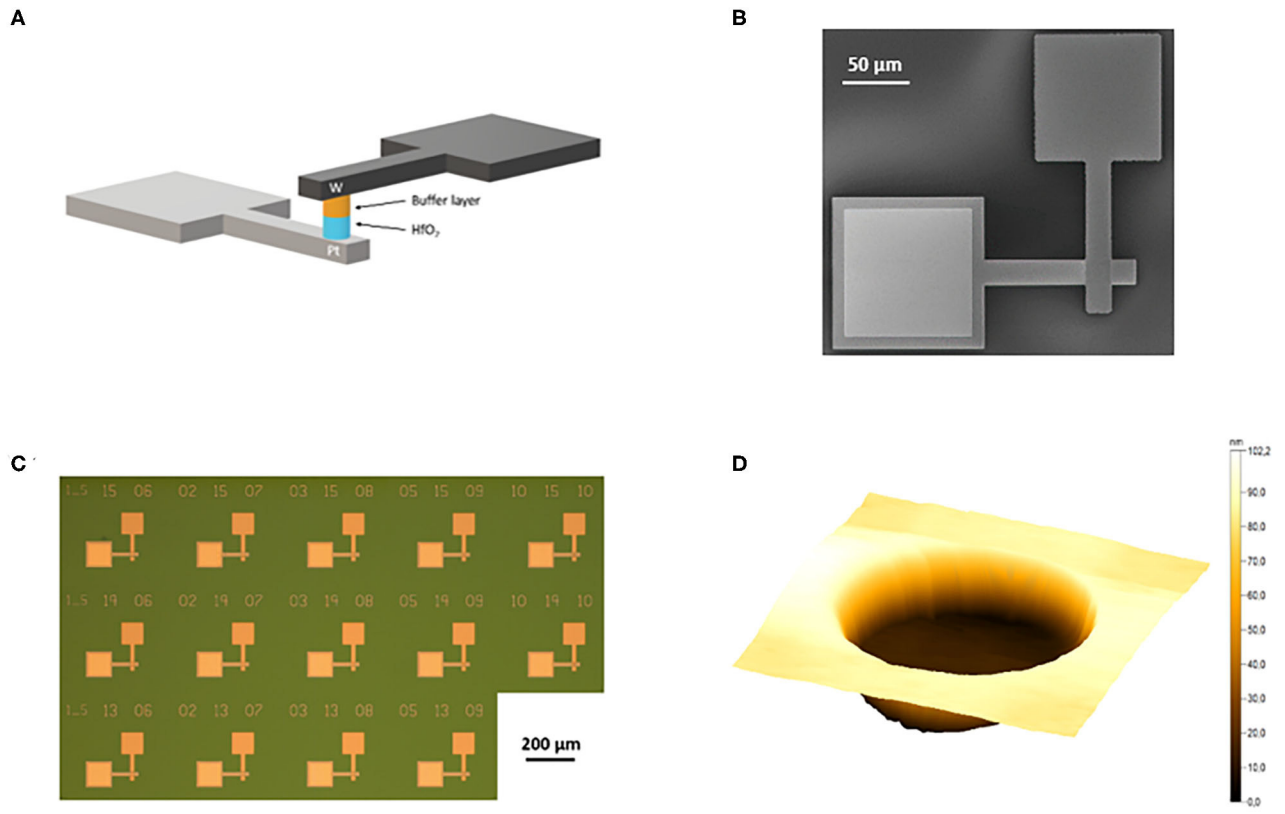

FIGURE 1 | The cross-point geometry of the tested devices is shown through a 3D sketch **(A)** and a field emission scanning electron microscope (FESEM) image in *top view* **(B)**. In the first case, the schematic, not to scale, focuses on a single device emphasizing the material stack, while in the second picture the actual geometry is shown. The periodic arrangement of the resistive random access memory (ReRAM) cells with all the different vertical interconnect access (VIA) dimensions is then highlighted by a micrograph **(C)**. In **(D)**, a single VIA with a diameter of 10 µm is shown by a topography image obtained with contact mode atomic force microscopy (AFM).

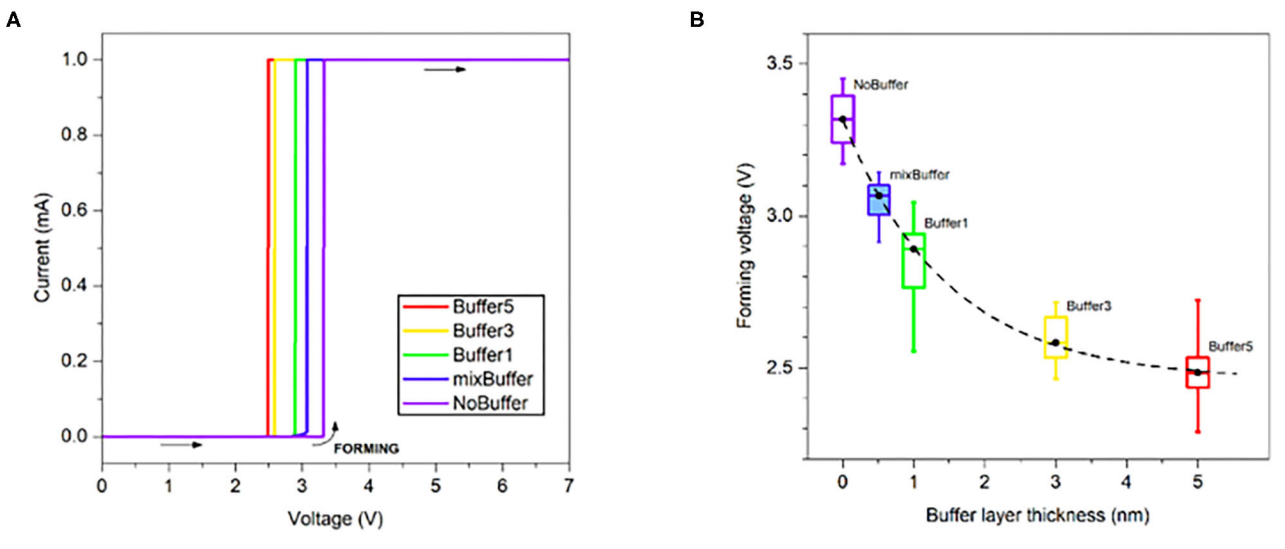

FIGURE 2 | The median values of $V_{FORMING}$ for each material stack show a dependence of the forming process on the buffer layer. In **(A)**, the corresponding *I–V* characteristics are shown, while in **(B)** their exponential decay as a function of the Ti-based buffer layer thickness is presented.

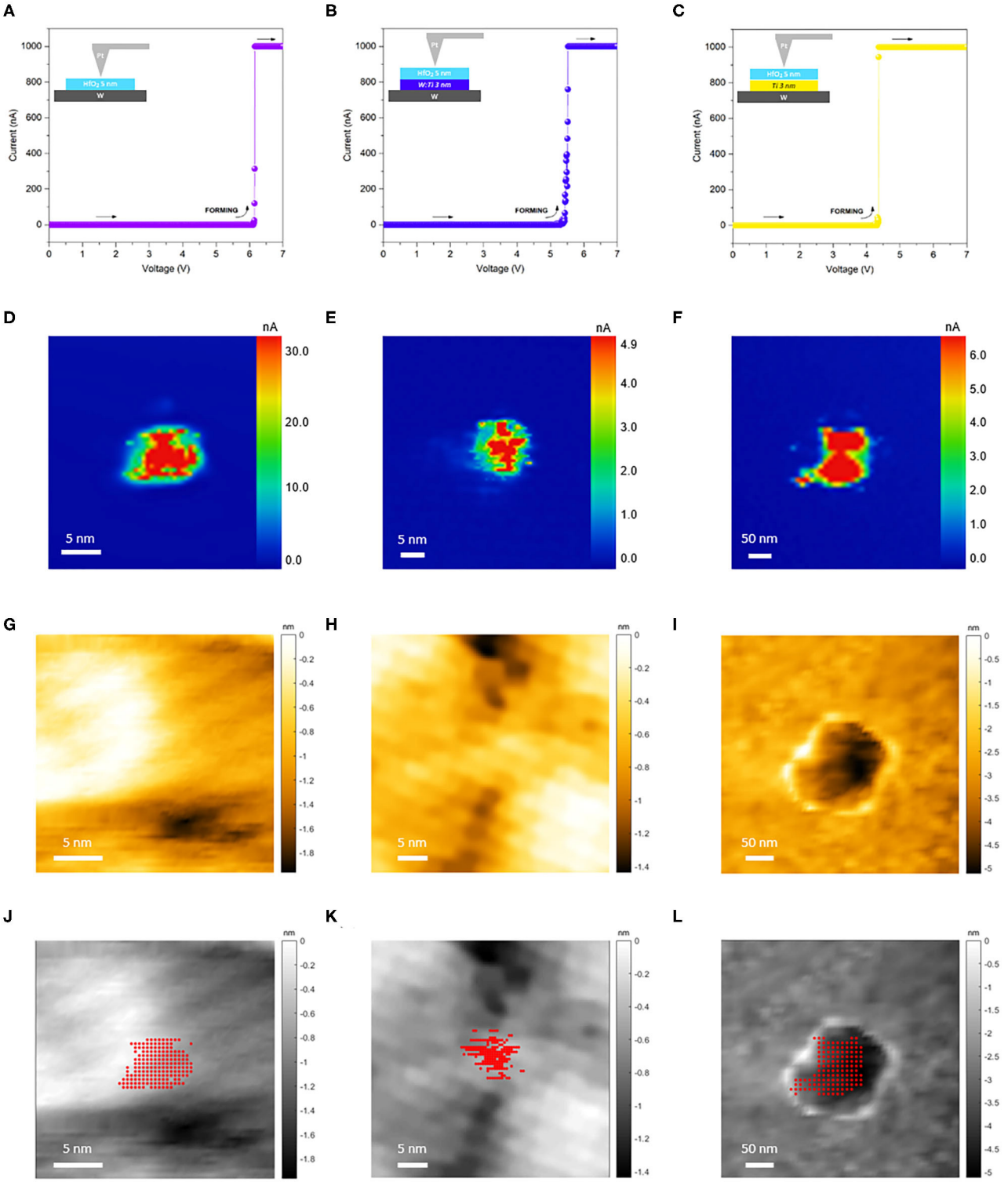

FIGURE 3 | Investigation of the forming process was performed with conductive atomic force microscopy (C-AFM) directly probing the oxide layer by means of full-platinum tips. The resulting *I–V* characteristics are reported in **(A–C)**, where $V_{FORMING}$ is reported to decrease with increasing amount of titanium in the buffer layer. In **(D–F)**, the current maps acquired after the forming process are reported, with conductive spots clearly shown for all the tested material stacks. The topography images obtained at the same time with the current maps are then reported in **(G–I)**, showing the presence of morphological changes in the case of the Buffer3 samples **(I)**. In **(J–L)**, the superposition of topographical and electrical images is presented.

by the box plot in **Figure 2B**, such a reduction turned out to be well-described by an exponential decay of the median values of $V_{FORMING}$ for the samples with pure Ti buffer layers. The same curve was then employed, the other way around, to define an effective thickness of the mixed buffer layer, which came out to be about 0.5 nm. Such an effective thickness, smaller than the real one of 3 nm, clarifies that the key player in the reduction of the forming voltage is not properly the thickness of the buffer layer but rather the presence, and the amount, of titanium between the hafnium dioxide film and the tungsten electrode.

Consistent results were shown by the C-AFM characterization too. As reported in **Figures 3A–C**, three different stacks were investigated, namely NoBuffer, mixBuffer, and Buffer3, with the structure sketched in the insets of **Figures 3A–C**. As is clear from those pictures, the same MIM geometry as the one schematized in **Figure 1A** was reproduced thanks to the full-platinum AFM tip, which played the role of the inert electrode. By selecting such triplet of stacks, the key points of the previous analysis were further investigated. Indeed, with this set of devices, two main comparisons were possible, namely (i) the case with or without the buffer layer and (ii) the case of pure or mixed titanium with a fixed thickness. For each sample investigated by means of C-AFM, forming was induced first and current maps were produced afterwards. For both the measurements, the platinum tip was kept grounded and voltages were applied at the tungsten electrode. To achieve forming, voltage sweeps from 0 to 7 V were employed as for the analysis carried out through the parameter analyzer, with a current compliance set at 1 μA. Current maps were instead produced applying fixed voltages. Similarly to **Figures 2A**, **3A–C** show a reduction of $V_{FORMING}$ depending on the presence of titanium between the oxidizing electrode and the oxide layer. Furthermore, in accordance with **Figure 2B**, such a reduction turned out to be related to the amount of titanium in the buffer layer rather than to the physical thickness of the Ti-based layer only. Indeed, both the buffer layers employed for the mixBuffer and Buffer3 samples are 3 nm thick, but their compositions differ from one another, with the mixBuffer sample exhibiting a tungsten film with 10% in weight of titanium instead of a pure Ti film. The current maps, produced after forming was induced, are then reported in **Figures 3D–F**. They show a nanometer-sized conductive spot for each sample, which strongly suggests a filamentary nature of the resistive switching in the tested devices. The topography images, acquired simultaneously with the creation of the current maps, are reported too (**Figures 3G–I**), and a superposition of the current maps on the topography images is presented in **Figures 3J–L** as the result of a point-by-point analysis of the electrical conduction. Particularly, in the case of Buffer3 samples, the presence of morphological changes is reported (**Figure 3I**), and **Figure 3L** highlights that such modifications turn out to perfectly match with the conductive spot found in the current map.

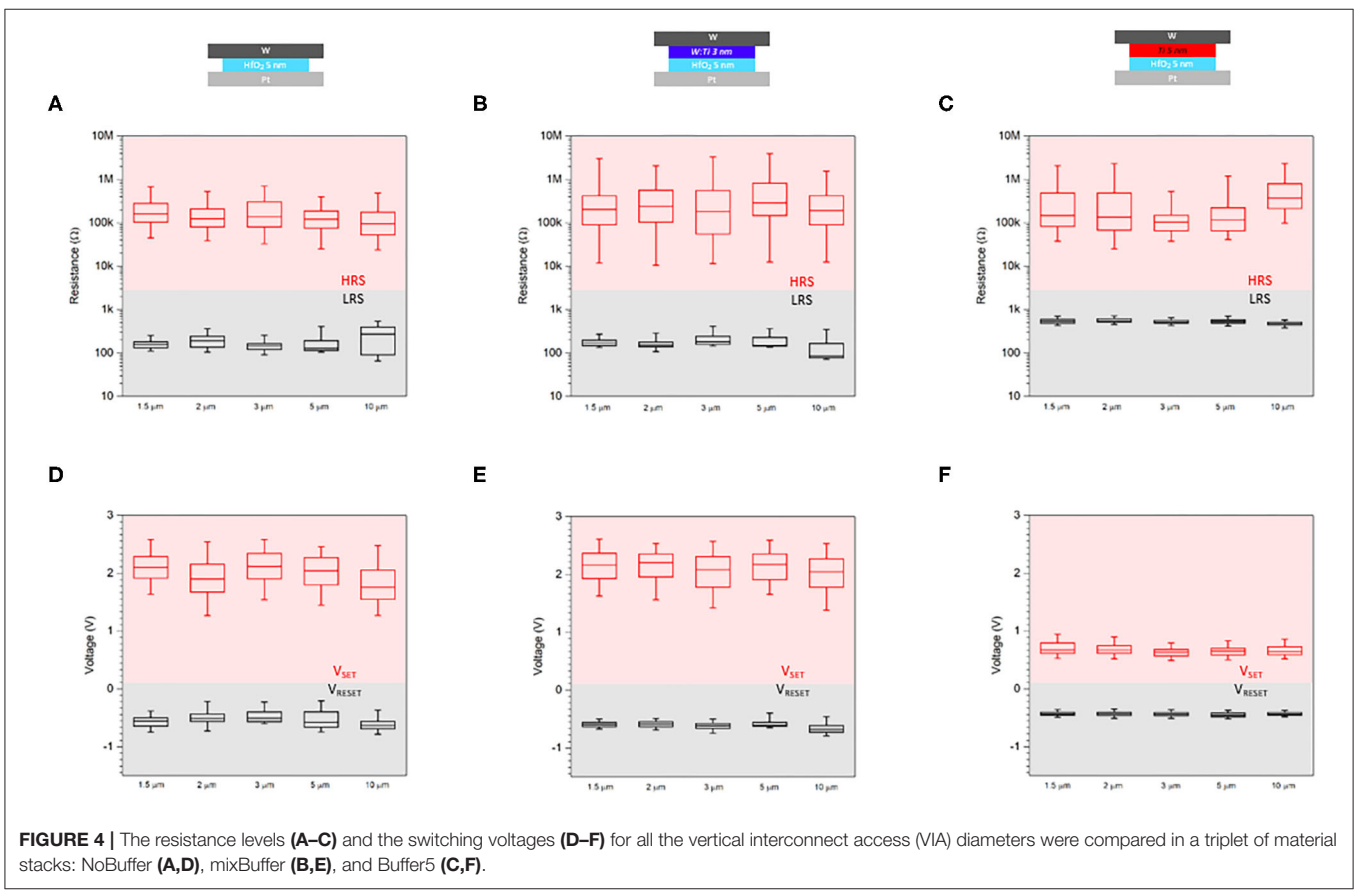

FIGURE 4 | The resistance levels **(A–C)** and the switching voltages **(D–F)** for all the vertical interconnect access (VIA) diameters were compared in a triplet of material stacks: NoBuffer **(A,D)**, mixBuffer **(B,E)**, and Buffer5 **(C,F)**.

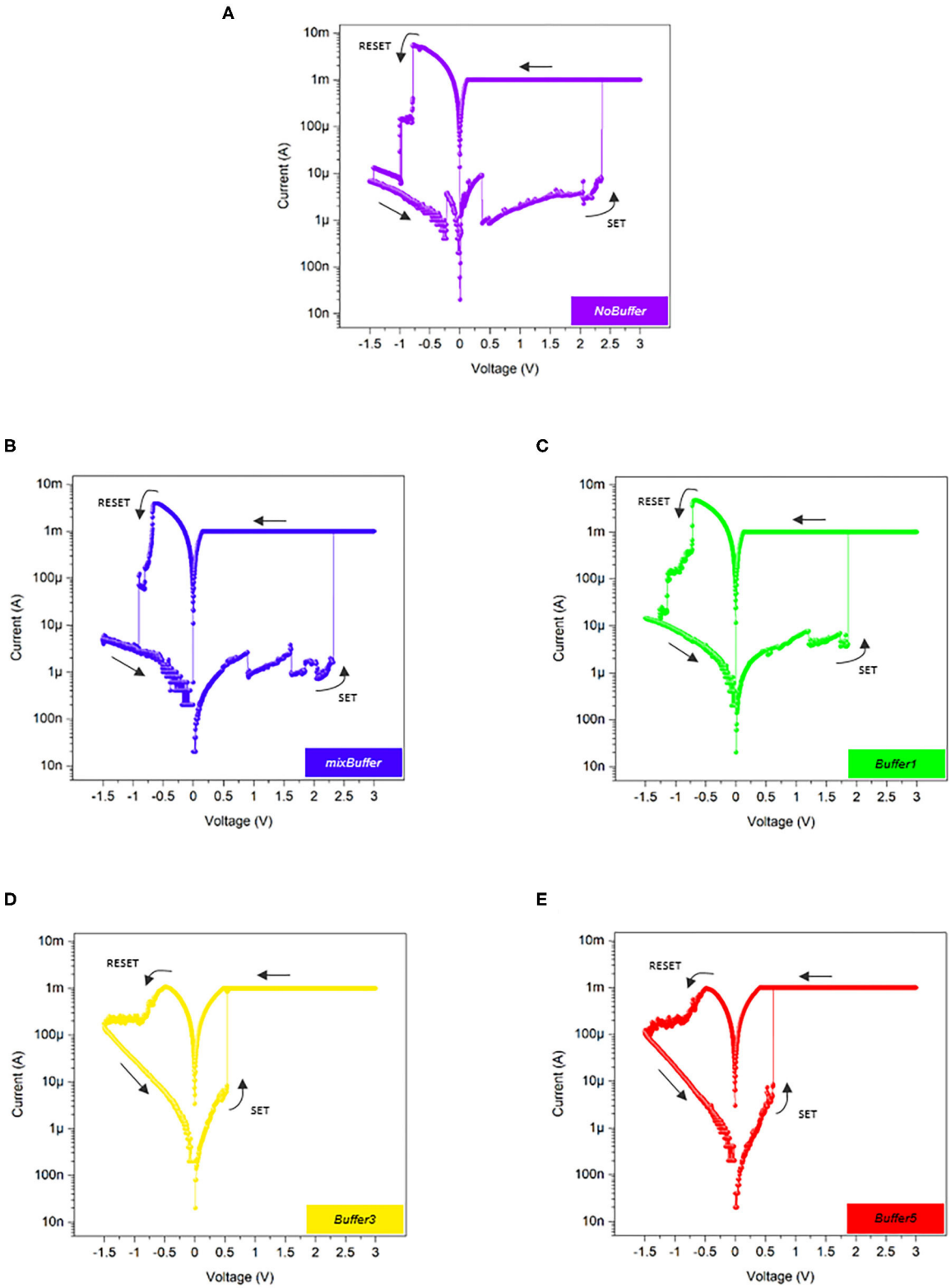

FIGURE 5 | Applying bipolar voltage sweeps, the switching behavior of the tested device was investigated through the resulting *I–V* characteristics. The reported graphs are representative curves for each material stack. In the NoBuffer samples **(A)**, current fluctuations occur before the SET process and RESET takes place abruptly. A similar behavior is shown by the mixBuffer **(B)** and Buffer1 **(C)** samples also. In the Buffer3 **(D)** and Buffer5 **(E)** samples, instead, the current fluctuations in the high-resistance state (HRS) in positive polarity are not observed; a lower V_{SET} is found and gradual RESET occurs as it is flagged by a smooth current decrease for negative voltages close to V_{RESET}.

Even though the C-AFM analysis clearly reported the presence, in all the tested material stacks, of conductive spots at the HfO_2/Pt interface, suggesting resistive switching of filamentary type, a statistical DC characterization was performed to exclude a dependence of the RS on the device area as a consequence of interfacial effects at the W/HfO_2 or buffer layer/HfO_2 interface. By means of the parameter analyzer, bipolar voltage sweeps in the range −1.5 to 3 V were applied on 25 devices for the NoBuffer, mixBuffer, and Buffer5 samples. As summarized by the box plots in **Figure 4**, such characterization revealed that RS parameters like the resistance levels, V_{SET}, and V_{RESET} are independent of the device area since no correlation was found between these quantities and the diameter of the VIAs (1.5, 2, 3, 5, and 10 μm). Therefore, we can conclude that the observed resistive switching can be truly ascribed to a filamentary mechanism.

Through the same DC characterization, that is to say applying consecutive cycles of bipolar voltage sweeps 0 V → −1.5 V → 3 V → 0 V, the switching behavior of the devices was investigated. As is reported in **Figure 5**, where *I*–*V* characteristics representative of a typical cycle for each material stack are shown, two different behaviors can be highlighted in the DC operation regime for Ti-based buffer layers thinner or thicker than 3 nm, respectively. More in detail, starting from **Figure 5A**, which reports the cycling behavior of the devices with no buffer layer, clear current fluctuations can be appreciated in the HRS for positive voltages. Interpreted from a different, but complementary, perspective, **Figure 5A** shows that the devices without a buffer layer exhibit some instability during the SET process, with sharp transitions from HRS to LRS occurring at relatively high voltages only after quick, repeated current variations. A similar behavior can be observed in the case of the mixBuffer (**Figure 5B**) and Buffer1 (**Figure 5C**) samples too, while a clear change occurs in the Buffer3 (**Figure 5D**) and Buffer5 (**Figure 5E**) samples. The latter two, indeed, still exhibit abrupt switching from HRS to LRS, but the sharp transition takes place at lower voltages and the *I*–*V* characteristics in HRS in positive polarity are much more stable, with no fluctuations. Moreover, as is graphically summarized in **Figure 6A**, which reports the statistical variations of V_{SET} and V_{RESET} obtained from the DC characterization, such improved stability in the device operation is coupled to a significantly reduced device-to-device variability.

The second major result arising from the insertion of a Ti-based buffer layer, which becomes apparent for Buffer3 and Buffer5 samples as for the HRS stability above-mentioned, involves the opposite polarity and the opposite transition. In **Figures 5D,E**, indeed, a fairly different behavior in the transition from LRS to HRS can be appreciated, with a gradual resistance variation instead of an abrupt switch. Interestingly, such change does not reflect into an increased device stability or reduced device-to-device variability. As reported in **Figure 6A**, indeed, differently from V_{SET}, the RESET voltage does not significantly vary neither from a device to another nor from a sample to another. Similar observations can be made for the resistance values also, whose statistical analysis is reported in **Figure 6B**. In this case, the effect of Ti-based buffer layers as a stabilizer can be appreciated looking at the variability of the LRS in the different samples. As is clear from the box plot, the resistance value of the highly conductive state is significantly more stable in Buffer3 and Buffer5 samples, while a relevant device-to-device variability affects the devices based on the other material stacks.

The statistical parameters resulting from the DC characterization performed on a total of 125 devices are summarized in **Table 2**.

Based on reaction (1), both the current fluctuations before SET occurs and the gradual RESET can be interpreted referring to oxygen exchanges, which, in turn, involve the oxidizing activity

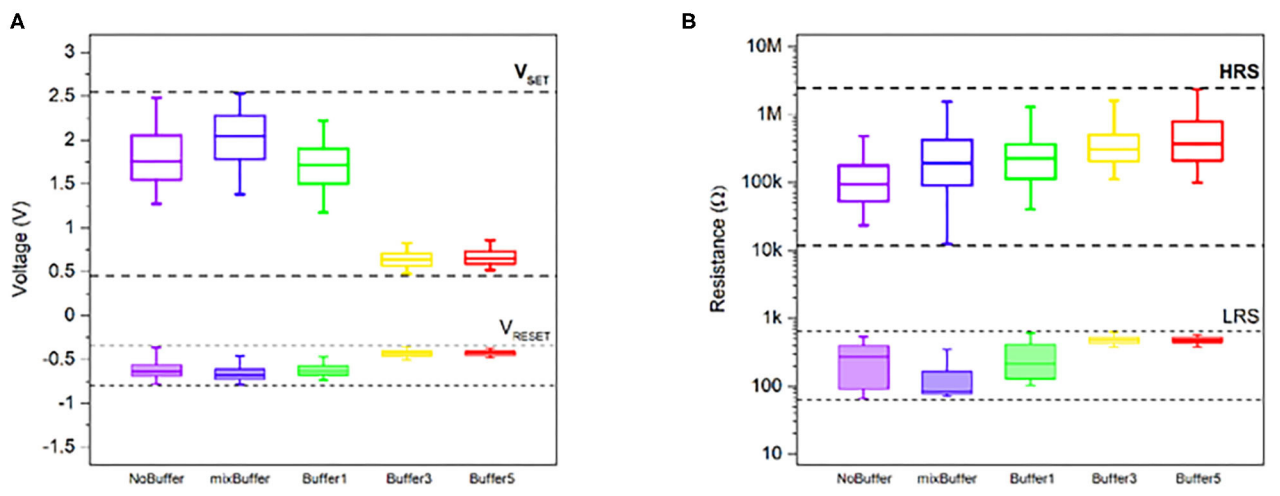

FIGURE 6 | The statistical analysis of the DC characterization performed on 25 devices for each material stack is presented by means of *box plots*. In **(A)**, the switching voltages are reported, while the resistance levels are shown in **(B)**. In both cases, for the sake of clarity, *dashed lines* are employed to distinguish the different ranges of data.

TABLE 2 | Median values and standard deviations from the statistical DC characterization.

Sample name	$V_{FORMING}$ (V)		V_{SET} (V)		V_{RESET} (V)		HRS (kΩ)		LRS (Ω)	
	Median	SD	Median	SD	Median	SD	Median	SD	Median	SD
noBuffer	3.31	0.09	1.76	0.38	−0.64	0.12	94.48	154.61	272.55	171.05
mixBuffer	3.07	0.08	2.05	0.34	−0.68	0.10	192.86	3711.84	84.86	84.86
Buffer1	2.89	0.15	1.72	0.32	−0.63	0.09	226.78	427.42	214.86	169.08
Buffer3	2.58	0.09	0.64	0.10	−0.43	0.04	309.41	499.79	483.00	77.28
Buffer5	2.49	0.12	0.65	0.10	−0.43	0.03	368.39	1011.09	474.82	69.09

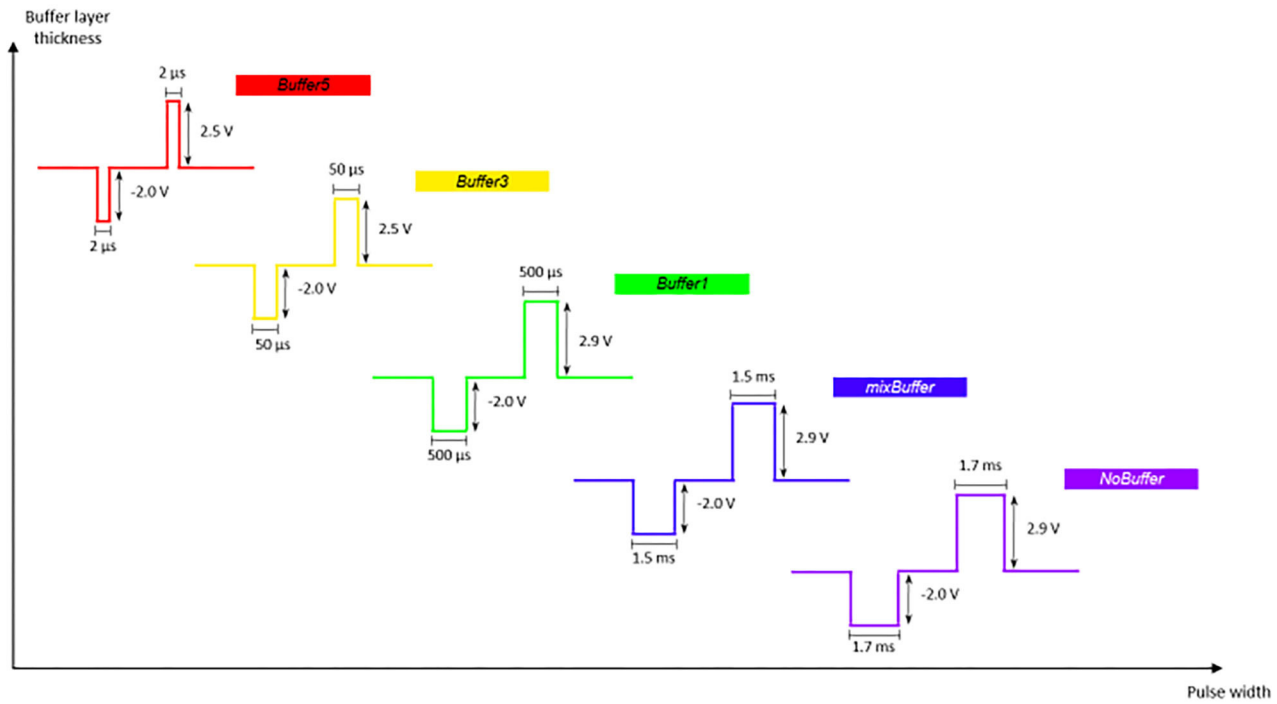

FIGURE 7 | The insertion of buffer layers with increasing amount of titanium translates into a faster response of the devices, as shown by the pulse width reduction achieved with thicker Ti-based buffer layers.

of the layers in contact with the hafnium dioxide. Since, as already mentioned, one of these layers is always made of platinum, which is inert, the two phenomena must be related to the buffer layer, or to the tungsten electrode when the former is not present. In this view, the interpretation of the observed behavior in the DC regime can be traced back to the different oxidizing characteristics of titanium and tungsten. Current fluctuations may be related to the multiple, metastable oxides tungsten can form before reaching the stable WO_3 (Lassner and Schubert, 1999; Shahrabi et al., 2019) since the emergence of such fluctuations can be appreciated in the NoBuffer, mixBuffer, and Buffer1 samples only. In the Buffer3 and Buffer5 samples, indeed, the thickness of the buffer layers is such that a large enough amount of titanium is present to effectively hinder the formation of metastable tungsten oxides (Shahrabi et al., 2019). On the other hand, concerning the transition from an abrupt to a gradual RESET, similar arguments hold, and the smoother resistance change can be again ascribed to the oxidizing behavior of the buffer layer. The gradual transition, indeed, takes place in the Buffer3 and Buffer5 samples only, that is to say, once more, only in those devices with a large enough amount of titanium between the tungsten electrode and the hafnium dioxide.

A further confirmation of the stabilizing effect given by the titanium buffer layer was then found with pulse tests aimed at investigating the endurance of the devices, namely their cycling reliability. For each material stack, an initial optimization procedure was first performed on the pulse parameters in order to find the best combinations of pulse width and pulse amplitude. As is shown in **Figure 7**, pulses were optimized for both SET and RESET since, as shown by the DC characterization, the bipolar RS of the tested devices is not symmetrical. Specifically, $|V_{SET}|$ turned out to be higher than $|V_{RESET}|$, while identical pulse widths were used in both polarities. Finally, a delay of 200 ms was always employed between a pulse and the following one.

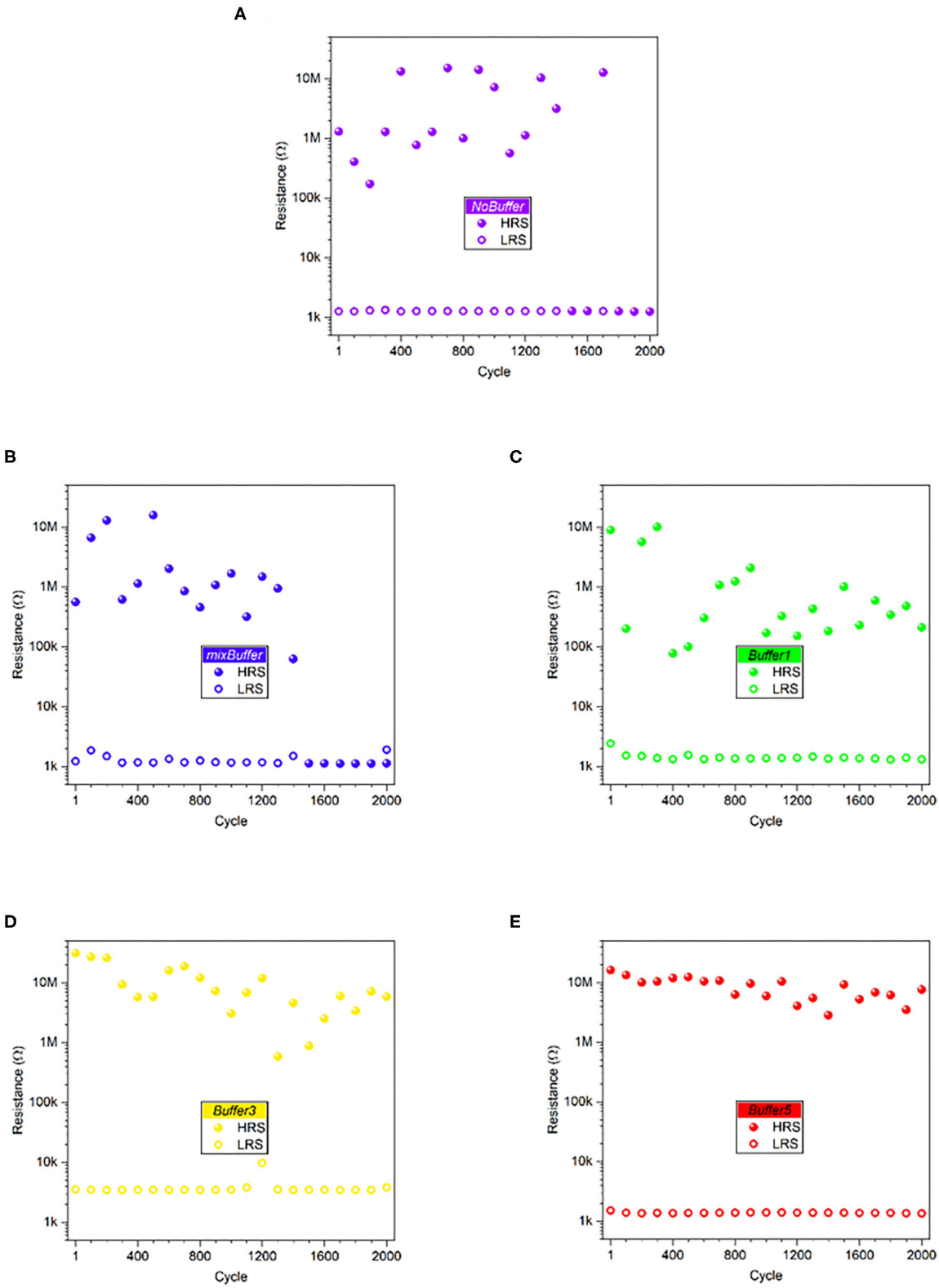

FIGURE 8 | Endurance tests were performed with a fixed sequence of 2,000 SET–RESET pulse pairs. The NoBuffer **(A)** and mixBuffer **(B)** samples showed high-resistance state (HRS) failure after about 1,500 cycles, while the devices from the other material stacks **(C–E)** successfully completed the fixed-length test. Additionally, a stabilization of the HRS was observed for the Buffer1 **(C)**, Buffer3 **(D)**, and Buffer5 **(E)** samples.

TABLE 3 | Summary of resistance values during endurance and retention measurements.

Sample name	Endurance				Retention			
	HRS		LRS		HRS		LRS	
	Mean (MΩ)	Relative uncertainty (%)	Mean (kΩ)	Relative uncertainty (%)	Mean (MΩ)	Relative uncertainty (%)	Mean (kΩ)	Relative uncertainty (%)
noBuffer	4.73	119	1.27	1.4	13.22	30	1.47	4.8
mixBuffer	3.10	156	1.27	18	1.26	2.0	1.00	2.3
Buffer1	1.61	180	1.44	16	0.93	2.9	1.35	2.3
Buffer3	10.11	87	3.81	36	32.26	3.3	2.52	3.9
Buffer5	8.52	41	1.38	2.3	17.02	5.1	1.27	6.3

HRS, high-resistance state; LRS, low-resistance state.

Figure 7 clearly shows that such an optimization revealed a key impact of titanium on the dynamical operation regime of the tested devices. Indeed, besides the reduction of pulse amplitude needed for successful RS, which was already pointed out with the DC characterization, pure Ti buffer layers turned out to lead to a pulse width reduction down to three orders of magnitude with respect to the devices without a buffer layer.

Once the pulse parameter optimization was completed, a common test procedure was defined and adopted for all the material stacks, so that a clear performance comparison among the different samples was possible. Specifically, all the devices subjected to the endurance test were subjected to 2,000 SET–RESET pulse pairs aimed at continuously switching between HRS and LRS. The results of this characterization, reported in **Figure 8**, show how, besides improving the device stability, pure Ti buffer layers also have a beneficial effect on the endurance itself. **Figures 8A,B**, indeed, reveal that the NoBuffer and mixBuffer samples suffered for HRS failures preventing them from reaching the common test length of 2,000 cycles. Particularly, the devices from both material stacks were not able to overcome 1,500 cycles. Conversely, the Buffer1, Buffer3, and Buffer5 samples were all able to reach the fixed benchmark of 2,000 cycles, thus demonstrating an improvement of about 30%. Moreover, as already mentioned, the stability of the devices significantly improved, as is highlighted in **Figures 8C–E** by the much less scattered data as the amount of titanium in the buffer layers increases. A quantitative evaluation of the data dispersion can be made through the relative uncertainty (**Table 3**), which, in the case of HRS, turns out to be smaller than 100% for the Buffer3 and Buffer5 samples only. In more detail, such samples provide relative uncertainties of 87 and 41%, respectively, while 119% is found for the NoBuffer samples, 156% in the case of the mixBuffer ones, and 180% for the devices coming from the Buffer1 samples. The relative uncertainties are instead much smaller for the LRS during the endurance tests, and they do not show any trend related to the material stack.

To complete the set of electrical characterizations, retention tests were performed on new samples to compare the capability of the different material stacks of preserving each resistance state. A summary of the mean values, together with their relative uncertainties, for both HRS and LRS during pulse operations is presented in **Table 3**. As for the endurance, a common benchmark was set for the retention tests too, and 2×10^4 s was adopted as the fixed length for the measurements in order to define a standard procedure for all the samples. The results are shown in **Figure 9**, where a good stability is reported for all the material stacks. In this case, no significant difference can be appreciated depending on the buffer layer, with all the devices able to reach the fixed value of 2×10^4 s and small relative uncertainties on the resistance values, in both HRS and LRS. As a consequence, the retention tests, which rely on the stability of the conductive filament rather than on its formation and rupture, seem to suggest that the Ti-based buffer layers actively play a role only when oxygen exchanges, as in reaction (1), occur, while they remain silent otherwise. The performance tunability and improvement titanium allows to achieve can hence be directly related to the stabilization of the interactions between the oxidizing electrode and the oxide layer. Compared to tungsten, titanium indeed requires a much lower energy to create oxygen vacancies in HfO_2, and this significantly hinders the slower tungsten oxidation (Kim et al., 2016). As a consequence, titanium efficiently mitigates the fluctuations induced by the formation of metastable tungsten oxides (Lassner and Schubert, 1999) and allows faster responses from the devices.

DISCUSSION

With this work, we have shown how titanium can be employed, as a buffer layer, to stabilize and tune the RS performances of ReRAM cells based on CMOS-compatible materials like HfO_2 and tungsten. With an extensive, systematic approach, 125 devices with different material stacks have been tested. Investigating different thicknesses and compositions of the Ti-based films, a dependence of the device performances on the buffer layer properties was found, and the amount of titanium in the buffer layer turned out to play a key role. The presented results can be ascribed to the different oxidizing characteristics of titanium and tungsten. The latter, indeed, suffers from a relatively slower oxidation process, producing a variety of metastable oxides, responsible for the RS instability which clearly appears in both DC switching and pulse operations. Employing buffer

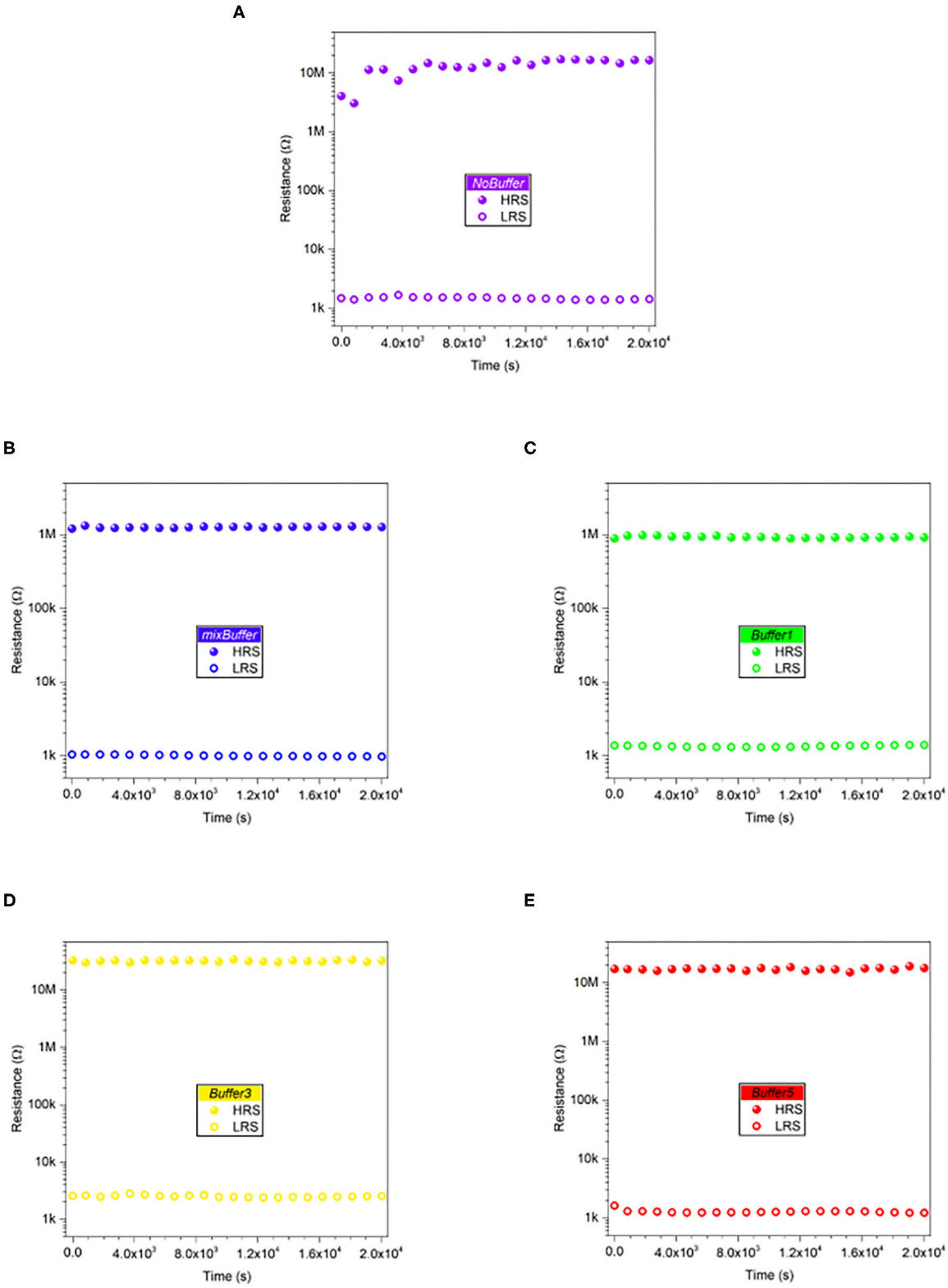

FIGURE 9 | (A–E) Retention measurements, performed for a fixed time of 2×10^4 s, highlighted that a good resistance state stability is provided by all the material stacks, with no significant contribution given by titanium.

layers with a high enough amount of titanium, relevant changes in the device performances have been reported. More in detail, the response speed has been shown to significantly increase according to the pulse width reduction of three orders of magnitude; an improvement of about 30% has been achieved in terms of endurance performance, and an increased stability of the resistance states, especially the HRS, has been obtained in the dynamic operation regime. In light of these results, the Ti buffer/W stack turns out to be a suitable choice for CMOS-compatible ReRAM cells that have to solve reliability issues coming from tungsten electrodes. Furthermore, the possibility of tuning the device performances according to the Ti-based buffer layer properties may open the way to the definition of new design rules for ReRAM integration with standard CMOS technology.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

VF and ES contributed to the design and fabrication of the devices. VF performed device characterization. VF and CR wrote and revised the manuscript. CR and YL helped with supervision. All authors contributed to the article and approved the submitted version.

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Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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