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A 3 GHz Spread Spectrum Clock Generator for SATA Applications Using Chaotic PAM Modulation

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***Abstract*— This paper proposes a prototype of a Spread Spectrum Clock Generator which is the first known specifically meant for 3 GHz Serial ATA-II applications. The modulation is obtained from a fractional PLL which employs a Delta-Sigma modulator. A further innovative aspect of our work is that our prototype takes advantage of a *chaotic* PAM as driving signal, instead a triangular signal as in all spread spectrum generators proposed in literature for SATA-II. In this way we avoid the periodicity of the modulated clock, completely flattening the peaks in the power spectral density. The circuit prototype has been designed in 0.13 μm CMOS technology and achieves a peak reduction greater than 14 dB measured at RBW = 100 kHz. The chip active area is 0.27×0.78 mm^2 and the power consumption is as low as 14.7 mW.**

I. Introduction

The reduction of Electro-Magnetic Interference (EMI) in electronic devices is an issue of increasing interest for designers. Digital signals, due to their sharp edges and their synchronization with a periodic clock signal, are preeminent sources of interference. In particular, several problems may arise with high–speed serial interfaces connecting signal processing units and peripheral devices. Interestingly, many of the protocols employed to this purpose explicitly mention EMI-related problems, as well as possible solutions. Among them, we can include the Serial AT Attachment (*SATA*) protocol [1].

This computer bus technology is designed for fast data transmission to and from Hard Disk Drives, according to the most recent specifications (known as SATA-II), at a clock speed of 1.5 GHz or 3.0 GHz. The protocol also allows the introduction of *spread spectrum* techniques on its clock signal, in order to perform an intrinsic EMI reduction.

The spread spectrum clock technique consists of introducing a continuous and slight *delay* or *anticipation* in the reference clock edges, thus avoiding a perfect periodicity. The result is the introduction of new components in the power spectra of all synchronous signals, but also a reduction in their peak level. This point of view is perfectly coherent with FCC and EC regulations [2] that link EMI compliance with the ability of fitting the interfering power spectrum below a predefined mask.

The most common way to get a spread spectrum clock is through a *frequency modulation* of the clock signal [3]:

$$s(t) = \mathrm{sgn}\left(\cos\left(2\pi f_0 t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)d\tau\right)\right) \qquad (1)$$

where f_0 is known as carrier frequency, Δf is the frequency deviation and $-1 < \xi(\tau) < 1$ the driving signal. If we refer to the first harmonic, its energy is spread, according to Carson's rule, into the frequency band $[f_0-\Delta f, f_0+\Delta f]$. Of course, this may impair the synchronization process between transmitter and receiver; for this reason it is necessary that the receiver device is designed to be compatible with the introduced modulation. This is particularly important in asynchronous applications, like the Serial ATA, to allow a correct clock recovery. To this purpose, the SATA-II protocol fixes the modulation parameters, allowing only a 30–33 KHz driving signal $\xi(t)$ and a 5000 ppm *down-spreading* frequency deviation [1]. Intuitively assuming that f_0 is the non-modulated clock frequency, a down-spreading is an asymmetric modulation where the output frequency cannot exceed f_0. In this way the allowed spreading band is $[f_0-2\Delta f, f_0]$. If we recast equation (1) to fit SATA-II specifications, we get $\Delta f = 0.005 \cdot f_0/2$

Under the above constraints, the performance of the system in terms of EMI reduction (measured as the reduction of the peak level in the power spectrum) depends only on the driving signal $\xi(t)$ employed, which is the only degree of freedom. Poor results are given by a simple sinusoidal $\xi(t)$ signal; better performances can be achieved with a triangular waveform; while we can get even better performances with a more complicated periodic driving signal [3]. Recently, many papers in literature proposed a 1.5 GHz spread spectrum clock generator for SATA-II [4], [5], [6], [7] employing a triangular waveform as modulating signal. Almost all of them are based on a fractional PLL employing a $\Delta\Sigma$ modulator.

In this paper we present a prototype of a spread spectrum clock generator which is the first one running at 3 GHz that is SATA compatible. A further fundamental difference between the prototype presented here and others proposed in literature is that our generator does not exploit a triangular driving signal, but a uniform chaotic PAM modulated driving signal, i.e. where $\xi(t)$ is a sequence of impulses whose amplitude is given by a chaotic system. The advantages of a chaotic modulation are known in literature [8] and can be summarized as a complete lack of peaks in the power spectrum when using the proper parameters.

In fact the modulation index m, defined as the ratio between the frequency deviation Δf and the frequency f_m of the modulating signal $\xi(t)$ (i.e. $m = \Delta f/f_m$) is very high in the case of serial ATA-II. We get $m \simeq 110$ for a 1.5 GHz SATA clock and $m \simeq 220$ for a 3.0 GHz SATA clock. It is shown in [8] that under this assumption the uniform chaotic PAM modulation outperforms any periodic modulation, including the patented modulation proposed in [3]. A sketch comparison between the power spectra of a triangular modulation, the proposed chaotic modulation and of an unmodulated clock can be observed in Figure 1. The advantage in terms of EMI reduction of the proposed modulation with respect to the triangular one depends on the resolution bandwidth used in evaluating the spectrum (which may represent the sensitivity of the EMI victim); the narrower the bandwidth, the larger the difference. As an example, when using the parameters allowed by the 3 GHz SATA-II spread-spectrum clock and a resolution bandwidth of 10 kHz the proposed chaotic modulation achieves a theoretical additional EMI reduction of about 7 dB.

The paper is organized as follows. Section II explains the working principle of the prototype and presents a few simulation results. The measurement results are presented in

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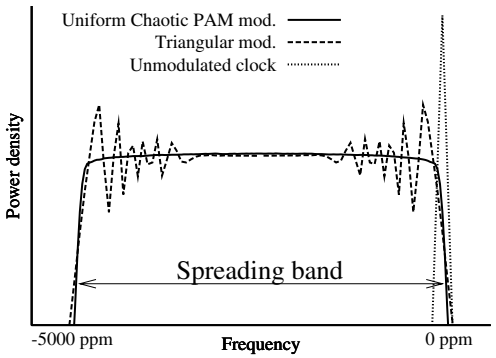

Fig. 1. Sketch comparison between the power spectra of an unmodulated clock (dotted line) and of a clock with a down-spreading modulation employing a triangular signal (dashed line) and a chaotic PAM signal (continuous line).

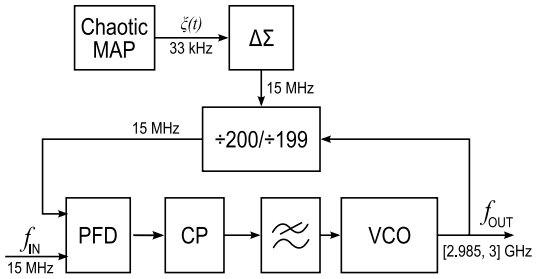

Fig. 2. Block diagram of the proposed spread spectrum clock generator.

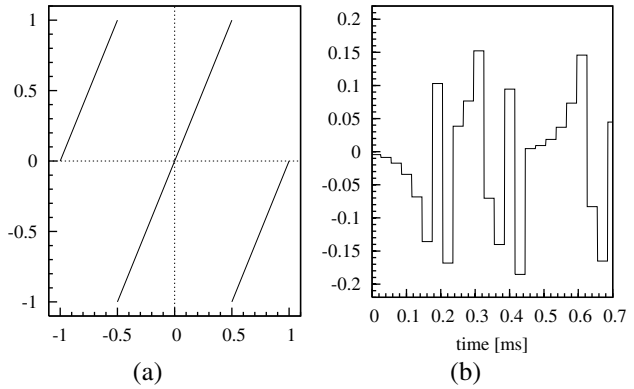

Fig. 3. (a) ideal M implemented in the prototype; and (b) output signal $\xi(t)$ of the chaotic map from circuital simulation (differential voltage).

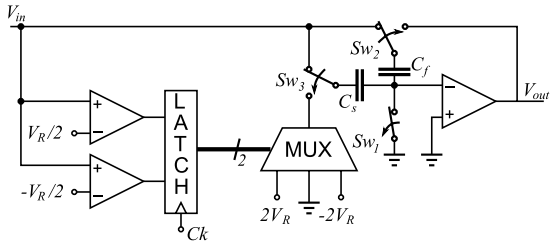

Fig. 4. Schematic of the circuit used for implementing the chaotic map of Figure 3-a.

section III, whereas conclusions are given in the last section.

II. Proposed Spread Spectrum Clock Generator

The block diagram of the proposed prototype is shown in Figure 2. This circuit is very similar to a classic fractional PLL [9] employing a phase/frequency detector, a charge pump, a low-pass filter, a VCO and an integer divider on the feedback path. The divider ratio is controlled by a first-order $\Delta\Sigma$ modulator, thus exploiting a fractional divider under the assumption of a low frequency $\xi(t)$ signal and of a high $\Delta\Sigma$ clock frequency (with respect to the PLL closed-loop bandwidth). In this way, with an input frequency of 15 MHz, the PLL can generate any output frequency between 15 MHz $\times$ 200 = 3 GHz and 15 MHz $\times$ 199 = 2.985 GHz (that is 3 GHz $-$ 5000 ppm) with a linear dependence on $\xi(t)$.

As mentioned before, in our prototype the driving signal $\xi(t)$ is the PAM signal

$$\xi(t) = \sum_k x_k g(t - kT) \tag{2}$$

where $g(t)$ is the impulse shape and where the coefficients x_k are given by the discrete-time autonomous system

$$x_{k+1} = M(x_k) \tag{3}$$

where $x_k \in X$ and the mapping function M is a proper non-linear function $M : X \mapsto X$. Systems such as (3) are usually referred to as *chaotic maps*; starting from an initial state x_0 (which is set in real systems by noise at circuit startup), they generate a succession $\{x_k\}$ that has very peculiar features. Roughly speaking, this is a bounded, non-periodic, deterministic sequence that, due to the increasing unpredictability of the system evolution under the assumption of noise perturbations, can be handled only as a random sequence.

The main property of these systems is that, under certain assumptions on M, they can be modeled as a stochastic process where the state x_k at time step k is a random variable with a probability density function ρ that depends only on M.

More details on a frequency modulation exploiting (2) as driving signal (*chaotic PAM modulation*), as well as a complete and extensive analysis on chaotic maps, can be found in [8]; for the purposes of this paper, it is sufficient to recall that, under the assumption of a large modulation index (defined in this case as $m = \Delta f \cdot T$) and of a rectangular-shaped impulse $g(t)$, the power spectrum of the modulated signal around the carrier frequency takes the shape of ρ. As a result, we can optimize the power spectrum using a map whose ρ does not present any peak, i.e. an *uniform* ρ. The example of Figure 1 has been obtained with a chaotic map generating symbols whose density is uniform in X.

The chaotic map we used to get the optimal symbol density is the following

$$M(x_k) = \begin{cases} 2x_k + 2 & \text{if } x_k \leq -\frac{1}{2} \\ 2x_k & \text{if } -\frac{1}{2} < x_k \leq \frac{1}{2} \\ 2x_k - 2 & \text{if } x_k > \frac{1}{2} \end{cases} \tag{4}$$

where we have assumed that X is the normalized interval $X = [-1, 1]$. This map can be found drawn in Figure 3-a. Figure 3-b instead shows a simulation of the PAM signal $\xi(t)$ representing the output of the chaotic map.

The schematic of the circuit implementing function (4) is depicted in Figure 4, and it is taken from [11], where the authors showed that this switched capacitors circuit, commonly used in 1.5 bit/stage pipeline ADC converters [10], can be conveniently used to implement the chaotic map (4) with $X = [-V_R, V_R]$ when setting $C_s = C_f$

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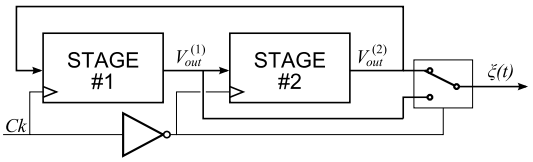

Fig. 5. Pipeline structure used to get the desired dynamical behaviour.

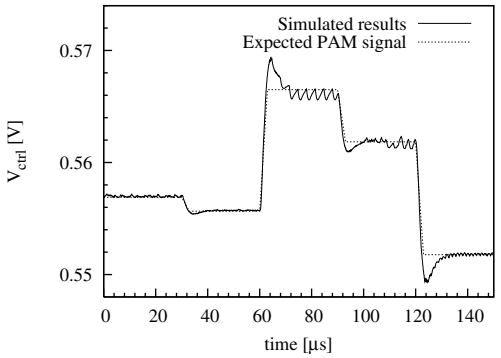

Fig. 6. VCO control voltage during a post-layout simulation (solid line), compared with the expected PAM signal (dotted line).

Note that this circuit introduces a delay of half clock cycle between output and input. In order to achieve a dynamic behaviour as in (3) it is necessary to close this circuit into a loop after a delay of full clock cycle. To get the additional delay required, we follow [11] and add another identical block working on the opposite clock phase, as in Figure 5. With this arrangement, assuming $2T$ is the period of the chaotic map clock, the symbols x_k are available alternately at the outputs of the two stages, at the rate of one symbol every time step T; to get the $\xi(t)$ as in (2) it is enough to add two simple pass transistors as in figure.

It is important to stress that the additional cost in terms of area and power consumption with respect to using a simpler delay circuit (e.g. a sample/hold) is negligible, since only the two comparators and few pass transistors are added.

Accordingly to serial-ATA specifications, the chaotic map generates the PAM signal $\xi(t)$ with a symbol rate of $1/T = 33$ kHz, while the $\Delta\Sigma$ modulator clock has been set to 15 MHz, corresponding to an oversampling ratio of about 450.

The PLL bandwidth is set to an intermediate value between the two above frequencies. In this way, the low-frequency variations of the PAM signal $\xi(t)$ can modulate the output clock, while the effect of the high-frequency variations of the $\Delta\Sigma$ modulated signal are strongly attenuated. Note that any residual modulation given by the $\Delta\Sigma$ modulator gives rise to an undesired *deterministic* jitter in the output clock. By setting the PLL closed loop bandwidth to 63 KHz, the VCO control voltage has the shape depicted in Figure 6, which compares it with the output of the chaotic map. Two remarks need here to be made: *i.* the worst case deterministic jitter introduced in the output clock by the residual modulation of the $\Delta\Sigma$ converter is experimentally evaluated in 0.4 ps rms; *ii.* due to the low frequency components of $\xi(t)$ and to the low PLL cut–off frequency, a VCO control voltage as in Figure 6 can easily be rebuilt by a clock recovery circuit. High–level simulations show that the additional jitter of the recovered clock is much lower with respect to the deterministic jitter of the transmitter clock.

As a final remark, it is necessary to stress that the chaotic map requires an analog implementation, since no digital circuit can exhibit chaotic behaviour. However, the low working frequency and the possibility of sharing the voltage references between the chaotic maps and the $\Delta\Sigma$ converter allow us a low power design. The overall power consumption of both circuits is estimated in 3.8 mW, much lower than the power consumption of the 3 GHz PLL.

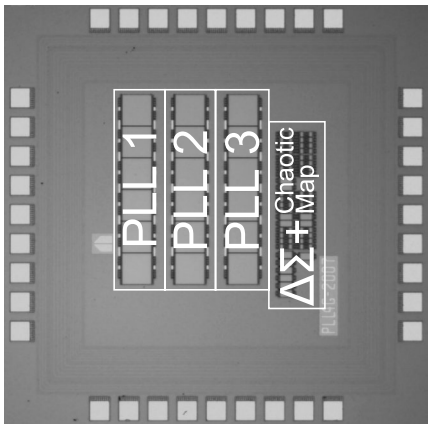

Fig. 7. Microphotograph of the chip prototype.

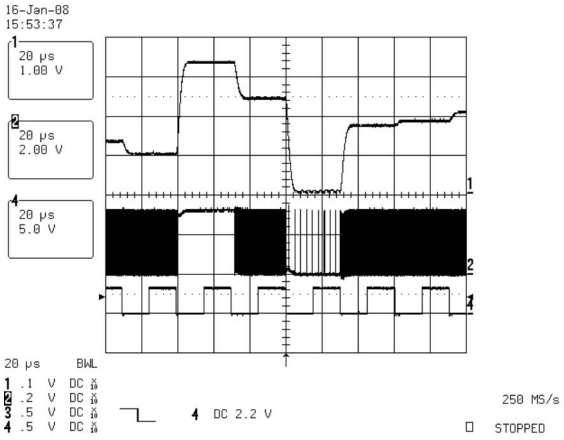

Fig. 8. Waveforms from the chaotic map/$\Delta\Sigma$ block. From bottom to top: clock of the chaotic map; driving signal $\xi(t)$ modulated by the $\Delta\Sigma$ converter; and the same signal demodulated by an external low-pass filter.

III. Measurement Results

We fabricated the 3 GHz spread spectrum clock generator SATA-II compatible in 130 nm CMOS technology. Figure 7 is a microphotograph of the chip prototype. Note that the prototype includes three different PLLs; this solution has been adopted to extend the chip tunable range from 2.5 GHZ to 3.5 GHz.

Due to this hardware replication, the power consumption of the entire chip is quite high, and it has been measured in 37 mW on the 1.2 V core power supply line. By a comparison with simulation results, we can say that the power consumption of a single PLL and of the chaotic map/$\Delta\Sigma$ block is as low as 14.7 mW.

The behavior of the block constituted by chaotic map and the $\Delta\Sigma$ modulator can be observed in Figure 8. In this figure we can found the chaotic signal $\xi(t)$ modulated by the $\Delta\Sigma$ converter (center trace) and demodulated by an external low-pass filter (upper trace), as well as the chaotic map clock (lower trace).

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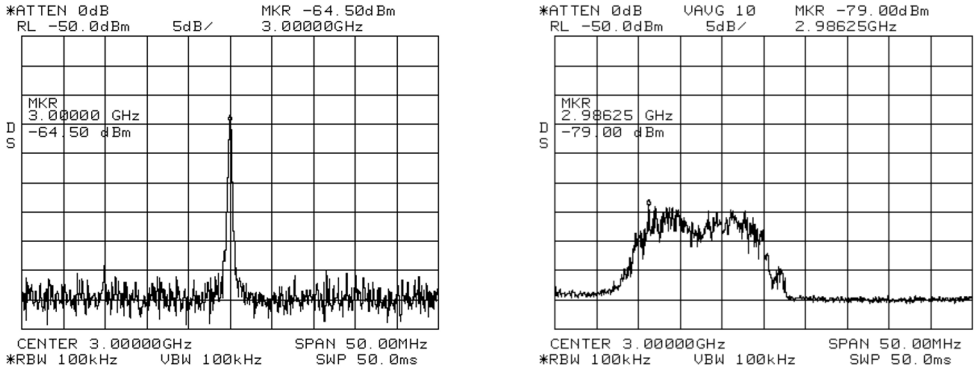
	This work	[4]	[5]	[6]	spec.
Mod. Method	$\Delta\Sigma$, chaotic	$\Delta\Sigma$, triang.	$\Delta\Sigma$, triang.	$\Delta\Sigma$, triang.	N/A
Working Frequency [GHz]	**3.0**	1.5	1.5	1.5	1.5/3.0
Mod. Freq. [kHz]	33.0	31.25	31.1	30.0	30.0-33.0
EMI Reduction [dB, RBW = 100 KHz]	**14.5**(1)	*9.6* (2)	10	9.8	>7
Spreading Ratio [ppm]	-5000/+0	5070(3)	-5000/+350	-5000/+0	-5000/+0
PLL Random jitter [ps rms]	5.9 (4)	N/A(5)	8.1	3.2	<12
PLL BW [kHz]	63	100	300	N/A	N/A
CMOS Technology [μm]	0.13	0.18	0.15	0.13	N/A
Power consumption [mW]	**14.7**	27	54	77	N/A
Chip area [mm^2]	**0.27 x 0.78**	0.44 x 0.48	0.88 x 0.48	1.75 x 0.94	N/A

(1) Since the frequency deviation is doubled with respect to the other solutions, there is a +3 dB EMI reduction since the spreading ratio is constant. In any case, this solution achieves the best reduction. (2) Paper [4] report a EMI reduction of 19.6 dB at RBW = 10 Khz; the value reported here is an estimation. (3) The exact spreading range is not indicated. (4) Estimated from phase noise. (5) A peak to peak jitter 30 ps is indicated.

TABLE I
MEASUREMENT SUMMARY AND COMPARISON WITH PREVIOUS WORKS.



(a) (b)

Fig. 9. Comparison between power spectrum of the output clock in non-spread spectrum (a) and spread spectrum (b) mode. Measurement conditions: RBW = 100 KHz, VBW = 100 KHz, Center Frequency = 3.0 GHz, Span = 50 MHz, positive peak detector mode. EMI reduction can be evaluated in 14.5 dB.

Finally, Figure 9 shows the measurements results of the output spectrum both in spread spectrum and in non-spread spectrum mode. The comparison is done at a resolution bandwidth of 100 KHz (suggested in [1]), and shows a flat spectrum in the range of interest with a peak reduction of 14.5 dB. From the measure of the phase noise in the non-spread spectrum, and accordingly to [12], we can assume a random jitter of 5.9 ps. Note also that the modulated clock spectrum presents the expected down-spreading modulation shape as expected by the SATA-II standard.

Measurement results are summarized in Table I. In the same table we also compared results from our prototype with results from other solutions in literature. All prototypes in [4], [5], [6] exploit a triangular modulation. Our prototype achieves the best performances in terms of power consumption and EMI reduction. Furthermore, it is the only one working at a 3 GHz frequency, while all other prototypes work at 1.5 GHz.

Note also that some prototypes use a spreading ratio larger than 5000 ppm. SATA-II protocol allows a ± 350 long term deviation from the main frequency, and some designers uses this additional allowed deviation for spreading purposes. However [1] clearly states that the accepted spreading ratio is only $-5000/+0$ ppm; larger ratios give rise to additional EMI reduction (up to $+0.3$ dB) making the comparison unfair.

IV. CONCLUSIONS

We developed a PLL-based spread spectrum clock generator compatible with 3 GHz serial ATA specifications. The prototype exploits a chaotic PAM modulation, thus flattening all peaks in the clock power spectrum. In fact, the EMI reduction can be measured in 14.5 dB peak reduction, that is the highest reduction among all prototypes presented in literature. Furthermore, the generator presented here achieves the lowest power consumption, which is only 14.7 mW.

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