Analog processing by digital gates: fully synthesizable IC design for IoT interfaces

Format of the tutorial: mini tutorial

Title: analog processing by digital gates: fully synthesizable IC design for IoT interfaces

Abstract

Analog integrated circuits do not take advantage of scaling and are easily the bottleneck in terms of cost and performance in Internet of Things (IoT) sensor nodes integrated in nanoscale technologies. While this challenge is most commonly addressed by devising more "digital friendly" analog cells based on traditional design concepts, the possibility to translate analog functions into digital, so that to implement them by true digital gates, is now emerging as a promising alternative. This last approach, which challenges the idea that "analog circuits will be always needed", is presented in this tutorial starting from the theoretical background to its application in digital-based operational amplifiers, voltage references, oscillators and data converters integrated on silicon which have proposed in recent literature.

The applicability of the concepts to the design of ICs which are natively portable across technology nodes and highly reconfigurable, thus enabling dynamic energy-quality scaling, as well as a low design effort and a fast time-to-market will be described.

Innovation Theme: Internet of Things

1. Motivation and Focus

Analog cells in integrated circuits do not take advantage of CMOS scaling and are in most cases the bottleneck in terms of power consumption, area, design effort and performance in nanoscale integrated circuits and systems for emerging Internet of Things (IoT) applications.

In view of that, much effort has been done in the last years to design "digital friendly" analog circuits. Based on the results of Claude Shannon's information theory, however, *information* in itself is discrete in nature. This suggests a different approach: i.e. to "translate into digital" the most common analog functions. In this way, traditional analog functions can be implemented by true digital circuits, taking full advantage of scaling in terms of low power consumption, performance, automated design flow, portability across technology nodes and reconfigurability.

This approach, which puts in question the common idea that some analog processing is always needed, at least in interfaces towards the physical world, will be followed and illustrated in this tutorial with reference to common analog or analog-intensive building blocks like operational amplifiers, voltage references and data converters.

In this perspective, the first part of the tutorial will illustrate new concepts which enable the implementation of analog functions by true digital circuits in practical cases. This part of the tutorial is expected to give the audience the basic understanding and methodological tools to apply a similar approach to different analog signal processing applications.

The second part of the tutorial is focused on the implementation on silicon of the new concepts in nanoscale CMOS IC technologies in near threshold and voltage/energy/technology scalability [1]. It

will cover the whole design flow starting from high level logic description (Matlab/Simulink/Verilog-A/Verilog) and then implementation in a digital flow, starting from behavioral logic verification performed by QuestaSim/ModelSim, then, using Design Compiler and finally at transistor level, (Cadence Virtuoso), where the logical functionality and the "analog" performance could be finally tested. The proposed ICs solutions have been validated based on the fabrication of the designed fully synthesizable IC building block.

Tentative syllabus:

First part:

- Theoretical background. Is the physical world really so analog? The information theoretical point of view [2].
- An operational amplifier as a digital circuit: the Digital-Based analog differential circuit [2-4]. Concept and mapping of analog performance into digital design parameters.
- A voltage reference as a digital circuit: the Virtual Voltage Reference concept and design example [5-6].
- New Digital to Analog conversion concepts: the Relaxation DAC [7-8] and the Dyadic Digital Pulse Modulation [9-10].
- Are really analog and digital different things? New perspectives and application scenarios.

Second part:

- Analog – Mixed-Signal design challenges in the IoT era, Fully synthesizable design flow [1]
- Wake-up oscillator: The first pW-range wake-up oscillator for IoT sensor nodes able to operate from 0.3V to 1.8V, avoiding the traditional need of additional power-hungry voltage regulation [11-13] will be presented.
- DACs. The first fully synthesizable Digital-to-Analog Converters (DACs) able to be designed with a fully automated digital design flow. The proposed DACs significantly reduce the design effort compared to conventional analog design as it is based on digital standard cells. Three different versions have been proposed. The first DAC with a nominal resolution of 12-bit exhibits a graceful degradation under voltage/frequency over-scaling [14]; the others are 16-bit and 12-bit versions pointing-out respectively only performance and area reduction [16].
- Analog comparator. An automatized design approach is employed to conceive analog comparison using only standard cells (logic gate) [17].
- ADC: The first (at the best of authors-knowledge) designed and tested. Current-input fully synthesizable Analog-to-Digital Converters (ADCs) will be described [18]. At the tutorial time, even the results of fully synthesizable Voltage-input ADCs architecture will be available for discussion.

References

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[18] O. Aiello, P.Crovetti, A. Sharma, M. Alioto, “Fully Synthesizable Current Input Analog to Digital Converter in 40nm CMOS”, Proc. of IEEE 2019 ICECS - Genova, Italy, 27-29 November 2019.

2. List of speakers:

Paolo S. Crovetti, *Politecnico di Torino*

3. Basic structure of the Tutorial:

The tutorial includes two parts, the first will be given by prof. Crovetti and it will include and introductory part of about 30min and three parts describing the digital-based operational amplifier, virtual voltage reference and Relaxation DAC concepts. The second part will be give by Dr. Aiello and will cover the application of the new concepts in the design flow and physical implementation of integrated circuits for IoT applications. At the end of each part there will be time for questions from the audience and interaction on the application of the approaches illustrated in the tutorial to other applications.

Speaker's Bio:

Paolo Crovetti (S'00-M'04) was born in Turin, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Turin, Turin, Italy, in 2000 and 2003, respectively.He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin, where he teaches courses of Analog Electronics, Automotive Electronics and Circuit Theory. He co-authored more than 50 papers appearing in journals and international conference proceedings. His main research interests are in the fields of analog, mixed-signal, and power integrated circuits. His recent research activities are focused on non-conventional information processing techniques allowing the fully digital implementations of analog functions and on ultra-low-power IC design for Internet of Things (IoT) applications targeted in this Tutorial. In this research area, he first proposed an operational amplifier circuit based only on digital gates (2013), the novel virtual voltage reference technique (2015) and, more recently the Dyadic Digital Pulse Modulation (DDPM, 2017) and the relaxation D/A conversion approach (2019). He is co-author of 12 publications (reference [1-12] above) including journal papers and international conference contributions on this specific research topic. He has been co-recipient of the EMC Kyoto 2009 Excellent Paper award and of the ICECS2019 Best Student Paper Award.

Prof. Crovetti is an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS and a Subject Editor of IET *Electronics Letters* in the area of Circuits and Systems and serves as a regular reviewer for several IEEE journals.