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Relaxation Digital-to-Analog Converter with Foreground Digital Self-Calibration

Paolo S. Crovetti[1], Roberto Rubino[1] and Francesco Musolino[1]
[1]*Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino*, Torino, Italy
{paolo.crovetti, roberto_rubino, francesco.musolino}@polito.it

***Abstract*—A reference-free, fully digital foreground self-calibration strategy intended to automatically tune the clock frequency of Relaxation Digital to Analog Converters (ReDACs), as demanded for linear operation, is presented in this paper. The effectiveness of the proposed approach is demonstrated by computer simulations on a 10-bit, 2MS/s ReDAC designed in 40nm CMOS and operated from a 600mV power supply voltage. After the proposed calibration, the ReDAC is shown to operate near the optimal clock frequency achieving 0.98 LSB maximum INL, 1.00 LSB maximum DNL and 9.06 ENOB.**

***Index Terms*—Relaxation Digital to Analog Converter (ReDAC), Digital to Analog Converter (DAC), Calibration, Internet of Things.**

I. Introduction

Traditional analog circuits are normally not well suited to ultra-low power, ultra-low voltage operation as demanded in low cost analog interfaces for the Internet of Things (IoT) and mostly digital solutions and IC design approaches have been the subject of an extensive research activity over the last years [1]–[3].

In this context, Relaxation Digital to Analog Converters (ReDACs), which exploit the impulse response of an RC network as a mean to generate binary weighted voltages and sum them up according to the digital input, have been recently proposed in [4], [5] as an alternative to weighted capacitors arrays [6], [7], sigma-delta ($\Sigma\Delta$) DACs [8] and dyadic DACs [9]–[11] to address the challenges of ultra-low power, ultra-low voltage digital to analog (D/A) conversion in low cost interfaces for IoT applications.

The operation and the linearity of a ReDAC, however, are strongly related to the clock period, which should be ideally equal to $T^\star = RC\log 2$, being RC the time constant of the first-order RC circuit on which the ReDAC is based. While the possibility to calibrate the ReDAC clock by foreground calibration starting from a high-frequency clock and using a reference voltage, has been suggested in [4], a novel, reference-free self-calibration technique, which does not require any high frequency clock and is compatible to low cost integration in CMOS processes by a fully digital flow is proposed in this paper and demonstrated by computer simulation on a ReDAC in 40nm CMOS.

The paper has the following structure: the principles and main features of ReDACs are revised in Sect.II. Then, in Sect.III, the proposed calibration procedure is described. In Sect.IV, the effectiveness of the calibration strategy and the performance of a calibrated ReDAC are discussed based on simulations. Finally, in Sect.V, some conclusions are drawn.

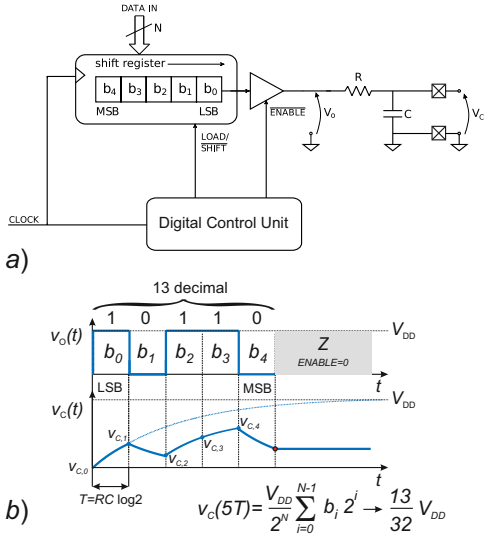


Fig. 1. Relaxation DAC operation principle.

II. Relaxation Digital-to-Analog Conversion Concept and Features

A. Relaxation DAC Operation Principle

A ReDAC converts a digital input n on N bits, expressed in terms of its binary representation $b_{N-1}\dots b_0$ as:

$$n = \sum_{i=0}^{N-1} b_i 2^i, \tag{1}$$

by exploiting a first-order RC network connected to a three-state digital buffer, as discussed in [4] and revised in what follows with reference to Fig.1. Here, the digital buffer is driven by an N-bit shift register loaded by the input n so that, when the buffer is enabled, it drives the RC network by a sequence of N rectangular pulses having duration T and amplitude $V_{\rm DD}b_i$, equal to $V_{\rm DD}$ or 0V, depending on the logical value of b_i, starting from the least significant bit (LSB) b_0 up to the most significant bit (MSB) b_{N-1}.

The evolution of the capacitor voltage $v_{\rm C}(t)$ during the $i^{\rm th}$ time interval $[(i-1)T, iT]$ can be expressed in terms of the capacitor voltage at the beginning of the same interval, i.e. $v_{{\rm C},i-1} = v_{\rm C}(t)|_{t=(i-1)T}$, of the steady-state voltage $v_{{\rm C},i}(\infty)$,

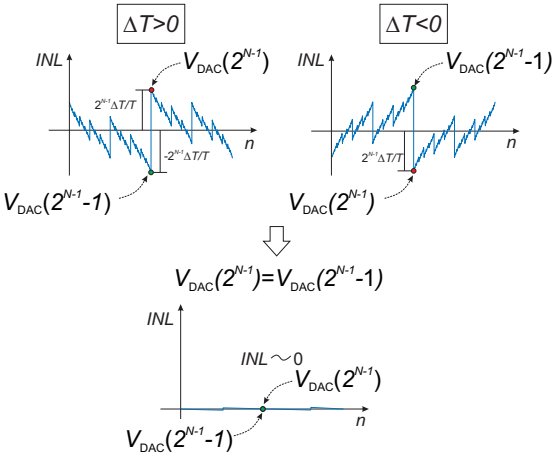


Fig. 2. Relation between integral nonlinearity error (INL) and clock period ΔT and its applicability for clock self-calibration.

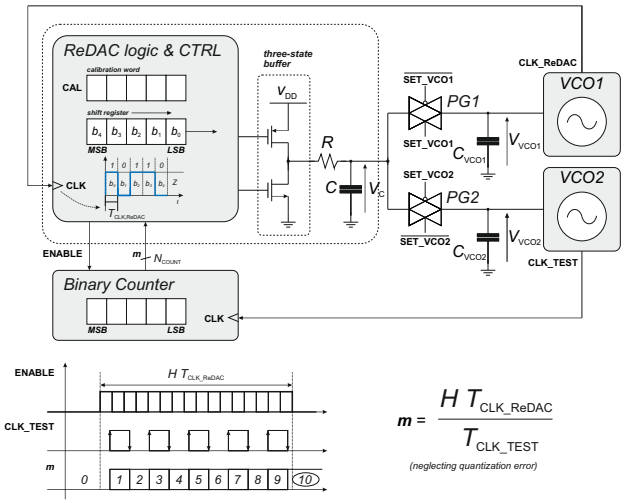


Fig. 3. ReDAC clock frequency self-calibration circuit architecture.

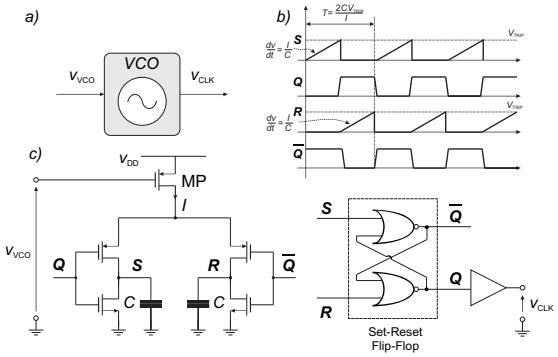


Fig. 4. Voltage controlled oscillator employed in the self-calibration circuit.

which is $V_{\rm DD}$ for $b_i = 1$ and 0V for $b_i = 0$, and of the time constant $\tau = RC$, as

$$v_{\rm C}(t) = v_{{\rm C},i}(\infty)\left[1 - {\rm e}^{-\frac{t-(i-1)T}{\tau}}\right] + v_{{\rm C},i-1}{\rm e}^{-\frac{t-(i-1)T}{\tau}}. \quad (2)$$

Assuming $v_{{\rm C},0} = v_{\rm C}(0) = 0$ as a reset condition, (2) can be iterated to express $v_{{\rm C},i}$ for $i = 1 \ldots N-1$ as a function of $V_{\rm DD}$, b_i and τ and the capacitor voltage after N clock periods can be finally expressed as:

$$v_{\rm C}(NT) = V_{DD}\left(1 - {\rm e}^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{N-1} b_i {\rm e}^{-\frac{(N-i-1)T}{\tau}}. \quad (3)$$

Based on (3), if T is chosen so that:

$${\rm e}^{-\frac{T}{\tau}} = \frac{1}{2} \qquad \Longrightarrow \qquad T = T^\star = \tau \log 2 \quad (4)$$

by substituting condition (4) in (3)

$$V_{\rm DAC}(n) = v_{\rm C}(NT) = \frac{V_{\rm DD}}{2^N} \cdot \sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N} V_{\rm DD}, \quad (5)$$

i.e., $V_{\rm DAC}(n)$ is proportional to the binary input value n expressed by (1), as demanded for D/A conversion. Finally, the capacitor voltage $V_{\rm DAC}(n)$ is held constant by releasing the enable signal of the three-state buffer.

B. Impact of Clock Period Errors on ReDAC Linearity

Based on (4), the linearity of a ReDAC does not rely on matching and it depends on the single process-sensitive quantity T/τ. This feature of ReDACs, not found in other DACs like current steering and weighted capacitors DACs [6]–[8], makes it possible to ideally achieve perfect linearity over the full ReDAC input range by single-point calibration, i.e. by tuning the ReDAC clock period T to enforce the correct output voltage for a single input code.

Moreover, if condition (4) is not exactly met, a deviation $\Delta T = T - T^\star$ of the clock period from the ideal value leads to a ReDAC nonlinearity error which is maximum in magnitude and opposite in sign for $n = 2^{N-1} - 1$ and $n = 2^{N-1}$ as observed in Fig.2. By Taylor series expansion of (2), in particular, it can be observed that the worst case integral nonlinearity error (INL) in LSB is about

$${\rm INL}_{\rm max} \simeq \quad 2^{N-1}\log 2 \cdot \frac{\Delta T}{T}. \quad (6)$$

From (6), in particular, a positive systematic error ΔT leads to $V_{\rm DAC}(2^{N-1}) > V_{\rm DAC}(2^{N-1}-1) + 1{\rm LSB}$ while the opposite occurs for a negative ΔT error, as shown in Fig.2. The above relation between ΔT and ${\rm INL}_{\rm max}$ will be leveraged in what follows to calibrate the ReDAC without requiring any external reference voltage, just tuning T so that to enforce the condition $V_{\rm DAC}(2^{N-1}) = V_{\rm DAC}(2^{N-1}-1)$.

III. Proposed ReDAC self-calibration

An automatic calibration strategy is proposed in this paper to automatically enforce the relation between the time constant $\tau = RC$ and the shift register clock period T expressed in (4). The proposed approach takes advantage of the relation between the clock period error $\Delta T = T - T^\star$ and the difference in the ReDAC output voltages at input codes $2^{N-1} - 1$ and 2^{N-1}, i.e.

$$\Delta V_{\rm DAC} = V_{\rm DAC}(2^{N-1}) - V_{\rm DAC}(2^{N-1} - 1), \quad (7)$$

which, considering (6), can be expressed as

$$\Delta V_{\mathrm{DAC}} = 1\mathrm{LSB} \cdot \left(1 + 2^N \log 2 \frac{\Delta T}{T}\right) \tag{8}$$

and is highlighted in Fig.2.

Based on (8), if the clock period T is tuned so that

$$V_{\mathrm{DAC}}(2^{N-1}) = V_{\mathrm{DAC}}(2^{N-1} - 1) \rightarrow \Delta V_{\mathrm{DAC}} = 0 \tag{9}$$

the maximum INL of the converter is found to be exactly 1LSB at the ReDAC resolution adopted in the calibration phase. It follows that, by enforcing condition (9) at a resolution higher than the target resolution of the converter (e.g. with E more bits), the final INL error at the nominal ReDAC resolution can be ideally made arbitrarily small (i.e. 2^{-E} LSBs).

A. Self Calibration Circuit Architecture

Based on the above property of ReDACs, the circuit architecture in Fig.3 is proposed in this paper to tune the clock frequency of the ReDAC enforcing condition (9) at N bit resolution. Here, the ReDAC clock is provided by the voltage controlled oscillator VCO1, whose control voltage $V_{\mathrm{VCO},1}$ is stored in $C_{\mathrm{VCO},1}$, which can be connected to the ReDAC output capacitor C by a pass gate as depicted in the figure. A second VCO, indicated as VCO2 in the figure, whose control voltage $V_{\mathrm{VCO},2}$ can be also driven by the ReDAC output through a pass gate, drives a binary counter and is used as a VCO-based analog to digital converter [12], [13].

The VCOs are based on the topology in Fig.4, widely adopted in recent relaxation oscillators [14]–[16], in which the output period is $T = 2\frac{CV_{\mathrm{TRIP}}}{I}$, being C the capacitance of the capacitors in Fig.4, V_{TRIP} the logic threshold of the Set-Reset latch, and I the drain current controlled by the gate voltage of MP.

The circuit is completed by a digital controller (finite state machine), which drives the calibration network so that to enforce condition (9) by negative feedback, following the procedure illustrated by the flow chart in Fig.5 and explained in what follows.

B. ReDAC Calibration Procedure

During the first calibration step, the ReDAC is operated at a frequency dictated by the capacitor voltage $V_{\mathrm{VCO},1}$ set at the previous step ($V_{\mathrm{VCO},1} = 0\mathrm{V}$ at startup corresponds to the maximum VCO frequency) and converts an internal digital calibration word CAL on N bits into a voltage V_{cal}, which is then applied to $C_{\mathrm{VCO},1}$ by enabling the first pass gate PG1, thus effectively updating the ReDAC clock frequency $f_{\mathrm{CLK_ReDAC}}$ based on CAL.

In the second step, the binary code 2^{N-1} is converted by the ReDAC so that to get the analog voltage $V_{\mathrm{DAC}}(2^{N-1})$, which is then applied as the control voltage $V_{\mathrm{VCO},2}$ of VCO2 by enabling the pass gate PG2. After the conversion, the binary counter is then reset and enabled for a time interval $H \cdot T_{\mathrm{CLK_ReDAC}}$ (i.e. an integer multiple of the VCO1 period) so that to count the clock transitions (both rising and falling) of the VCO2 output at frequency $f_{\mathrm{CLK_TEST}}$ related to

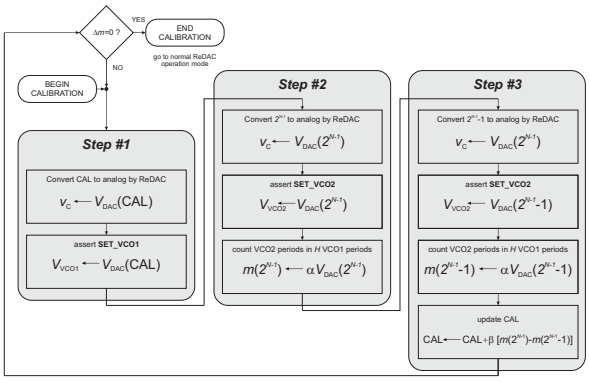


Fig. 5. Flow chart of the proposed Relaxation DAC self-calibration algorithm.

$V_{\mathrm{VCO},2} = V_{\mathrm{DAC}}(2^{N-1})$. The content of the counter m at the end of the enabling period can be therefore written as

$$m(2^{N-1}) = \frac{2H f_{\mathrm{CLK_TEST}}(2^{N-1})}{f_{\mathrm{CLK_ReDAC}}} \simeq \alpha V_{\mathrm{DAC}}(2^{N-1}) \tag{10}$$

and, neglecting quantization error, it is fairly proportional to $V_{\mathrm{DAC}}(2^{N-1})$ with

$$\alpha = \frac{2H \cdot k_{\mathrm{VCO},2}}{f_{\mathrm{CLK_ReDAC}}}$$

and $k_{\mathrm{VCO},2}$ is the VCO gain. In other words, $m(2^{N-1})$ can be regarded as the result of the re-conversion into digital of $V_{\mathrm{DAC}}(2^{N-1})$ by a VCO-based ADC made up of VCO2 and of the counter.

In the third calibration step, the binary code $2^{N-1} - 1$ is applied to the ReDAC operated at the same $f_{\mathrm{CLK,ReDAC}}$ frequency as before, so that to get the converted voltage $V_{\mathrm{DAC}}(2^{N-1} - 1)$ and the same operations described for the second calibration step are repeated, so that the content of the counter at the end of the third step, corresponding to $V_{\mathrm{DAC}}(2^{N-1}-1)$ re-converted into digital in analogy with (10), is:

$$m(2^{N-1} - 1) \simeq \alpha V_{\mathrm{DAC}}(2^{N-1} - 1).$$

As a consequence, the difference Δm in the final value of the counter m at the end on the second and of the third step

$$\Delta m = m(2^{N-1}) - m(2^{N-1} - 1) \simeq \alpha \Delta V_{\mathrm{DAC}}, \tag{11}$$

is proportional to ΔV_{DAC} and related to ΔT by (8). This relation is not affected by additive errors in the VCO-based ADC and by charge injection in PG2. It follows that Δm can be taken as an error signal to correct the calibration word CAL converted in the first calibration step as:

$$\mathrm{CAL}^{\mathrm{new}} = \mathrm{CAL}^{\mathrm{old}} - \beta \cdot \Delta m \cdot \tag{12}$$

where β is a convenient negative feedback gain coefficient, so that to reduce ΔV_{DAC} in magnitude, thus approaching the $\Delta V_{\mathrm{DAC}} = 0$ condition which needs to be enforced to get $\Delta T \simeq 0$ as observed in Fig.2. It is worth being observed that, when $\Delta V_{\mathrm{DAC}} \simeq 0$, VCO2 operates nearly with the same control voltage in the second and in the third step so that Δm

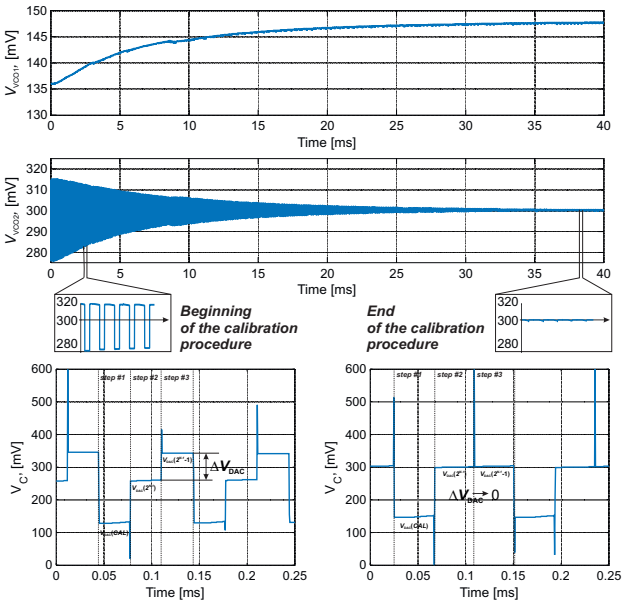


Fig. 6. Simulated VCO1 and VCO2 control voltages V_{VCO1} and V_{VCO2} and ReDAC capacitor voltage V_{C} during the proposed calibration procedure.

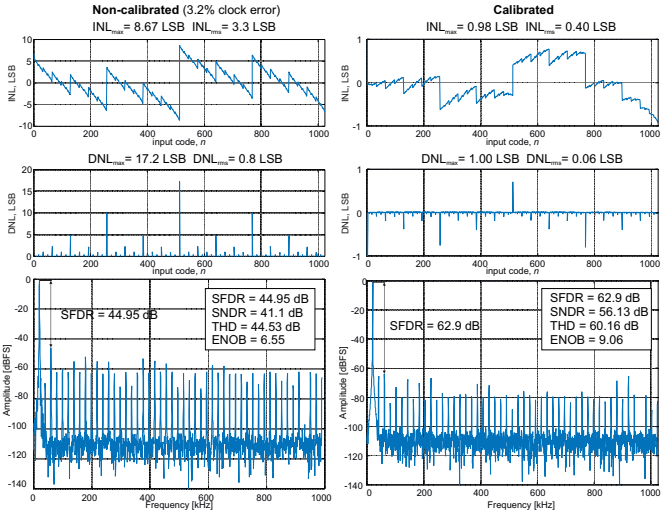


Fig. 7. Simulated static and dynamic performance after the proposed self-calibration procedure

is not affected by the nonlinearity in the voltage-frequency characteristic of VCO2.

The three-step calibration procedure is then repeated with the updated calibration word until $\Delta m = 0$, which corresponds to $\Delta V_{\mathrm{DAC}} = 0$ within the calibration resolution. When this condition is met, the self calibration procedure is completed and the ReDAC can be operated at nominal resolution using the clock signal generated by VCO1 according to the last calibration word.

IV. Simulation Results

The proposed self-calibration architecture has been tested on the 10-bit, 2MS/s ReDAC in 40nm CMOS operated at 0.6V power supply presented in [5]. This ReDAC includes a resistor $R = 128\mathrm{k}\Omega$ and a capacitor $C = 450\mathrm{fF}$ and requires a clock period $T^{\star} = RC\log 2 = 40\mathrm{ns}$ for proper operation. The architecture in Fig.3 is simulated describing the ReDAC core, the pass gates and the VCOs at transistor level and including a Verilog-A model of the counter and the control logic.

In Fig.6, the time-domain waveforms of the VCO1 and VCO2 control voltages during the ReDAC calibration are reported. It can be observed that V_{VCO1}, converges to 147.8mV which corresponds to a VCO1 output period $T = 40.8\mathrm{ns}$. Moreover, the fluctuations in the V_{VCO2} control voltage, which correspond to ΔV_{DAC}, are decreasing through the calibration phase and reach $200\mu\mathrm{V}$ at the end of the process. This is confirmed by the ReDAC output voltage V_{C} waveforms reported at the beginning and at the end of calibration, where it can be observed that the ReDAC output voltages at the second and third calibration steps, i.e. $V_{\mathrm{DAC}}(2^{N-1})$ and $V_{\mathrm{DAC}}(2^{N-1}-1)$, converge to the same value.

In order to verify the calibrated ReDAC operation, the converter has been characterized with the clock signal generated by VCO1 at the end of the calibration procedure and compared with the performance of an uncalibrated ReDAC with 3.2% error in the clock frequency. The static INL and DNL errors with and without the proposed calibration procedure are reported in Fig.7 and reveal a maximum (rms) INL of 0.98 (0.40) LSB and a maximum (rms) DNL 1.00 (0.06) for the calibrated ReDAC, compared to a maximum (rms) INL of 8.67 (3.30) LSB and a maximum (rms) DNL 17.2 (0.8) of the uncalibrated ReDAC. In the same figure, the ReDAC has been characterized with a sine wave input with amplitude of 90% of the input swing and with frequency 20.42kHz, which corresponds to $1/(100T_{\mathrm{conv}})$, being $T_{\mathrm{conv}} = (N+2)T = 490\mathrm{ns}$ the sampling period. The output spectrum of the calibrated ReDAC reveals an SFDR of 62.9dB, a THD of 60.16dB and a SNDR of 56.13dB, yielding to 9.06 effective bits (ENOB), compared to an SFDR of 44.95dB, a THD of 44.53dB and a SNDR of 41.1dB of the uncalibrated ReDAC, corresponding 6.55 effective bits (ENOB).

Both static and dynamic performance is fully comparable (0.34 less ENOB) with the ReDAC at the same sample rate presented in [5], where condition (4) is manually enforced to the ideal value, and demonstrates the effectiveness of the proposed calibration.

V. Conclusions

A digital self-calibration technique intended to automatically tune the clock frequency of a ReDAC, as demanded for linear operation, has been presented. The effectiveness of the proposed approach is demonstrated by computer simulations on a 10-bit, 2MS/s ReDAC in 40nm CMOS operated from a 600mV power supply voltage. After the proposed calibration, the ReDAC is shown to achieve a maximum INL of 0.98 LSB, a maximum DNL of 1.00 LSB and 9.06 ENOB. The proposed technique does not require a reference voltage nor a high frequency clock and is therefore well suited to low power, low cost IoT applications.

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