Optimal Design of Grid-Side LCL Filters for Electric Vehicle Ultra-Fast Battery Chargers

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***Abstract*—This paper proposes a complete design procedure for LCL filters intended for electric vehicle (EV) ultra-fast battery chargers. The basic modeling of LCL filters is reported and the optimal ratio between grid-side and converter-side inductance is discussed. The design methodology is based on the identification of all parameter constraints, which allow to graphically determine the filter design space. Once the available space is identified, the feasible design which minimizes the total required inductance is selected, since inductors dominate the overall LCL filter volume, loss and cost. The proposed design procedure is directly applied to a 50 kW, 20 kHz 3-level unidirectional rectifier for a modular EV ultra-fast charger. The performances of the selected design, in terms of harmonic filtering and current control dynamics, are verified by means of simulation in PLECS environment, proving the validity of the proposed design methodology.**

***Index Terms*—LCL filters, active front-end (AFE), power factor corrector (PFC), battery chargers, electric vehicles (EV), ultra-fast charging (UFC)**

I. Introduction

To leverage the widespread industrial power electronics knowledge, state of the art DC ultra-fast chargers (UFC) are normally connected to the low voltage grid [1]. The basic structure of off-board and on-board battery chargers is practically the same and usually consists of two power converter stages, schematically represented in Fig. 1. The grid-connected stage is a three-phase AC/DC converter with unity power factor correction (PFC) capabilities, also referred to as active front-end (AFE). The role of this stage is to absorb the desired amount of power from the grid while ensuring a sinusoidal input current shaping (i.e. with low distortion and harmonics). The second stage is a high-frequency DC/DC converter, which must provide battery-side current control and galvanic isolation from the mains.

To comply with grid current harmonic restrictions at the point of common coupling (PCC), such as IEEE 519 [2], the AFE must include an AC-side filter capable of attenuating the unwanted switching harmonics deriving from pulse-width modulation (PWM), as highlighted in Fig. 1. The filter can play a major role in achieving the performance targets of the converter (i.e. efficiency, power density), therefore it is the subject of the present work.

A purely inductive L filter is the most simple configuration to provide grid harmonic current attenuation. However, despite its simplicity, a filter of this kind would require large-size inductors, resulting in excessive volume, weight and power loss [3].

Substantial advantages are achieved with an LCL filter, due to its superior attenuation capability (i.e. up to 60 dB/dec), which allows a drastic filter size and loss reduction [3]. Decreasing the total inductance leads to lower cost and possibly higher converter dynamic performance, if the filter and/or the control loop are properly designed. The higher filter order, however, complicates the design procedure, as the available degrees of freedom are increased and several constraints of different nature must be enforced. Moreover, the inherent filter resonance may amplify some unwanted harmonics and it can have a negative impact on the closed-loop current control phase and gain margins, possibly leading to instability [3]–[5]. For these reasons, the resonance peak must be mitigated either by passive or active damping methods [6], [7], which add further complexity to the filter design.

In modern high-frequency power converters the LCL filter can be considered as the first element of a multi-stage differential-mode EMI filter, since it can provide attenuation for the current harmonics lying in the lower part of the 0.15-30 MHz CISPR range, i.e. with the highest energy content. Nevertheless, high-frequency EMI filtering is a very complex problem and does not represent the scope of this work, thus it will not be considered in this paper.

As a result of the previous considerations, several design procedures have been proposed in literature [3], [5], [7], [8], most of which search for a suitable design by iterative means. Even though the literature on LCL filters and their applications is extensive and well established, as of the author's best knowledge, a design procedure specifically targeted to high-power battery chargers has not been proposed yet. In particular, since UFCs are typically unidirectional, a

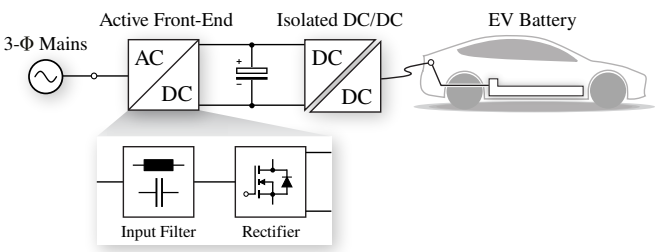

Fig. 1. Ultra-fast EV battery charger schematic overview.

low current ripple at the converter side is required to avoid discontinuous conduction mode and the related low-frequency current distortion. Moreover, the filter capacitance maximum value is strictly constrained, as the converter may be unable to compensate the generated reactive power.

Therefore, the main goal of this work is to provide a complete, non-iterative design procedure for LCL filters, specifically targeting EV ultra-fast battery chargers. This procedure is illustrated in a graphical form, which provides a better understanding of the filter design space, thus simplifying the identification of the optimal design results.

This paper is structured as follows. In Section II the equivalent circuit of the complete system is explained and the most significant LCL filter transfer functions are reported. In Section III the filter parameter restrictions are identified and the proposed design methodology, based on the graphical representation of the filter design constraints, is described. This procedure is applied to a 50 kW, 20 kHz 3-level AFE for EV ultra-fast battery charging and the feasible LCL filter design with lowest total inductance is selected. In Section IV the performance of the designed filter are evaluated: the PCC current distortion and the closed-loop current control stability are verified by means of PLECS simulation. Finally, Section V concludes this paper with a summary of the main results.

II. Filter Model

The equivalent circuit of the complete three-phase active rectifier system is illustrated in Fig. 2. The grid is modeled by three sinusoidal voltage sources u_{abc} in series with an inductive impedance L_{g}, representing the sum of the line inductance and the distribution transformer leakage inductance. The power converter is modeled as a set of voltage sources, dividing the low-frequency voltage contribution $v_{\mathrm{abc,LF}}$ (i.e. at the mains frequency) from the high-frequency contribution $v_{\mathrm{abc,HF}}$ (i.e. switching harmonics). The LCL filter may or may not have a set of damping resistors in series with the filtering capacitors, depending whether passive damping needs to be provided.

Due to its symmetrical properties, the described model can be represented with the single-phase equivalent circuit

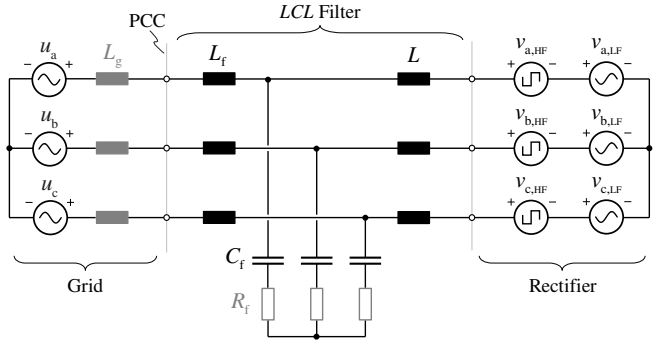

Fig. 2. Three-phase equivalent circuit of the considered system, composed of the active rectifier, the LCL filter and the grid. L is the converter-side boost inductance, C_{f} is the filter capacitance and L_{f} is the grid-side filter inductance. The grid internal inductance L_{g} and the filter damping resistance R_{f} are greyed out, since they are not always present and/or quantitatively meaningful to the analysis.

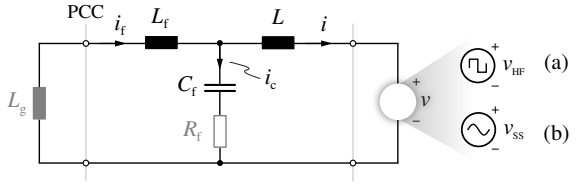

Fig. 3. Single-phase equivalent circuit of the considered system. v_{HF} (a) and v_{SS} (b) represent the high-frequency and small-signal voltages, respectively.

reported in Fig. 3. Both from a high-frequency harmonic perspective (i.e. filter attenuation) and a small-signal stand point (i.e. closed-loop control stability) , the low frequency voltage sources of Fig. 2 appear as short circuits.

Once the system small-signal equivalent circuit has been identified, the most significant filter transfer functions can be directly derived. Referring to the naming conventions of Fig. 3,

$$Y(s) = \frac{i(s)}{v(s)} = \frac{1}{sL}\frac{s^2 + 2\xi_{\mathrm{f}}\omega_{\mathrm{f}}s + \omega_{\mathrm{f}}^2}{s^2 + 2\xi_0\omega_0 s + \omega_0^2}, \tag{1}$$

$$Y_{\mathrm{f}}(s) = \frac{i_{\mathrm{f}}(s)}{v(s)} = \frac{1}{s(L+L_{\mathrm{f}}+L_{\mathrm{g}})}\frac{2\xi_0\omega_0 s + \omega_0^2}{s^2 + 2\xi_0\omega_0 s + \omega_0^2}, \tag{2}$$

are obtained, where

$$\begin{cases} \xi_{\mathrm{f}} = \dfrac{\omega_{\mathrm{f}} R_{\mathrm{f}} C_{\mathrm{f}}}{2} \\ \omega_{\mathrm{f}}^2 = \dfrac{1}{C_{\mathrm{f}}(L_{\mathrm{f}}+L_{\mathrm{g}})} \end{cases}, \tag{3}$$

$$\begin{cases} \xi_0 = \dfrac{\omega_0 R_{\mathrm{f}} C_{\mathrm{f}}}{2} \\ \omega_0^2 = \dfrac{L+L_{\mathrm{f}}+L_{\mathrm{g}}}{C_{\mathrm{f}} L (L_{\mathrm{f}}+L_{\mathrm{g}})} \end{cases}. \tag{4}$$

$Y(s)$ plays a key role in the converter closed-loop current control, since it links the voltage applied by the converter to the generated (and controlled) current. $Y_{\mathrm{f}}(s)$ is the actual filter admittance, as it relates the high-frequency voltage source with the current harmonics generated at the system output, i.e. at the PCC. The magnitude Bode plot of $Y(s)$ and $Y_{\mathrm{f}}(s)$ is qualitatively illustrated in Fig.4, where the effect of different damping resistance values is shown.

The ratio between the grid-side and the converter-side inductances $r_{\mathrm{L}} = {}^{L_{\mathrm{f}}+L_{\mathrm{g}}}/_{L}$ provides useful information on the LCL filter performance characteristics. This ratio can be optimized to maximize the filter attenuation for a given total amount of inductance $L_{\mathrm{tot}} = L + L_{\mathrm{f}} + L_{\mathrm{g}}$. Developing the asymptotic expression of the filter admittance,

$$Y_{\mathrm{f}}(s) \overset{s\to\infty}{=} \frac{R_{\mathrm{f}}}{s^2 L_{\mathrm{tot}}^2}\frac{(1+r_{\mathrm{L}})^2}{r_{\mathrm{L}}}, \tag{5}$$

it is found that the minimum filter admittance value, corresponding to the maximum filter attenuation, is obtained for $r_{\mathrm{L}} = 1$, meaning $L = L_{\mathrm{f}} + L_{\mathrm{g}}$. In this condition, for a given attenuation requirement, the total filter inductance is minimized. Since the inductive components largely dominate over filter capacitors, also the filter cost, weight and volume are generally minimized for $r_{\mathrm{L}} = 1$. Moreover, minimum inductance translates in minimum voltage drop under load

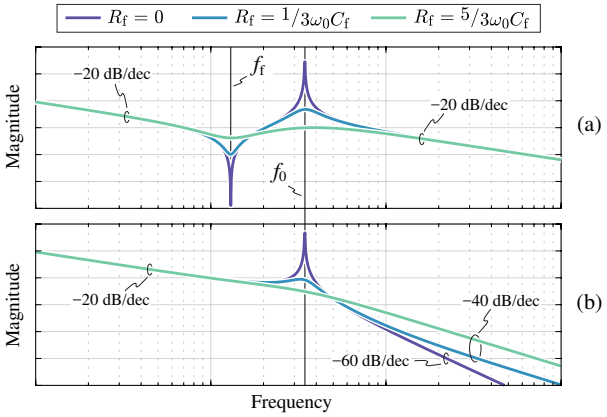

Fig. 4. Qualitative representation in the logarithmic scale of the magnitude of $Y(s)$ (a) and $Y_f(s)$ (b), for different values of damping resistance. The resonance frequencies $f_f = \omega_f/2\pi$ and $f_0 = \omega_0/2\pi$ are highlighted. The asymptotic trends are noted on the curves in dB/dec.

(thus minimizing DC-link voltage and semiconductor switching losses) and higher dynamic performance, i.e. if the control loop is properly designed. Finally, depending on the specific conditions, equal inductance values can translate in equal inductor designs, providing a reasonable cost advantage. Values of r_L higher than unity can yield the only benefit of increasing the control robustness against grid impedance variations [7].

It is well known that the LCL filter resonance may cause the loss of the converter control stability, depending on the filter component values [3]–[5]. In general, an increase in the current control phase and gain margins can be achieved either by reducing the controller bandwidth (if possible) or by adopting active and/or passive damping solutions. Active damping is based on introducing additional feedback mechanisms inside the control loop, to improve its performance and achieve robust stability [7]. On the contrary, passive damping is obtained in a more simple way, by inserting resistors in series with the filter capacitors to directly damp the resonance peak [6], as shown in Fig. 4. Even though passive damping causes a lower filter asymptotic attenuation (i.e. 40 dB/dec) and generates power losses in the resistors, it is usually the preferred solution because of its simple implementation and no need of additional measurements and computational overhead (required for active damping). In general, the required damping cannot be established without knowing the current control loop transfer function. However, when this is the case, a resistance value similar to the impedance of the filter capacitor at the resonance frequency is usually selected, such as $R_f = 1/3\omega_0 C_f$ [8].

It is worth mentioning that the grid inductance L_g is not always known during the filter design phase, as the converter installation location can be undefined. Moreover, the location itself may witness large inductance variations during the day and/or along the year. In general, a weak grid characterized by high inductive impedance and low short-circuit ratios (SCR) can compromise the converter control stability, since the filter resonance frequency f_0 may end up lower than expected and possibly interfere with the controller bandwidth [7]. For this reason, a certain margin must be considered during the converter design and control tuning phases.

III. Design Procedure

In this section, a complete, non-iterative design procedure of an LCL filter for EV ultra-fast battery charging is presented. Sinusoidal quantities are expressed with their peak values in this work.

A. Specifications and Performance Targets

The filter design procedure is applied to a modular UFC connected to the European low-voltage grid (i.e. 50 Hz, 400 V line-to-line), schematically illustrated in Fig. 5. Each AFE module is composed of a 3-level T-type unidirectional rectifier and an LCL filter, both rated at 50 kW nominal active power. Notably, each module must ensure proper filtering at the PCC by itself, since the number of paralleled modules in one installation is not defined a priori. The single converter specifications and nominal operating conditions are reported in Table I.

The scope of the LCL filter is to make the AFE comply with the harmonic emission standards at the PCC prescribed by IEEE 519 [2]. The harmonic limits, reported as a percentage of the nominal current in Table II, are a function of the grid SCR and are more stringent for even-order harmonics (i.e. 25% of the limits for the odd ones). Since the installation of the converter is not predetermined, the worst-case SCR ratio (i.e. < 20) is considered in this work. It is important to mention that, since the converter switching frequency is 20 kHz, all of the generated switching harmonics will be higher than the 35th (i.e. 1750 Hz), therefore 0.3% and 0.075% limits apply to odd and even harmonics respectively. IEEE 519 also defines a maximum current total harmonic distortion (THD), however the stringent harmonic requirements at high frequency generally satisfy the maximum THD constraint by a large margin.

TABLE I. AFE specifications and nominal operating conditions.

Parameter	Description	Value
f	grid frequency	50 Hz
P	nominal active power	50 kW
Q	no-load reactive power	$\leq$ 5 kvar
V	peak phase voltage	325 V
I	peak output phase current	102.5 A
$\cos\varphi$	power factor	$\geq$ 0.995
V_{dc}	DC-link voltage	650 V
f_{sw}	switching frequency	20 kHz

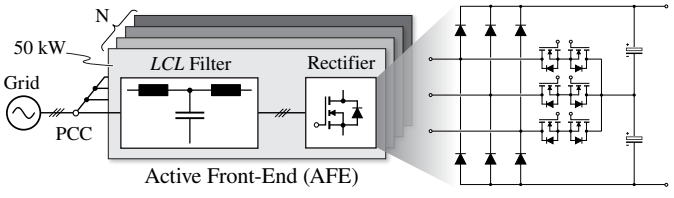

Fig. 5. Schematic overview of the considered modular EV ultra-fast battery charger with highlight of the AFE converter topology. Each one of the N modules is rated at 50 kW nominal active power.

TABLE II. IEEE 519 CURRENT HARMONIC LIMITS FOR DISTRIBUTION SYSTEMS WITH A $0.12-69$ kV NOMINAL OPERATING VOLTAGE [2].

Maximum odd-harmonic current distortion in percent of I

I_{sc}/I	$h<11$	$11\leq h<17$	$17\leq h<23$	$23\leq h<35$	$35\leq h$
<20	4.0	2.0	1.5	0.6	0.3
$20\dots50$	7.0	3.5	2.5	1.0	0.5
$50\dots100$	10.0	4.5	4.0	1.5	0.7
$100\dots1000$	12.0	5.5	5.0	2.0	1.0
>1000	15.0	7.0	6.0	2.5	1.4

I_{sc}: short-circuit current, I: rated current, h: harmonic number

Even-order harmonics are limited to 25% of the odd-harmonic limits

B. Parameters and Constraints

Due to its high-order structure, the LCL filter has several design degrees of freedom based on the choice of parameters L, L_f, C_f and R_f. It is worth noting that, since L_g is not known a priori, the design procedure neglects this term (i.e. $L_g=0$). For the reasons highlighted in Section II the grid-side to converter-side inductance ratio is fixed to $r_L=1$ (i.e. $L=L_f$), thus removing one degree of freedom. Moreover, passive damping is here considered, to ease the controller implementation: the damping resistance value is fixed to $R_f=1/3\omega_0 C_f$ as in [8]. Therefore, only two degrees of freedom remain, namely the choice of C_f and $L_{tot}=L+L_f=2L$. As a consequence, all design constraints must be expressed as functions of one or both variables.

The following constraints, which are reported in analytical form in Table III, must be satisfied:

① The filter resonance frequency f_0 must be higher than 10 times the grid frequency ($f_{0,min}=10f$), to avoid resonance problems in the lower part of the harmonic spectrum and allow a sufficient current control bandwidth.

② The filter resonance frequency f_0 must be lower than half of the switching frequency ($f_{0,max}=f_{sw}/2$), to avoid unwanted amplification of switching harmonics.

③ The current ripple through the boost inductor L must be below a specified amount to limit inductor losses and, in the present unidirectional case, to avoid excessive discontinuous current mode operation at the waveform zero-crossings, which causes low-frequency harmonic distortion. This limit is set to 20% of the peak nominal current ($\Delta I_{pp,max}=0.2\,I$).

④ The maximum voltage drop under nominal load conditions must be lower than a specified value depending on the high-line grid voltage ($U_{max}=1.1\,U$), the maximum modulation index of the converter ($M_{max}=2/\sqrt{3}$) and the DC-link voltage, resulting in $\Delta V_{max}=\sqrt{V_{dc}^2/3-U_{max}^2}$.

⑤ The maximum no-load reactive power generation is set to 10% of the nominal power ($Q_{max}=0.1\,P$).

⑥ The minimum power factor at a specified minimum load condition ($P_{min}=P/2$) is set to $\cos\varphi_{min}=0.995$, taking into account that the unidirectional rectifier cannot generate or absorb reactive power.

⑦ The minimum filter attenuation $A^*(f_d)$ is set according to IEEE 519 with an additional margin of 50%.

To gather insight into the peak-to-peak boost inductor flux linkage $\Delta\Psi_{pp}$ and the full harmonic spectrum of the converter output voltage, a fast simulation is performed in MATLAB environment. The voltage waveform spectrum is then calculated in post-processing by means of a fast Fourier transform (FFT). Standard space-vector modulation has been considered for the voltage waveform derivation, yielding $\Delta\Psi_{pp}=1.74$ mVs in nominal operating conditions.

To calculate the minimum attenuation needed to comply with IEEE 519, the asymptotic filter behaviour is exploited (i.e. $s\to\infty$), as the LCL resonance frequency f_0 is sufficiently lower than the switching frequency:

$$A(f_h)=\frac{1}{|Y_{f,s\to\infty}(j2\pi f_h)|}=\frac{\pi^2 f_h^2 L_{tot}^2}{R_f}\quad f_h\gg f_0, \tag{6}$$

where A is the filter attenuation, increasing with a 40 dB/dec rate. $A(f_h)$ represents the input-to-output filter impedance at the h-th harmonic, linking the voltage harmonics V_h generated by the converter to the current harmonics I_h at the PCC. The required harmonic attenuation to satisfy IEEE 519, including a safety margin, is easily described in logarithmic scale (dB):

$$A^*_{dB}(f_h)=V_{h,dB}(f_h)-I_{h,limit,dB}(f_h)-\text{margin}_{dB}. \tag{7}$$

TABLE III. LCL FILTER DESIGN CONSTRAINTS IN TERMS OF L_{tot} AND C_f, CONSIDERING $L_g=0$, $L=L_f$ AND $R_f=1/3\omega_0 C_f$.

	Description	Constraint	Analytical Expression
①/②	minimum/maximum resonance frequency	$f_{0,min}\leq f_0\leq f_{0,max}$	$\frac{1}{\pi^2 f_{0,max}^2 L_{tot}}\leq C_f\leq\frac{1}{\pi^2 f_{0,min}^2 L_{tot}}$
③	maximum inductor current ripple	$\Delta I_{pp}\leq\Delta I_{pp,max}$	$L_{tot}\geq 2\frac{\Delta\Psi_{pp}}{\Delta I_{pp,max}}$
④	maximum load voltage drop	$\Delta V\leq\Delta V_{max}$	$L_{tot}\leq\frac{\sqrt{V_{dc}^2/3-U_{max}^2}}{2\pi f I}$
⑤	maximum no-load reactive power generation	$Q\leq Q_{max}$ @ $P=0$	$C_f\leq\frac{Q_{max}}{3\pi f U^2}$
⑥	minimum power factor	$\cos\varphi\geq\cos\varphi_{min}$ @ $P=P_{min}$	$C_f\leq L_{tot}\frac{I_{min}^2}{U^2}+\frac{P_{min}}{3\pi f U^2}\frac{\sqrt{1-\cos^2\varphi_{min}}}{\cos\varphi_{min}}$
⑦	minimum IEEE 519 attenuation	$I_h\leq I_{IEEE,519}(f_h)\ \forall$ h	$C_f\geq\frac{A^{*2}(f_d)}{36\pi^4 f_d^4 L_{tot}^3}$

The design frequency f_d is defined as the harmonic which requires the largest filtering effort to be attenuated:

$$f_\mathrm{d} \iff \max\left[A^*(f_\mathrm{h}) - 40\log_{10}(f_\mathrm{h})\right]. \tag{8}$$

In the present case, the design frequency is of even-order ($f_\mathrm{d} = 19.5$ kHz), requiring an attenuation of $A^*(f_\mathrm{d}) \approx 250\ \Omega$.

C. Results

The proposed design procedure is based on translating the constraints ①–⑦ into boundaries in the filter design space (i.e. the $C_\mathrm{f} L_\mathrm{tot}$ plane). This representation allows to have a clear view of the remaining degrees of freedom for the filter optimization. Many different criteria have been proposed in literature, mostly based on weight, volume or energy minima. In this work, the feasible design with lowest inductance is considered as the best candidate, since the capacitor generally has a small impact on the filter size, weight, loss and cost.

The results of the design procedure are illustrated in Fig. 6. The feasible LCL filter design with minimum total inductance is found at the intersection between boundaries ③ (i.e. maximum converter-side current ripple) and ⑦ (minimum required attenuation for IEEE 519). The parameters of the selected design are reported in Table IV.

To make sure that resistor losses don't have a significant impact on the converter efficiency, they can be calculated by assuming that the high-frequency current ripple Δi_RMS completely flows into the capacitor branch:

$$P_\mathrm{loss} = 3R_\mathrm{f}\left[\Delta i_\mathrm{RMS}^2 + \frac{U_\mathrm{RMS}^2}{[1/(j2\pi f C_\mathrm{f}) + R_\mathrm{f}]^2}\right] \tag{9}$$

In the present case, the total damping losses amount to ≈ 22 W.

TABLE IV. Optimal LCL filter parameter values.

L	L_f	C_f	R_f	f_0
85.0 µH	85.0 µH	24.5 µF	0.44 Ω	4.93 kHz

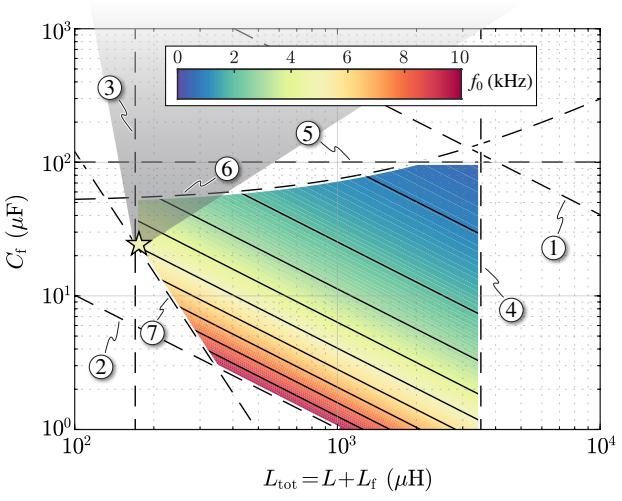

Fig. 6. LCL filter design space in the $C_\mathrm{f} L_\mathrm{tot}$ logarithmic plane. Constraints ①–⑦ bound the feasible design region. The design with minimum total inductance is selected.

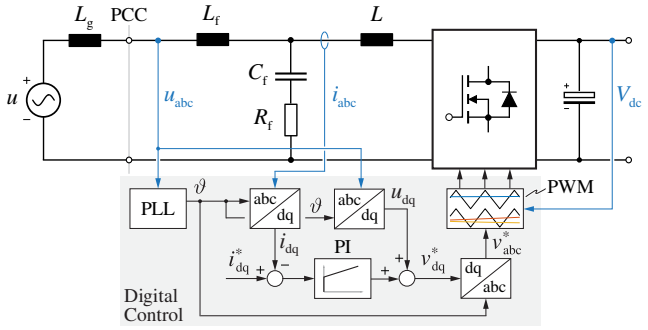

Fig. 7. Simplified schematic of the implemented system simulation: the adopted closed-loop current control in the dq frame is highlighted in grey.

IV. Simulation Verification

A complete system simulation in PLECS environment is implemented in this section, including the grid, the filter, the 3-level T-type rectifier and a digital closed-loop current control (see Fig. 7). The output harmonic attenuation and the controller performance obtained with the selected LCL filter design are thus verified.

A. Filter Attenuation

The grid-side and converter-side current waveforms in nominal stationary conditions are illustrated in Fig. 8. A slight distortion in the grid-side current can be seen in proximity of the current zero crossings, as the T-type rectifier briefly enters the discontinuous conduction mode.

The current spectrum is calculated by means of FFT, yielding the results reported in Fig. 9 and a THD of 0.19%. It is shown that all harmonics comply with the IEEE 519 limits: in particular, the worst-case current harmonic at the design frequency f_d is attenuated with a 15% margin. Due to the slight current distortion previously discussed, a small amount of low frequency harmonics appear, nevertheless they are limited by the current control loop.

B. Control Stability and Dynamic Response

The standard voltage-oriented control scheme illustrated in Fig. 7 is here adopted [3]–[5]. The rotating dq frame is exploited to obtain zero stationary error with a simple PI controller. The PCC voltages are measured to achieve the reference frame synchronization with the grid, which is performed by a PLL [3]. These voltages are also fed forward in the current control loop, to unburden the integral part of

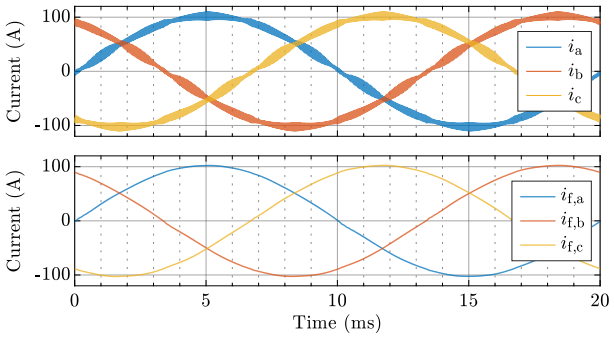

Fig. 8. Converter-side (top) and grid-side (bottom) current waveforms.

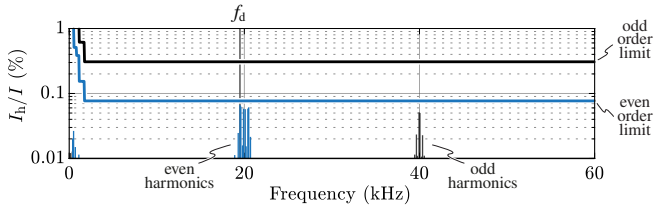

Fig. 9. Filtered grid current spectrum compared with IEEE 519 odd-order and even-order harmonic limits.

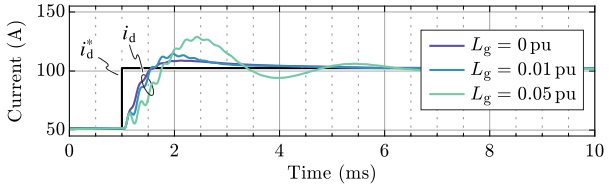

Fig. 11. d-axis current control loop step response between 50% and 100% load for different values of grid inductance.

the PI regulator. The digital sampling and update is performed once per switching period (i.e. at 20 kHz), clearing the current measurement from the switching ripple.

Two main delay components are introduced by the digital control implementation. The first is directly related to the digital processing, which introduces a one sampling period delay (T_s) between the measured quantities and the control signal output. The second is linked to the PWM modulator, which introduces a zero-order hold (ZOH) effect. The expressions of both transfer functions are reported in Fig. 10.

Since the LCL filter transfer function $Y(s)$ behaves as a pure inductance (L_{tot}) up until the first resonance f_f (see Fig. 4), the current control tuning may be carried out in a standard way. The PI regulator is tuned to obtain a 500 Hz bandwidth (f_b), while setting the PI zero five times lower ($f_z = f_b/5$) to achieve good disturbance rejection capabilities:

$$\begin{cases} k_P = 2\pi f_b L_{tot} \\ k_I = 2\pi f_z k_P \end{cases} \tag{10}$$

The current control block diagram is illustrated in Fig. 10, together with the open-loop Bode plots for different values of grid inductance L_g. In general, for the closed-loop current control to be stable, its open-loop transfer function magnitude must be lower than 0 dB when its phase crosses $-180°$ (Nyquist criterion). It can be observed that the system gain margin decreases for higher values of L_g (i.e. lower SCR), reaching the stability limit for $L_g = 0.05$ pu (SCR $= 20$). Furthermore, a larger L_g reduces the converter bandwidth meanwhile reducing the distance between f_b and f_z, thus decreasing also the phase margin.

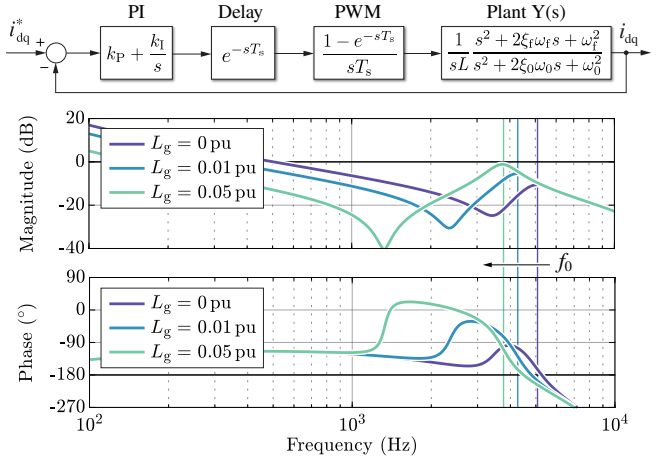

Fig. 10. Current control transfer function block diagram (top) and open-loop Bode plots for different values of grid inductance (bottom).

Another way to look at the results is by analysing the converter load step response, illustrated in Fig. 11. It is observed that the control loop is stable in all conditions, however larger grid inductance values cause at the same time a slower response (i.e. lower bandwidth), a higher overshoot (i.e. lower phase margin) and an increased high-frequency oscillation (i.e. lower gain margin at the phase crossover frequency).

It is worth mentioning that this model neglects the high-frequency resistance of the LCL filter inductors deriving from skin, proximity and core losses, which may be considerable at the resonance frequency (i.e. ≈ 5 kHz). In experimental practice, this resistance greatly helps in damping the filter resonance peak, increasing the controller stability and allowing higher bandwidth. Furthermore, an enhancement of the controller performance may be obtained with the adoption of a lead-lag network [3], [4]. However, this increases the controller complexity and has not been considered in the present work.

It can be concluded that stability is achieved for all grid SCR values up to 20, nevertheless the control performance decreases as the grid connection becomes weaker.

V. Conclusion

This work has presented an LCL filter design methodology based on the graphical representation of the parameter constraints on the $C_f L_{tot}$ plane. This procedure has been applied to a 50 kW, 20 kHz T-type unidirectional rectifier for UFC applications and the feasible design with lowest total inductance has been selected. Finally, this design has been tested in PLECS environment, verifying both the harmonic attenuation requirements and the closed-loop current control stability, thus validating the proposed design methodology.

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