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Massimo Ortolano[1, 2], Martina Marzano[2], Vincenzo D'Elia[2], Ngoc Thanh Mai Tran[2, 1], Ryszard Rybski[3], Janusz Kaczmarek[3], Mirosław Kozioł[3], Krzysztof Musioł[4], Andreas Christensen[5], Andrei Pokatilov[6], Luca Callegaro[2], Jan Kučera[7] and Oliver Power[8]

[1]Politecnico di Torino, Turin, Italy
massimo.ortolano@polito.it
[2]Istituto Nazionale di Ricerca Metrologica, Turin, Italy
[3]University of Zielona Góra, Zielona Góra, Poland
[4] Silesian University of Technology, Gliwice, Poland
[5]Trescal A/S, Silkeborg, Denmark
[6]AS Metrosert, Tallinn, Estonia
[7]Czech Metrology Institute, Prague, Czech Republic
[8]National Standards Authority of Ireland, Dublin, Ireland

***Abstract*—We present here a comprehensive analysis of the error sources in electronic fully-digital impedance bridges, for both sourcing and digitizing bridges. This work can be used as a basis to optimize the design and the operating parameters of digital bridges, and in the evaluation of the uncertainty.**

***Index Terms*—Impedance measurement, bridge circuits, measurement errors, measurement uncertainty, calibration**

I. Introduction

In recent years, electronic fully-digital impedance bridges based on polyphase digital signal sources have emerged as devices suitable for primary impedance metrology [1], [2]. With typical accuracies in the 10^{-6}–10^{-5} range, these kinds of bridges are not as accurate as traditional transformer-ratio bridges, but can measure impedances across the whole complex plane and are characterized by affordable cost, short measuring time and ease of operation. These features make them of interest for calibration laboratories.

We present here a comprehensive analysis of the error sources in electronic fully-digital bridges for two standard architectures: *sourcing* (*DAC-based*) bridges, where an impedance ratio is compared to a reference ratio determined from the settings of a digital signal source; and *digitizing* (*sampling* or *ADC-based*) bridges, where an impedance ratio is compared to a ratio determined from digitized samples.

II. Sourcing bridges

For the purpose of analyzing error sources, common four-terminal-pair fully-digital impedance bridges can be reduced to the basic schematic of Fig. 1 on the next page, where the network of a sourcing bridge is represented by black and red lines. Relevant quantities and symbols are defined therein.

For the balanced bridge, the impedance ratio is given by

$$W = \frac{Z_1}{Z_2} = -\frac{E_1}{E_2}. \tag{1}$$

In a sourcing bridge, the readings E_1^{read} and E_2^{read} of the voltage phasors E_1 and E_2 are computed from the samples used to synthesize the two waveforms. Due to the source non-idealities, the actual voltage phasors differ from the readings, $E_k = [1 + g_k(E_k^{\mathrm{read}})]E_k^{\mathrm{read}}$, $k = 1, 2$, with $g_k(E_k^{\mathrm{read}})$ representing a possibly voltage-dependent complex gain error that accounts for nonlinear magnitude and phase errors. This error can be partially compensated by performing two measurements (*channel swapping*), one with E_1 and E_2 connected as in Fig. 1 (F configuration) and one with the two channels exchanged (R configuration), and by computing the reading $W^{\mathrm{read}} = \sqrt{E_{1\mathrm{F}}^{\mathrm{read}} E_{2\mathrm{R}}^{\mathrm{read}} / (E_{2\mathrm{F}}^{\mathrm{read}} E_{1\mathrm{R}}^{\mathrm{read}})}$.

The impedance ratio W differs from W^{read} by the error $\Delta W = W^{\mathrm{read}} - W$. The main components of this error are: i) the *source nonlinearity*, that is, the dependence of the gain errors g_k from the generated voltages, $g_k = g_k(E_k^{\mathrm{read}})$; ii) the *source crosstalk*, that is, the interference of one source channel onto another, $E_j = E_j^{\mathrm{read}} + \sum_{k \neq j} a_{jk} E_k^{\mathrm{read}}$; iii) the *bridge unbalance*, that is, the deviations of V_{L1}, V_{L2}, V_{H1} and V_{H2} from zero; and iv) the *source loading*, that is, the fact that E_1 and E_2 have to energize the stray admittances Y_{H1} and Y_{H2} through the source output impedance z. Tab. I reports, for each error component, the error equation $\Delta W / W^{\mathrm{read}}$ which results from the analysis of the circuit of Fig. 1, by considering channel swapping. In four-terminal-pair sourcing bridges, the source loading effect is typically negligible, for the mismatch $Y_{\mathrm{H1}} - Y_{\mathrm{H2}}$ is usually small compared to z^{-1}.

III. Digitizing bridges

The network of a digitizing bridge is represented in Fig. 1 by black and blue lines. The impedance ratio is given by (1). In a digitizing bridge, the readings E_1^{read} and E_2^{read} of the voltage phasors E_1 and E_2 are computed from the digitized samples. The digitizer is based on an analog-to-digital converter (ADC) which reads the voltages at the high- and low-potential ports of the impedances Z_1 and Z_2 (the detector D and the digitizer V can be then the same device).

Equations similar to those reported in Tab. I can be derived also for the error sources of a digitizing bridge, just by