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PROCEEDINGS OF SCIENCE

A multi-channel trigger and acquisition board for TDC-based readout: application to the cosmic rays detector of the PolarQuEEEst 2018 project.

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In the summer of 2018, the PolarQuEEEst experiment accomplished a measurement of cosmic rays flux in the Arctic. The detector, installed on a sailboat, was based on scintillation tiles read by a total of 16 SiPM. A multi-channel board (called TRB) has been designed to process the discriminated SiPM signals providing both self-trigger capability and time-to-digital conversion; it was based on a Cyclone-V Intel FPGA. Time-to-digital conversion has been implemented both into FPGA and with the HPTDC chip (as a backup). In this document the board will be described, enlightening the main features and the achieved performance. Lastly, the PolarQuEEEst measurement campaigns will be briefly described, showing how the TRB board has proved to be effective for experiments which require low power consumption, integration with position and environmental sensors and great portability as well. Final thoughts on future improvements will be also discussed.

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1. Introduction

During the summer of 2018 the Nanuq sailboat circumnavigated the Svalbard archipelago in memory of the 1928 crash of the Italian airship ITALIA of U. Nobile [1]. This mission hosted also few scientific programs and in particular the experiment PolarquEEEst to measure the flux of cosmic rays at latitudes from 62°N to 82°N degrees, where there are scarse measurements [2]. The experiment was conceived and performed within the Extreme Energy Events project of Centro Fermi in Rome [3]. The detector was based on scintillation tiles read by a total of 16 SiPM, each of them were digitized by applying discrimination over a programmable thresholds. Signals were sent, as LVDS standard, to a FPGA-based custom board called TRB, which had self-triggering capabilities, provided time-to-digital conversion of the SiPM signals, gathered precise timing and position information from a GPS navigation system, packed event data and sent them to a commercial Raspberry PI 3[1] single board computer, aimed to data recording. The Electronics Design Service of the INFN Bologna Division has designed both the whole TRB board hardware and a fully-functional firmware. The project had to fulfil two severe limitations: The whole system should have a maximum power consumption of 15 W (due to restriction of available supply on the boat) and the size of both the detector and the electronics had to be kept within boundaries of a dedicated box inserted inside a specially designed hatch, just above the sleeping berth. Beside, due to the tightness of the production schedule and because it was the first project where we planned to implement time-to-digital conversion into FPGA, in order to mitigate risks, we decided to implement an ad-hoc mezzanine hosting a custom chip called High Performance Time to Digital Converter (HPTC) [4] which had been foreseen as a backup solution.

2. The Trigger and Acquisition board

2.1 Hardware overview

The TRB board is shown in figure 1; in figure 2 the HPDTC mezzanine is plugged over the main FPGA. The main features of the board are:

- 32 differential input channels: 16 connected in parallel to both the FPGA and the HPTDC,16 only to the HPTDC;
- parallel-fifo interface with FTDI FT232H USB bridge for a maximum of 60 MB/s output data bandwidth;
- 1 high-speed (3.125 Gb/s) I/O transceiver line with SMA connectors;
- interface with GPS module: power supply, serial signals (TX, RX) and pulse-per-second (PPS);
- connector matching the 40-pin general purpose I/O strip of the Raspberry card; most of the signals are routed to the FPGA (f.i. I^2C);
- backup/auxiliary interfaces: SD SPI signals, UART-USB via Silicon Labs CP2102N module and 3 LVTTL general-purpose I/O (2 of them can be configured as a single LVDS pair).

[1] https://www.raspberrypi.org/products/raspberry-pi-3-model-b-plus/

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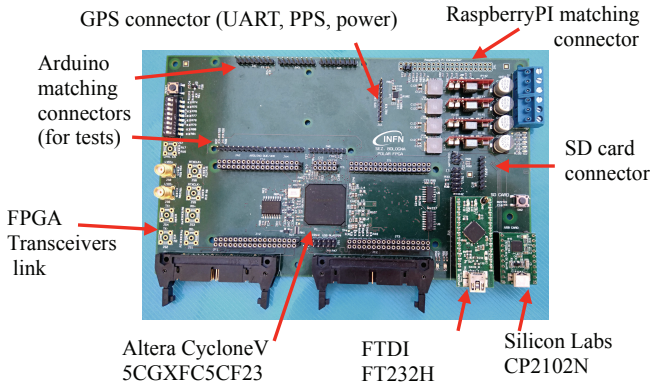

Figure 1: Picture of the Trigger and Acquisition Board. Major components and connectors are highlighted.

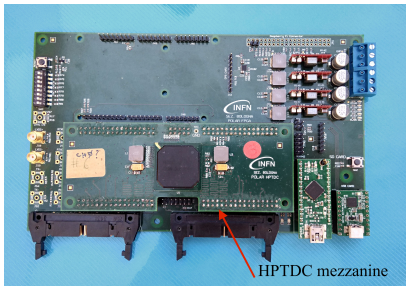

Figure 2: TRB with HPTDC-based mezzanine board plugged on top.

The TRB has a single power input line of 12V and can deliver all its regulated voltages (5V, 3.3V, 2.5V, 1.1V) to outside devices through an ad-hoc connector, so acting as a power distributor for the whole electronics setup.

2.2 Highlights of the firmware designed for the Polar QuEEEst project.

The firmware performs a precise event time-tagging. Coarse information is recorded by decoding GPS information encoded in the NMEA communication standard [5]. The actual firmware recognises three sequences (called GPGGA, GPRMC, GNRMC) and it is proved to be effective in collecting data for both GPS and GLONASS (the russian GLObal NAvigation Satellite System) satellite navigation systems. Fine timing-tag is performed by resetting a 100 MHz clock frequency counter with the precise pulse-per-second (PPS) signal from GPS module.

As for the TDC implementation into the FPGA, we have designed a pure carry tapped delay line made of 512 taps forced to be into the same logic array block. From preliminary tests we have measured an average tap delay of about 9 ps so we decided to sample only one every four (for a total of 128 taps sampled with a 320 MHz clock) in order to speed up the decoding logic with a resolution degradation which turned out to be acceptable for our purposes. We have estimated the TDC resolution by sending the same pulse to each channel and measuring the phase difference between every pair. Given the phase difference histogram for two channels (see for instance fig. 3), the standard deviation of the distribution is the square sum of the single channel RMS resolution. Therefore, all channels resolution can be calculated by solving a linear equations system; typical achieved values range from 40 to 90 ps. Non linearities are calculated from the bin occupancy plots (see for instance fig. 4), which are obtained by sending randomly timed pulses. All channels have typical integral non-linearities (INL) of about 100 ps; typical differential non-linearities (DNL) are comparable (~100 ps). Since the scintillation tiles for the PolarQuEEEst detector were 30x20 cm^2, the maximum timing resolution achievable is about 500 ps. Therefore, TDC performances were considered acceptable and no improving methods were implemented.

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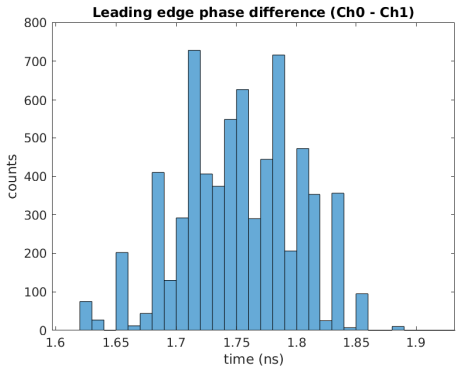

Figure 3: Example of phase difference when the same pulse is applied to two TDC channels.

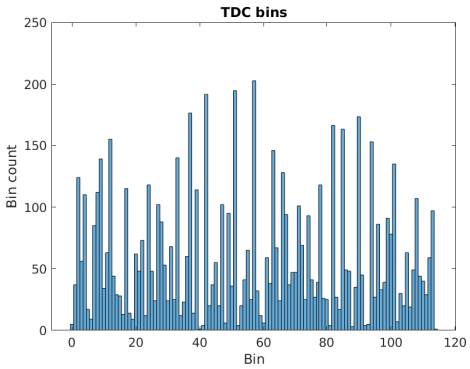

Figure 4: Typical TDC bin occupancy for a randomly-timed signal.

3. Performance of the TRB for the PolarQueEEEst detector

The detector built for the 2018 Polar QuEEst expedition consists of 2 scintillation layers of 60x40 cm (4 tiles/layer), 2 SiPM per tile, for a total of 16 channels digitized by applying discrimination over a programmable thresholds. A complete and easily transportable trigger and acquisition system (fig. 5) has been designed and installed underneath the box containing the scintillators equipped with SiPMs and the front-end electronics. The TRB provides trigger by finding coincidences between layers (a majority of 3 over 4 correspondent SiPM coincidence). When a trigger happens, GPS timing information as well as channel time-over-threshold time (measured from both TDC into FPGA and HPTDC) are packed into a data event and sent to the Raspberry card. In addition, the Raspberry card configures and controls runs as well as acquires data from the environmental sensors. Total power consumption is less than 13 W. About 2 months of cosmic rays events were recorded in Arctic, with a ~30 Hz trigger rate. Data have been off-line corrected using environment sensors and compared with two identical detectors acting as a reference (one in Italy and another one in Norway). First results can be found in [2]. Further measurements have

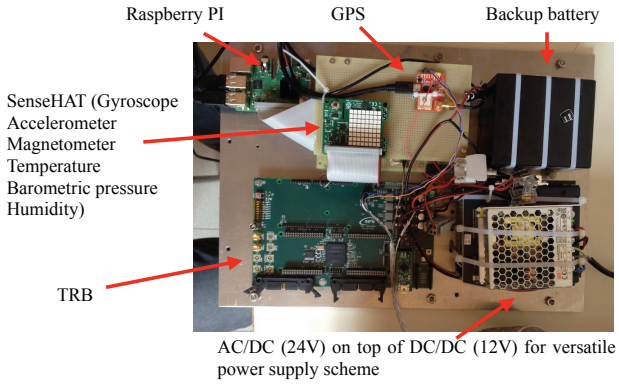

Figure 5: Trigger and acquisition system for the PolarQuEEEst detector. It is hosted into an aluminum box under the detector. Note the versatile power supply scheme: both 220 V AC (for lab operation) and 24 V CC (for ship operation) can be configured as input.

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been accomplished afterwards, confirming the electronics' performance at a greater extent [7]. The portability of the system was confirmed when the detector from Arctic has been carried around Italy, Switzerland and Germany, mostly by car (the detector fits into a medium trunk), in order to provide measurements at several latitudes. Performance has been enhanced when three detectors reconvened at CERN: A new firmware allows all detectors to be synchronized within 10 ns of absolute time reference to look for coincidences. At the end of May 2019 the detectors were installed back at the Svalbard islands, into close barracks (within the Arctic station of the italian CNR research institute) for a few years measurement campaign. Performance of TDC into FPGA are compared with HPTDC configured in low resolution mode (200 ps) and both have been found comparable.

4. Conclusions and future perspectives

The TRB board described in this paper proved to be reliable as a trigger and data acquisition device, providing a low power consumption. An absolute time-tagging event within a 10 *ns* resolution can be achieved by means of an external GPS module. Sixteen TDC channels have been implemented in a Cyclone V FPGA , with an average of less than 100 ps RMS resolution. The TRB performed successfully during the PolarQuEEEst measurement campaign, showing its potential and versatility. Future upgrades can be: use the high speed transceiver for high rate applications; implement more channels into the FPGA; implement more channel in total by separate HPTDC channel from the ones to the FPGA; improve TDC resolution and non-linearity by applying mitigation techniques (such as either Wave Union or Multichain Averaging).

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