Electro-magnetic Crosstalk Effects in a Millimeter-wave MMIC Stacked Cell

# Electro-magnetic Crosstalk Effects in a Millimeter-wave MMIC Stacked Cell

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***Abstract*—This work discusses the design of a 2-stacked cell at 36 GHz, analyzing the large discrepancies found between circuit-level and electro-magnetic (EM) simulations due to crosstalk (gate power leakage). At millimeter-wave frequencies, EM optimization of the inter-stage matching is crucial, however, its layout compactness poses several issues on the selection of the EM set-up, thus simulations reliability was put in doubt. To dispel this doubt the cell was fabricated and tested, demonstrating the effectiveness of EM predictions and the actual presence of gate power leakage. This required a deep re-design of the cell, currently on-going, based on a completely different inter-stage matching approach.**

***Index Terms*—stacked PA, EM design, MMIC design**

## I. Introduction

Efficient and compact power amplifiers (PAs) working at millimeter-wave frequencies, in the Ka-/Q-/V-band, are highly demanded by a number of applications (5G, SATCOM, ...). At such high frequencies, electro-magnetic (EM) verification/optimization of PA passive structures (matching networks) is mandatory, due to possible crosstalk effects among adjacent components, which cannot be predicted in any way by circuit-level (CL) simulations. EM modeling can be a tough job when the structures to be analyzed are complex and have many access ports with different orientation and/or reference planes. This is usually not the case for standard structures, like parallel power combiners, however, when dealing with the inter-stage matching of a stacked-FET PA, several issues can arise.

The stacked power amplifier was first introduced in [1]. It relies on series power combination from a common source (CS) stage and a number of cascaded pseudo-common gate (CG) stages. It shows the advantages of increased bias voltage and output impedance [2], reduced chip area occupation [3] and increased gain [4]. The latter makes the stacked PA particularly interesting also for GaN implementations at millimeter-wave frequencies, where the maximum available gain of single devices is rather low.

This works discusses the design of a 2-stacked cell at 36 GHz, developed with a commercial 100 nm GaN/Si process. Circuit-level predictions for the designed cell were extremely promising, but EM simulations reported instead an unexpected gate power leakage effect due to EM crosstalk. The compactness and complexity of the stacked structure posed several issues on its EM modeling, thus the reliability of EM simulations was questionable and crosstalk effects might have been overestimated. To assess the dependability of EM predictions and the effective presence of power leakage, the original CL-designed cell was fabricated and measured, eventually confirming the accuracy of the EM simulation set-up adopted and the need for cell re-design.

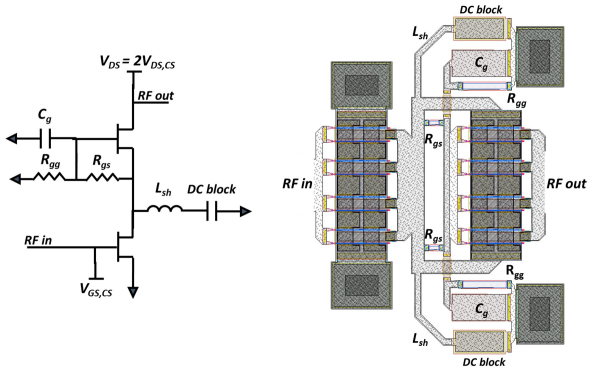


Fig. 1. Schematic diagram (left) and layout (right) of the 2-stacked cell.

## II. Stacked Cell Design

The schematic diagram of the designed 2-stacked cell is reported in Fig. 1 (left). The cell is biased in class-AB with $V_{\mathrm{DD}} = 22.5\,\mathrm{V}$ and $I_{\mathrm{Dq}} \approx 30\,\mathrm{mA}$ (5 % $I_{\mathrm{DSS}}$). The CS and CG stages adopt the same device, namely an $8\times75\,\mu$m device, which shows, at 36 GHz a maximum available gain (MAG) of 6.5 dB. Device stacking should improve this value of roughly 3 dB, achieving a gain around 9 dB, an outstanding value for a power stage at this frequency. As demonstrated in [5], [6], at high frequencies the effect of reactive parasitics creates voltage de-phasing between the stages and must be compensated for. The shunt inductance approach [7] is in this case adopted to internally match the devices on the optimum load.This approach has the advantage of allowing for separately tuning the real and imaginary part of the load seen by the CS stage.

To adopt the developed 2-stacked cell as basic building block of more complex PA structures [8], layout compactness and a self-bias approach are desirable. A 2-stacked cell requires, in fact, three different bias voltages, which represents a potential issue for the routing of the bias lines when many cells must be combined. The self-bias network, composed by $R_{\mathrm{gs}}$ and $R_{\mathrm{gg}}$, allows to derive the CG gate voltage from the CS drain one. Self-bias network design must take into account layout constraints, additional current consumption

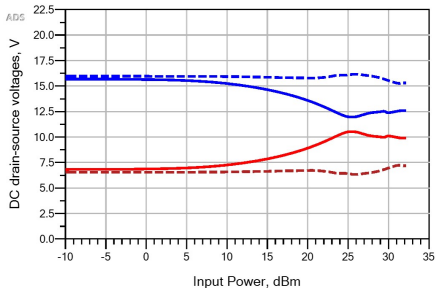


Fig. 2. CL (solid) and EM (dashed) simulated DC drain-source voltages as a function of input power: (red) CS stage, (blue) CG stage.

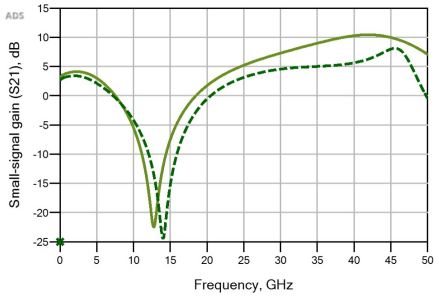


Fig. 3. CL (solid) and EM (dashed) simulated $S_{21}$.

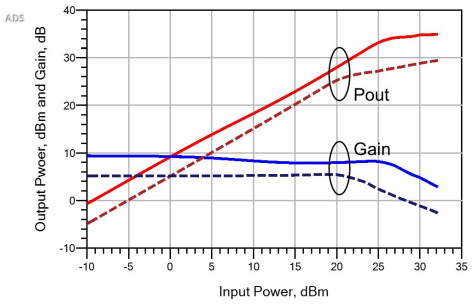


Fig. 4. CL (solid) and EM (dashed) simulated large-signal results at 36 GHz.

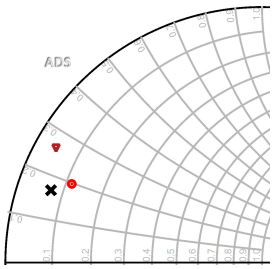


Fig. 5. Synthesized CS load impedance at 36 GHz (nominal output power): CL (circle) and EM (triangle) result compared to the optimum load (cross).

and possible non-linear behaviour of the internal drain-source voltage distribution with input power [6], as shown in Fig. 2. The self-bias network has been thus designed to achieve a fairly equal voltage distribution at the operating output power level rather than in small-signal conditions.

The cell layout is depicted in Fig. 1: symmetry has been enforced by connecting the source of the CG stage at both sides and splitting all the passive elements into parallel pairs. The gate of the CG stage has been extended at the top and bottom edges, crossing the (CS)drain-(CG)source interconnection lines with air bridges and the shunting elements ($C_{\mathrm{g}}$ and $R_{\mathrm{gg}}$) have been placed after the crossing. The shunt inductance $L_{\mathrm{sh}}$ was implemented with a high-impedance transmission line, sharing the via holes for ground connection with $C_{\mathrm{g}}$ and $R_{\mathrm{gg}}$.

## III. Critical Analysis of EM simulations

Circuit-level simulation results are shown in Fig. 3 and Fig. 4: the cell was expected to have a small-signal gain ($S_{21}$) as high as 9.3 dB at 36 GHz, with a saturated output power of 34 dBm, thus very close to ideal stacking operation. However, analyzing the ISMN with Keysight ADS Momentum planar-3D EM simulator, the results obtained showed significantly lower performance, as also shown in Fig. 3 and Fig. 4. The CS stage resulted highly mismatched, as shown in Fig. 5, and a non-uniform DC drain-source voltage distribution appeared (see Fig. 2), causing early compression of the CS stage. Consequently, the saturated output power resulted only 27 dBm (1/5 of the CL prediction) and small-signal gain was as low as 5.1 dB.

The bad results found with EM simulations, are symptoms of possible power leakage from the CS drain to the CG gate, a parasitic crosstalk effect that can dramatically change the cell behavior. EM simulations with Momentum can also output the 2D current density distribution along the simulated structure, selecting one or more of the ports as feed. This feature can be extremely useful to locate critical points of the structure and to trace crosstalk paths among EM coupled structures. Fig. 6 (right) reports the results obtained when the CS drain port is selected as feed: in normal operation the power flow must go from this port to the two source ports, but, in this case, a coupling between the drain-source interconnection lines and the gate is clearly evident at the air bridge crossing point. Hence a more detailed EM analysis of the air bridge structure was carried out: interestingly, EM simulations of the air bridge cross alone give results much more coherent with CL predictions, with limited crosstalk between the crossing lines. Therefore, the power leakage that appears in the full ISMN simulations is a consequence of the combined effect of the air bridge and of the close surrounding elements, making it crucial to EM-simulate the entire network and not only its sub-components to find out all possible interactions.

The accuracy of the EM-modeled networks is therefore crucial for the cell design. If EM simulations are correct, EM crosstalk in the designed cell is unacceptably high and the cell must be completely re-designed. On the other hand, if EM crosstalk is overestimated in simulation, any layout change made to optimize EM result may eventually worsen cell performance.

EM simulations of the ISMN at 36 GHz are indeed very critical and, in particular, the EM port calibration issue is

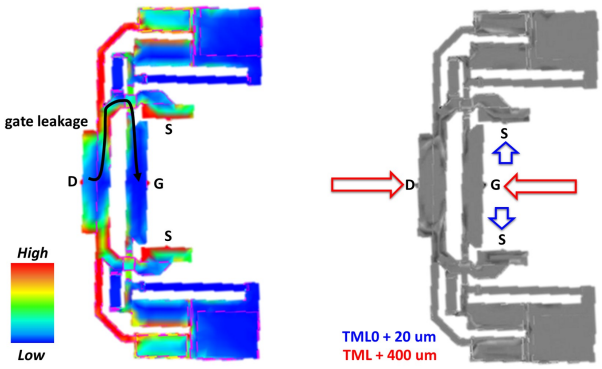


Fig. 6. EM simulation ports setup (left) and 2D map of EM current distribution when feeding the structure form CS drain (left).

worth to be addressed. Momentum offers several types of calibrated and un-calibrated ports, each one suited for a specific application. The transmission line calibration (TML) should be in principle adopted to simulate a MMIC matching network in conjunction with additional offset lines (to be then de-embedded) which ensure that the feeding signals arriving at the ports are uniformly distributed and do not interfere with the network discontinuities. However, for the stacked ISMN, the CG source ports are orthogonal to the CG gate port and are facing each other, thus making it impossible to adopt TML calibration and long offset lines. The final EM set-up selected is that of Fig. 6 (left), with 400 $\mu$m-offset TML ports at CS drain and CG gate terminals and 20 $\mu$m-offset TML-zero-length (TML0) ports at CS source terminals. This set-up is expected to provide the best accuracy in terms of port discontinuity de-embedding.

## IV. Experimental Characterization Results

The unexpected gate leakage found with full-ISMN EM simulations was so severe that a possible overestimation due to inappropriate EM set-up was suspected. In order to verify the dependability of the performed EM simulations, the designed stacked cell was fabricated and characterized (see Fig. 7). Small-signal scattering characterization is performed from 1 GHz to 40 GHz adopting an Agilent E8361A PNA, calibrated with a 2-port SOLT procedure. Fig. 8 reports the comparison of the simulated and measured small-signal gain $S_{21}$, when both ports are referred to 50 $\Omega$. The measured data are in fairly good agreement with the EM simulations, while the CL simulations are less accurate in predicting the minimum around 15 GHz and overestimate gain at the design frequency. Moreover, when re-normalized to the optimum source and load impedances determined in simulations, the measured S-parameters predict a small-signal gain around 4 dB at 36 GHz, which is in line with EM predictions ($\approx$5 dB) and much lower than CL ones (>9 dB). This results demonstrates, on one hand, that the adopted EM set-up is reliable despite the high operating frequency and the network complexity. On the other hand, it also proves that the designed cell actually suffers from

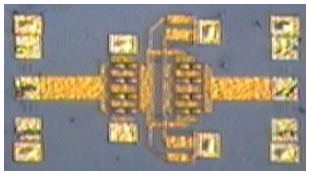

Fig. 7. Microscope picture of the realized stacked cell.

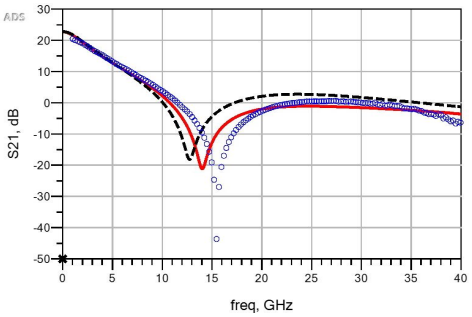


Fig. 8. $S_{21}$ of the stacked cell (50 $\Omega$ reference): comparison between CL simulations (black), EM simulations (red) and experimental results (blue).

the gate power leakage predicted by EM simulations and must be re-designed. A new stacked cell, adopting a different inter-stage topology, is currently under development.

## V. Conclusions

The design of a self-biased 2-stacked cell at 36 GHz has been discussed, comparing CL and EM simulation results with small-signal measurements. Characterization results proved to be in line with the extremely pessimistic EM results. This confirms the key role of EM optimization at high frequency and proves the accuracy of the EM simulation set-up adopted, even in presence of a very complex network. It also demonstrates the severity of crosstalk effects in stacked PA design.

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