GaN Doherty MMIC Power Amplifiers for Satellite Ka-band Downlink

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***Abstract*—This work presents the design and preliminary experimental results of two integrated Doherty power amplifiers fabricated on 100 nm Gallium Nitride on Silicon, targeting the satellite downlink Ka-band (17.3–20.3 GHz). The MMICs, based on different architectures, have been designed respecting the stringent limits on linearity and devices' maximum junction temperature imposed by the application. Nevertheless, an average output and efficiency higher than 36 dBm and 30%, respectively, are expected across the overall band, while fulfilling the aforementioned constraints. The initial characterization of the fabricated MMICs shows measured small signal behaviours well in agreement with the simulations. In particular, for both MMICs, the measured small signal gain is in excess of 25 dB with both input and output return losses better than 10 dB in the whole frequency band.**

***Index Terms*—Power amplifiers, SatCom, Doherty, GaN.**

I. Introduction

Satellite communication services have evolved to accommodate high data rates and flexible area coverage. The adoption of spectral efficient modulations, often in conjunction with multi-beam active antennas, leads to large peak-to-average power ratio signals that require output power back-off operation of the Power Amplifiers (PAs) to avoid clipping and strong non-linearity effects. The ability of the Doherty Power Amplifier (DPA) to operate efficiently at significant output power back-off has made it the reference solution in the mobile base-station market where it is operated in combination with powerful digital linearisers. However, this approach is practically unfeasible for space applications where such digital linearisers cannot be employed, thus posing strong requirements on the DPA linearity. The typical distortion parameter used in satellite system is the Noise-to-Power Ratio (NPR) [1] that must be adopted when dealing with spectrally efficient modulation schemes.

This work presents two Monolithic Microwave Integrate Circuits (MMICs) DPAs fabricated on 100 nm GaN-Si technology, targeting the satellite downlink Ka-band (17.3–20.3 GHz). Two different design strategies, with their pros and cons in terms of performance and practical considerations, are discussed and the simulation results with large-signal models and fully-EM simulated networks are presented. The initial characterization results on a significant number of MMIC samples are also shown, highlighting a good agreement between simulated and measured parameters.

II. Design

A. Specifications and technology

The design of integrated DPAs is particularly challenging when dealing with applications requiring large bandwidth at high carrier frequency. Indeed, keeping the load modulation and the phase alignment under control on reasonable bandwidths, and maintaining at the same time good linearity, requires *ad-hoc* design solutions and very accurate large-signal models and measurements [2], both for Class-AB and -C conditions. This task becomes even more complex for space applications, due to the de-rating rules on supply voltage, maximum junction temperature, and radiation hardness.

The design specifications for the DPAs presented in this work are summarised and compared with the current state of the art in Table I. The target output power and efficiency are above the current state of the art, especially considering that most of available examples are not designed to respect the stringent thermal constraints of satellite applications.

TABLE I
Comparison between target performance and SOA Ka-band PAs

Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	NPR (dB)	Der. Y/N	Ref
20–21	33	27	27.5	15	N	[3]
18–20	34.5	18	22	–	N	[4]
21–23	32	32	17	–	N	[5]
20.2–21.2	29	18	19	–	N	[6]
17.3-20.3	**36**	**35**	**30**	**15**	**Y**	**Target of T.W.**

For [3], data at 15 dB NPR. For [4], [5], [6] an estimate for similar linearity

In addressing such a demanding target, technology plays a crucial role. The present market in terms of MMICs beyond X-band is still dominated by short-gate Gallium Arsenide pseudomorphic High Electron Mobility Transistors (pHEMTs) thanks to their high cut-off frequency (above 100 GHz) and excellent noise figure. The main issue is related to the low power density, of the order of 0.5 W/mm at mm-waves, thus requiring large-scale on-chip power combination and hampering significantly the bandwidth and efficiency. This issue is particularly evident for DPAs, where the constraints dictated by the load modulation complicate further the design. GaN has shown very promising results, and is today available

on both Silicon Carbide (SiC) and Silicon (Si) substrates. For mass applications and where a steady supply chain is required, GaN-Si can be seen as a preferred choice also in consideration of the possible integration. Additional advantages come from the larger wafers and lower production costs [7]. Thermal management, on the other hand, requires particular attention due to the worst thermal conductivity of Si compared to SiC [8]. The selected technology in this work is a 100 nm GaN-Si, with cut-off frequency around 100 GHz and power density in excess of 2 W/mm at the frequencies of interest, when accounting for the space de-rating on the supply voltage.

B. Strategy

For the selected technology, the largest device for which a large-signal electrothermal model is available is the $8 \times 100\,\mu$m, which can provide around 33.5 dBm saturated output power and 9 dB gain at 18.8 GHz (center frequency) for the highest required backside temperature (75°C), with efficiency around 52%. To meet the output power requirement, on-chip power combination is required. Accounting for the losses of the passive networks and the foreseen amount of back-off to operate with the required linearity, the selected total periphery of the final stage is 3.2 mm (4 identical $8 \times 100\,\mu$m devices). Moreover, as the final stage does not exceed 10 dB of gain, a 3-stage architecture is selected to meet the gain requirement.

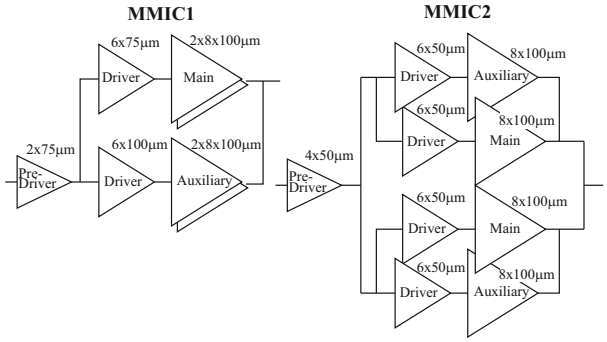

Fig. 1. Comparison between the circuit planning for MMIC1 (left) and MMIC2 (right).

The MMICs presented in this work are based on the same final stage overall periphery, but radically different design strategies, see Fig. 1.

MMIC1 is a single DPA whose main and auxiliary branches are composed of two parallel-combined $8 \times 100\,\mu$m devices. Compensation of the output capacitance of the device is achieved by using a stub, followed by a matching combiner. The low-impedance quarter-wave inverter is implemented with a capacitive-loaded microstrip line, connected on the main side straight to the common 50 Ω load. The auxiliary side uses a compensated half-wave microstrip line to maximize the bandwidth and to adjust the back-off output impedance.

MMIC2 combines two DPAs, each of them using a single $8 \times 100\,\mu$m device for the main and auxiliary. The output capacitance of the device is embedded in the impedance inverter, completed by a series piece of line and a shunt capacitor. The common-node impedance is low, requiring further matching to the external 50 Ω. In this case, only an additional quarter-wave is used on the auxiliary side.

MMIC1 has the advantage of a simpler layout and routing compared to MMIC2, with smaller overall size as it can be appreciated in Fig. 2, where microscope pictures of the fabricated MMICs are shown. On the other hand, MMIC2 allows a better control of load modulation since the DPA combiner is designed at single device level.

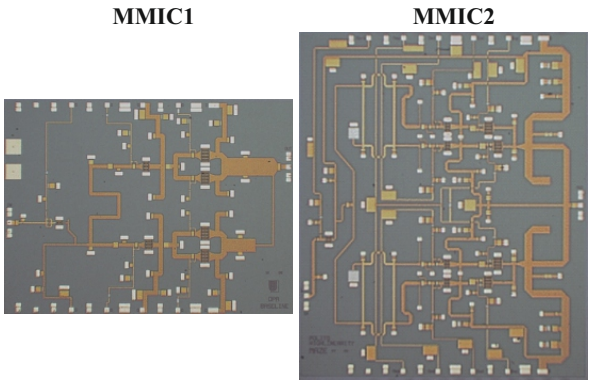

Fig. 2. Microscope pictures of the fabricated MMIC DPAs. MMIC1 (left): 5x3.7 mm^2. MMIC2 (right): 5x6 mm^2.

Both MMICs integrate the drivers in the main and auxiliary branches, and use an additional pre-driver in front of all the combined stages. In particular, MMIC1 adopts a $2 \times 75\,\mu$m pre-driver, a $6 \times 75\,\mu$m driver for the main stage and a $6 \times 100\,\mu$m driver for the auxiliary stage. MMIC2 uses a $4 \times 50\,\mu$m pre-driver in front of the two combined DPAs, each of which includes separate $6 \times 50\,\mu$m drivers in the main and auxiliary stages and is fed at the input by an isolating power splitter based on a semi-lumped branch-line topology. The presence of the isolated power dividers at the input enhances the matching compared to MMIC1, which features a non-isolating splitter between the pre-driver and the Doherty stage.

Overall stability has been carefully assessed by using loop-stability analysis. This step is necessary given the complexity of the designs, especially considering the embedded drivers and the overall high gain. Countermeasures have been taken by adding damping resistors for both in-band and out-of-band stabilization. Very low-frequency stabilization will be ensured with off-chip by-pass circuitry.

III. Results

The simulated large signal performance from 17.3 GHz to 20.3 GHz is shown in Fig. 3. The nominal gate bias conditions ($V_{\mathrm{G,PD}}$=-1.3 V, $V_{\mathrm{G,DM}}$=-1.3 V, $V_{\mathrm{G,M}}$=-1.45 V, $V_{\mathrm{G,DA}}$=-1.45 V, $V_{\mathrm{G,A}}$=-4.5 V for MMIC1 and $V_{\mathrm{G,PD}}$=-1.4 V, $V_{\mathrm{G,DM}}$-1.4 V, $V_{\mathrm{G,M}}$=-1.4 V, $V_{\mathrm{G,DA}}$=-2.4 V, $V_{\mathrm{G,A}}$=-1.9 V for MMIC2) are applied to the two MMICs, with a drain supply voltage of $V_{\mathrm{DD}} = 11.25$ V in all cases. The NPR of the MMICs is evaluated in simulation by using the harmonic balance two-tone test and applying the approach of [1]. Considering the memory effects of the amplifiers, the tone spacing is

swept from 18 MHz to 900 MHz. This leads to upper (with also the presence of sweet spots) and lower bounds for the NPR estimation. The power level corresponding to 15 dB NPR highlighted in Fig. 3, where the performance is evaluated, corresponds to the lower bound estimated at 18.8 GHz.

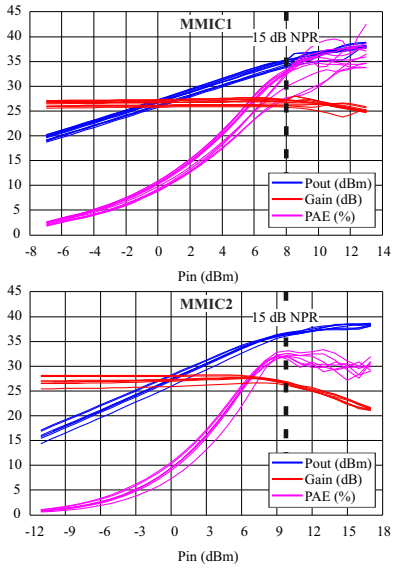

Fig. 3. Simulated large signal performance for MMIC1 (above) and MMIC2 (below).

IV. Measurements

A first set of measurements has been performed on the whole wafer to identify the functional dies that will be mounted on carrier jigs for the large-signal characterisation.

A PNA vector network analyser was used to measure the 2-port scattering parameters from 10 MHz to 50 GHz, calibrated on-wafer with a short-open-load-through calibration. Two bias conditions were considered for the MMICs. The first is the nominal bias condition (A), with the main stages in class AB and the auxiliary stages turned-off in class C. The second condition (B) is with both branches, main and auxiliary, in class AB. Although not an operational condition, the latter is useful to assess the operation of the auxiliary side and to provide early information for the comparison measurements vs. simulations.

The measured small-signal gain in the nominal bias condition, compared with the simulated one, is shown in Fig. 4 and Fig. 5, for MMIC1 and MMIC2, respectively, in the 1 GHz–50 GHz frequency range. To be noted the rather good agreement between simulations and measurements; only MMIC1 shows a slight shift in frequency. The same agreement is obtained in the bias condition B (all-on) here not reported.

V. Conclusion

Two integrated Doherty power amplifiers for Ka-band satellite applications have been presented. Simulations show the potential to provide power added efficiency better than 30% while respecting system level temperature and linearity

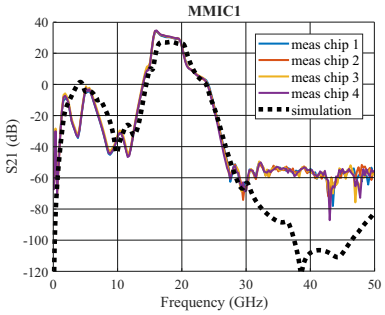

Fig. 4. Simulated and measured small-signal gain in the nominal bias condition (A) for MMIC1.

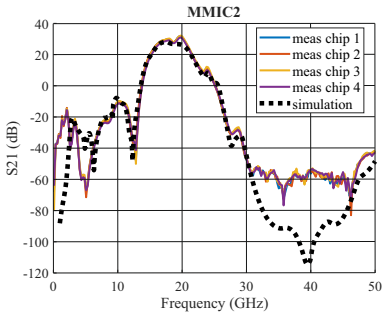

Fig. 5. Simulated and measured small-signal gain in the nominal bias condition (A) for MMIC2.

requirements. Initial measurements on wafer before dicing and fixturing show good uniformity of performance and agreement with simulations.

References

[1] N. B. Carvalho and J. C. Pedro, "Compact formulas to relate ACPR and NPR to two-tone IMR and IP3," *Microwave Journal*, vol. 42, no. 11, pp. 70, 77–78, 80, 82, 84, Dec 1999.

[2] R. Quaglia, A. Piacibello, F. Costanzo, R. Giofrè, M. Casbon, R. Leblanc, V. Valenta, and V. Camarchia, "Source/Load-Pull Characterisation of GaN on Si HEMTs with Data Analysis Targeting Doherty Design," in *2020 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2020, pp. 5–8.

[3] V. Valenta, I. Davies, N. Ayllon, S. Seyfarth, and P. Angeletti, "High-gain GaN Doherty power amplifier for Ka-band satellite communications," in *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan 2018, pp. 29–31.

[4] C. Friesicke, P. Feuerschutz, R. Quay, O. Ambacher, and A. F. Jacob, "A 40 dBm AlGaN/GaN HEMT power amplifier MMIC for SatCom applications at K-band," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016, pp. 1–4.

[5] C. Campbell, K. Tran, M.-Y. Kao, and S. Nayak, "A K-Band 5W Doherty Amplifier MMIC Utilizing 0.15μm GaN on SiC HEMT Technology," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE*, Oct. 2012, pp. 1 –4.

[6] O. Cengiz, O. Sen, and E. Ozbay, "High power K-band GaN on SiC CPW monolithic power amplifier," in *2014 9th European Microwave Integrated Circuit Conference*, Oct 2014, pp. 548–551.

[7] V. Camarchia, R. Quaglia, A. Piacibello, D. P. Nguyen, H. Wang, and A. V. Pham, "A Review of Technologies and Design Techniques of Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, to be published (DOI: 10.1109/TMTT.2020.2989792).

[8] C. Ramella, M. Pirola, A. Reale, M. Ramundo, P. Colantonio, M. A. D. Maur, V. Camarchia, A. Piacibello, and R. Giofrè, "Thermal-aware GaN/Si MMIC design for space applications," in *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, 2019, pp. 1–6.