

Doctoral Dissertation

Doctoral Program in in Electrical, electronics and Communications Enginering, with curriculum in "Electronic Devices" in convention with the National Institute for Nuclear Physics (32^{nd} cycle)

Low-Power Mixed-Signal ASIC for Cryogenic SiPM Readout

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Politecnico di Torino

2020

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Turin, 2020

Summary

There is a growing interest in the use of Silicon photomultipliers (SiPMs) operating at cryogenic temperatures. The largely suppressed dark count rate observed at liquid Xenon and liquid Argon temperature makes such sensors ideally suited to equip large area detectors like those needed in dark matter and neutrino experiments. Research programs to explore the possibility of building total body PET scanners based on noble liquids readout by SiPM are also ongoing. Highly integrated front-end electronics embedded in the cold volume close to the sensor allows for a significant reduction of the interconnections and feed-through as data can be easily multiplexed and serialised in the digital domain. Depending on the application, the SiPM pixel size may range from a few mm^2 to a few cm^2.

The INFN-Torino group developed a low-power mixed-signal ASIC to readout SiPM at low temperature. The chip, called ALCOR, is designed in 110 nm CMOS technology, is a first prototype suitable for future 3D integration with the photon sensor. The architecture comprises of 32 independent pixels, each of them features an analogue front-end, discriminators, digital logic and low-power TDCs based on analogue interpolation. The total area of the IC is $4.95 \times 3.78\ mm^2$, where each pixel occupies $500 \times 500\ \mu m^2$ for a power consumption less than $10\ mW$. The pixel generates the timestamp of the arrival time of the event when it operates in a single photon detection mode, but it can be programmed to operate also in Time-over-Threshold where two timestamps are generated for each event. This modality is useful when many photons pile-up to yield a continuous signal. In single photon counting mode, an event rate of up to $5\ MHz$ per pixel can be accommodated. The time binning of TDCs is $50\ ps$ at the maximum system clock frequency of $320\ MHz$. The 32-bit data payloads are transmitted externally to a FPGA through four LVDS drivers with maximum throughput of $640\ Mb/s$.

Normally, digital standard cell models below $-40\ ^{\circ}C$ are not provided by the technology vendor. Therefore, a preliminary Test Chip ASIC has been produced and tested in order to get insight into cryogenic behaviour. This ASIC embeds some of critical building blocks that are employed in the mixed-signal ASIC. In particular, a digital synchronisation circuit designed with 110 *nm* standard cells has been included. This thesis reports the dedicated test results at cryogenic temperature and a comparison with SPICE simulation of extrapolated models at 77 K of the same circuits.

My personal contribution to the development of this work has been divided into three parts. The first part concerns the definition of specifications, simulation and implementation of digital circuits for ALCOR. Subsequently, I dealt with the development and cryogenic characterization of some critical digital blocks. Finally, I carried out a preliminary study of a distributed sensor network that allows to minimize the number of interconnections with the outside world while maintaining a high fault tolerance.

The Chapter 1 introduces the DarkSide-20k experiment, an underground detector for direct dark matter detection which is the future upgrade of the DarkSide-50 detector built in Laboratori Nazionali del Gran Sasso (LNGS). The detector is based on a two-phase Liquid Argon Time Project Chamber and cryogenic SiPM photo sensors to detect scintillation events.

The Chapter 2 describes briefly the structure and behaviour of SiPM photosensor and reports the state-of-art of ASICs for both analogue and digital SiPM readout.

The Chapter 3 discussed the design of the mixed-signal ASIC suitable for cryogenic SiPM readout. The chapter describes the architecture employed and the chip simulation results that describe the behaviour of the circuit.

The Chapter 4 reports the issue related to designing a digital circuit for the cryogenic environment, showing the characterisation and results of a test chip fabricated embedding important building blocks.

The Chapter 5 describes a preliminary study of a distributed readout network suitable for a large area of sensor. It describes the implementation of the network in a 3D digital SiPM where data are digitised and multiplexed reducing the cable connection at the minimum necessary.

Keywords: Noble liquid detectors, Mixed analogue digital integrated circuits, Timing, Cryogenic electronics.

Acknowledgements

I would like to acknowledge my supervisor Angelo Rivetti, for his wise advice and for all his support during my doctoral studies. Special thanks to Manuel Rolo for his teaching and expertise that made this work possible.

My gratitude also goes to the VLSI office: Federico, Jonhatan and Fabio that welcomed me from the very beginning in this group; Antonio, Simona and Weishuai my 32^{nd} cycle mates with whom I shared incredible experience during this three years; Alejandro, Lorenzo and Raffaele whom brought experiences and laugh to this group. Many thanks to the INFN Torino Darkside group: Giulio Dellacasa, Marco Mignone and Richard Wheadon.

I would like to express my most sincere thanks to my parents, my relatives and my friends for their support. In particular, my brother Thanushan that has guided me since I was born and made me what I am today.

Finally, the best thanks goes to my fiancée Babithra, who through her love, her advice and her patience has supported me till the end and beyond.

To all people that find the courage to change their life for a brighter future.

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Chapter 1

Engineering challenges in dark matter detectors

The existence of dark matter in the Universe is commonly accepted as the explanation of many astrophysical and cosmological phenomena. Roughly 85 % of the matter in the universe is in some non-baryonic form that neither emits nor absorbs electromagnetic radiation, material that scientists cannot directly observe. Dark matter particle should interact weakly or sub-weakly with photons and ordinary baryonic matter. Therefore, one of the most promising hypothesis that explains these observations is that dark matter is made of Weakly Interacting Massive Particles (WIMP) [70, 14, 33]. However, no such particles exist in the Standard Model, and none have been directly observed at particle accelerators or elsewhere. Hence, the nature of the dark matter remains unknown. WIPMs can be observed in three classes of searches: indirect detection based on the observation of gravitational effects thanks to satellites (LAT [7]), balloons (GAPS [12]) and ground-based telescope (CTA [22]); direct detection in shield underground detectors and detection at particle colliders where dark matter particles may be directly produced in high-energy collisions (DEAP-3600 [8], XENON1T [11]).

This chapter will take the DarkSide-20k experiment as example to discuss the engineer challenges in the dark matter detector.

1.1 DarkSide-20k

The DarkSide Collaboration, following the operational experience with the DarkSide-50 detector in a background-free mode at Laboratori Nazionali del Gran Sasso (LNGS) laboratory, is building DarkSide-20k (DS-20k), a direct WIMP detector that employs two-phase Liquid Argon Time Projection Chamber (LAr TPC) with a total active mass of 38.6t and a fiducial mass of 31.8t with 10 cm cut both vertically and laterally. The target sensitivity for this upgrade is to reach a cross sections of $1.2x10^{-47}$ cm^2 for WIMPs of 1 TeV/c_2 mass, achievable in a 5 year run producing an exposure of 100t per year free from any instrumental background interaction lower than 0.1 events. The structure of DS-20k experiment, shown in Figure 1.1, consist of two detectors: the inner and the veto detector. [2, 83, 52, 13, 31]

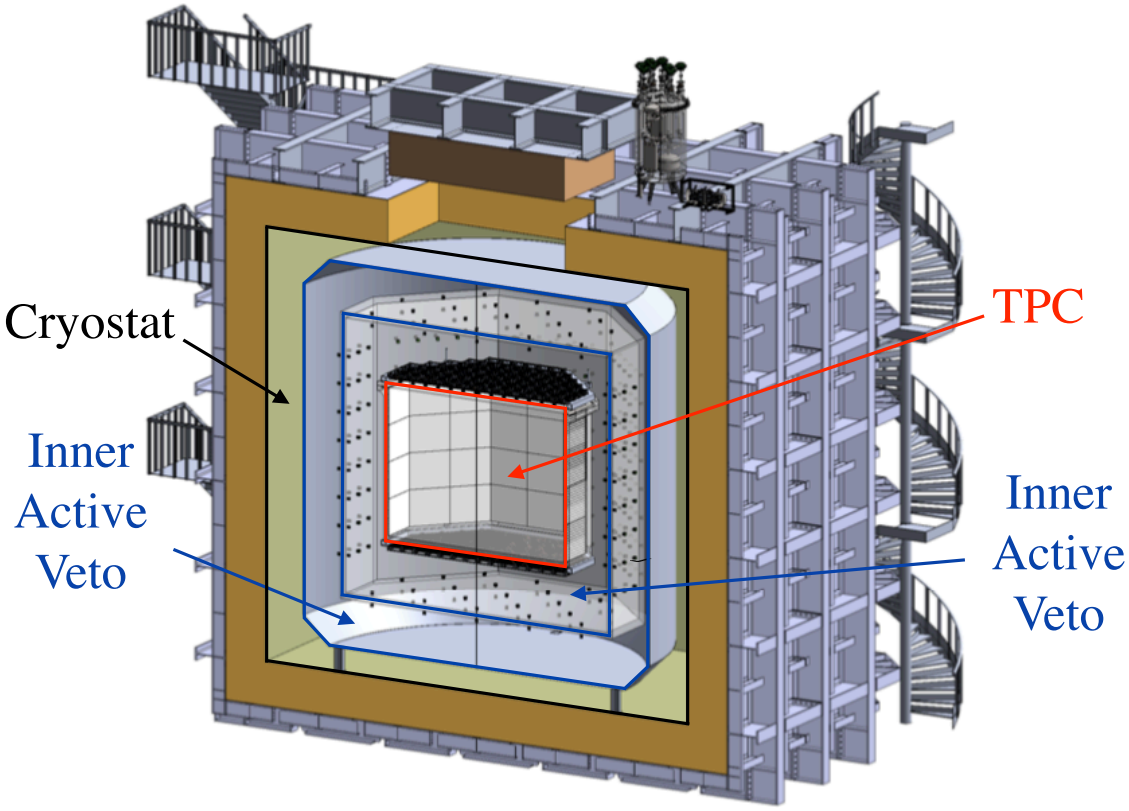


Figure 1.1: 3D schematic of the DS-20k experiment.

The inner detector is an octagonal shape TPC filled with underground argon (87 K) with a dimension from edge to edge of 3.5 m and a high of 2.63 m. Top and bottom of TPC are covered by SiPM detectors. The SiPM sensor employed in DS-20k experiment are mounted on basic Photodetector Module (PDM) such a way to include mechanical structure required to assemble all sensors and to efficiently dissipate heat in order to minimize the production of bubbles inside the detector (Figure 1.2). The single PDM has a dimension of 5 cm × 5 cm and it is build with 24 rectangular SiPM of 12 mm × 8 mm developed by Fondazione Bruno Kessler (FBK) [1]. The characteristics of SiPM required for this experiment are: a PDE parameter equal or greater than 45% at 420 nm wavelength and a total correlated noise probability lower than 60%.

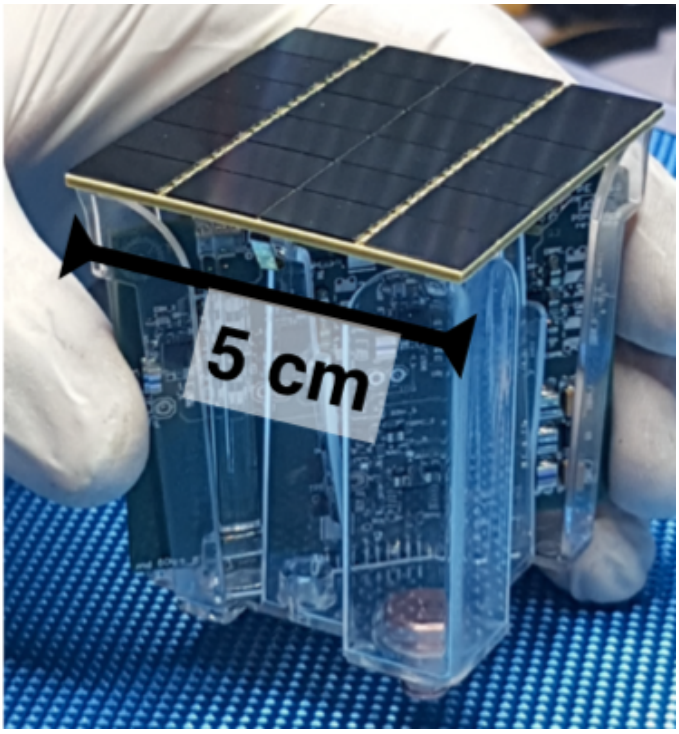


Figure 1.2: Single PDM of $5 \times 5 cm^2$ has mounted 24 SiPMs of 12×8 mm^2 each. The structure comprises also the readout electronics [21].

PDMs are then combined in two different shapes: Square Board (SQB) and Triangular Board (TRB) motherboards. Each SQB contains 25 PDMs and are used to cover the majority of active area of the bases of TPC. Figure 1.3 depicts the first fully mounted motherboard structure of a SQB. While TRB are bild with 15 PDMs and are used to fill remaining holes of the octagonal shape. The motherboard structure is made such that

each PDM can be easily removed and replaced, during the assembly and construction phase, with a new one in case of a failed sensor. Inside the inner detector there are 8280 PDMs equally distributed on the top and on the bottom of the TPC for a total area of 20.7 m^2. The Fig.1.4 shows the pattern scheme of motherboards distributed at the base of TPC detector.

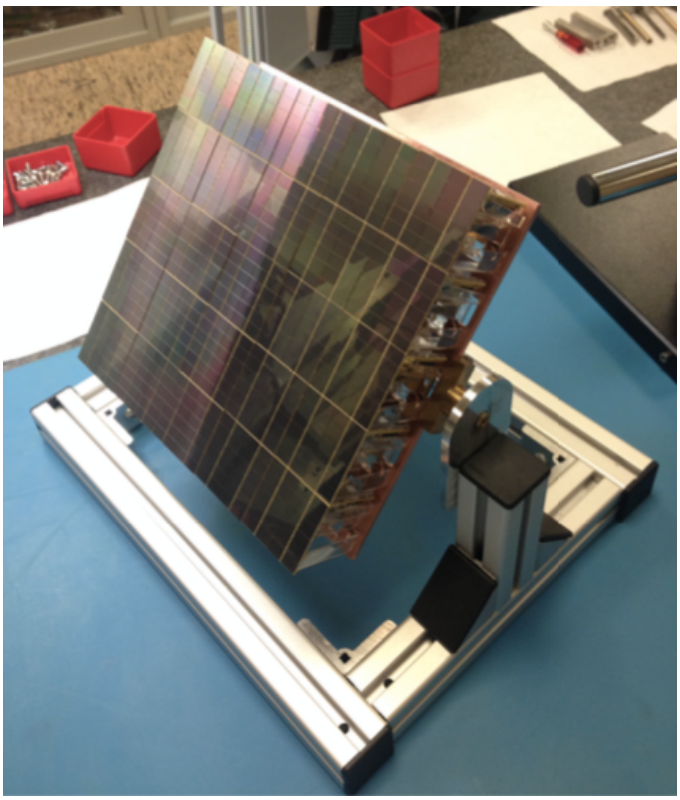


Figure 1.3: Single SQB motherboard fully equipped with 25 PDMs.

The energy deposited in the LAr by an energetic charged particle, electron or nuclear recoil results in a production of excited and ionized argon atoms that carry out a formation of argon excimers decaying thorough emission of scintillation light. This first instant light contains two components with different time constant of emission, the combination of both is marked as S1. This signal is used for energy determination and pulse-shape discriminator. LAr scintillation has a wavelength of 128 *nm* that is absorbed in most of the materials, therefore a wavelength shifter must be used to cover all the area that the light will hit. The first scintillation produces ionization electrons that escape from the recombination are accelerated through a strong electric field to the

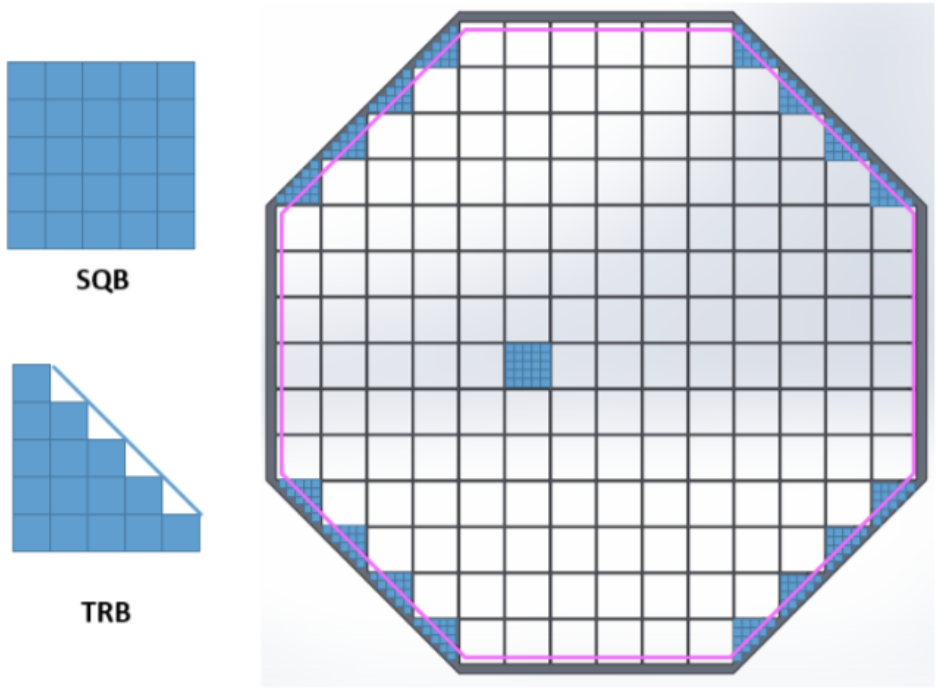


Figure 1.4: Patterning scheme of the motherboards on the base surface of the TPC.

top of TPC, where gaseous Argon reacts with those electrons generating a secondary scintillation signal proportional to the ionization charge, marked as S2. This secondary signal is used for energy and 3D position of the event, the z coordinate is recovered from the drift time between S1 and S2, while the x/y coordinates are given from the pattern of light in the top photosensor area of the TPC. Figure 1.5 shows a full simulation of S1 and S2 signal in TPC detector. The S2 signal generated from the gas layer is mainly detected by top SiPM, while S1 signal is distributed approximately on both top and bottom sensors and it produces at maximum $1 Photon Electron(PE)$ per tile, for expected 3.3×10^3 noise hits during the drift time. The S2 signal is a sum of pileup photons, and it lasts for 20 μs. The number of photons depends on mainly on the details of LAr TPC design, where half of the photons may be concentrated on a few PDMs. The single sensor may produce 4000 PE at a peak rate of $0.4 PE/ns$.

SiPM arrays are placed above the anode and below the cathode and are set on the top and on the bottom of TPC in order to detect both light scintillations with high efficiency. Each PDM will also embed a cryogenic preamplifier that amplifies and shapes the signal before it is sent to a signal transmitter. It must be pointed out that all components

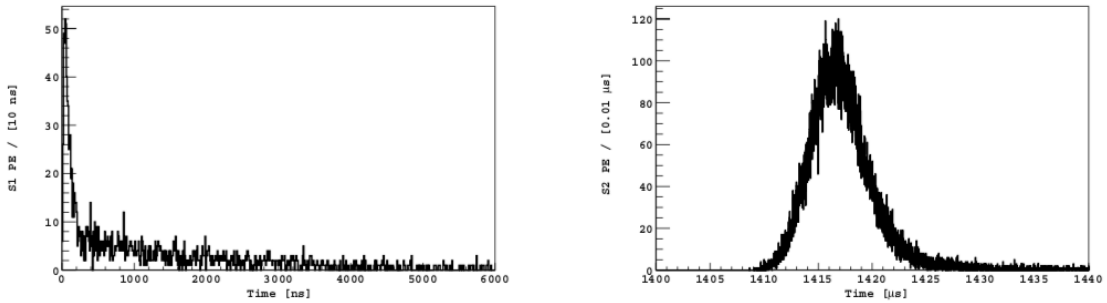


Figure 1.5: Simulation of arrival time of S1 (left) and S2 (right) signals in DarkSide-20k experiment. [2]

making the detector, like the cryostat, the LAr TPC, the SiPMs and cables, must be made from material of the highest radiopurity to keep backgrounds as small as possible in order to reduce any contamination to the measurements. Therefore, the SiPMs on the same PDM are grouped in a single readout channel, in order to reduce the total mass of signal cabling and the number of flanges. The SiPM sensors typically have a total terminal capacitance in the order of 50 pF/mm^2. This implies a careful design of the readout electronics circuits and SiPMs connection scheme on the tile in order to maximise the signal to noise ratio. The aim in DS-20k is to operate with 8280 channels, each as a single analogue element which is transmitted outside the cryostat layer and digitized by a DAQ system placed in the warm area.

A correlated S1 and S2 event rate of 45 Hz is expected in the DS-20k experiment. The average event rate in the single channel is dominated by the SiPM's Dark Count Rate (DCR), where the experiment specification requests about 250 Hz per single module, therefore total expected rate for the TPC is about $250\ MHz \times 8280 = 2.07\ MHz$.

The veto detector surrounds the TPC, the total volume is composed by an Inner Active atmospheric argon Buffer (IAB) surrounding the LAr TPC, a passive Gd-loaded pure polymethyl methacrylate shell an Outer Active atmospheric argon Buffer (OAB). AAr scintillation light will be detected employing SiPM's and dedicated front-end electronics. The contamination of both buffer's signal will be used to mark and reject neutron-induced signals.

1.1.1 SiPM readout in DS-20k

The SiPM readout electronics for the DS-20k experiment has been developed considering the single PDM tile equipped with 24 SiPMs [27, 28]. The discrete electronics will be mounted with the sensor module inside the cryogenic environment. Therefore, all the system has been designed considering the low temperature requirement, and in particular the materials employed have been chosen in order to be immersed in the LAr. Placing the readout electronics inside the cryostat allows to minimize the capacitance at the input of front-end amplifiers and to improve the signal integrity [62].

The tile is divided in 6 SiPMs quadrants and each of them is read with an independent low-noise Transimpedance Amplifier (TIA) based on *LMH6629* from Texas Instrument for high-speed operational amplifier [29]. Then a second-stage amplifier is used to sum the four TIAs and bring out the analogue signal from the cryostat. The schematic diagram of this circuit is depicted in Figure 1.6, where the SiPM inside the single quadrant are placed in three branches with two sensors in series. This topology allows to reduce the noise since the series arranging reduces the detector capacitance seen from the TIA. The cryogenic summing amplifier uses the operational amplifier *LMH6624* from Texas Instrument [30]. The signal gain is 10 V/V, while the noise gain is 41. The maximum bandwidth achievable is 36 MHz at room temperature and 30 MHz at cryogenic temperature.

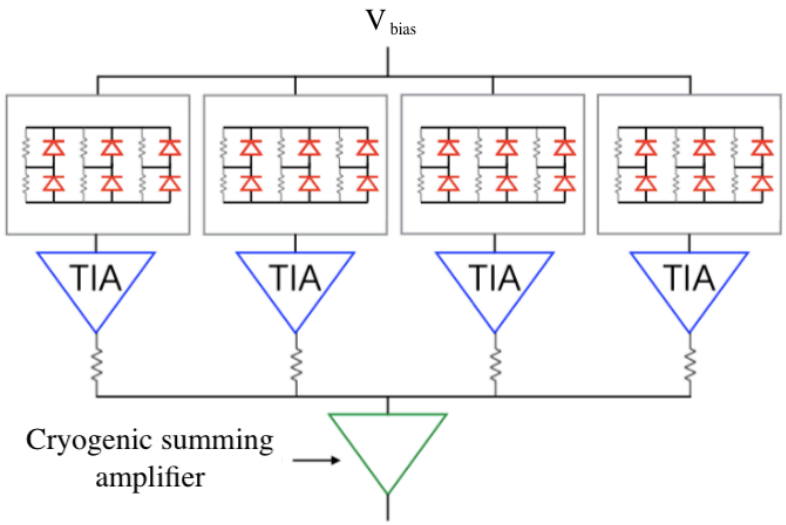


Figure 1.6: Schematic diagram of SiPM sensor of DS-2-k experiment.

The amplified analogue signal is then driven outside the cryostat and digitised by a Data Aquistition (DAQ) system. The DAQ system digitizes each channel in order to characterise each PDM signal in terms of the work function, pulse shape, single photon response, dark rate, stability in time, correlated pulses, and robustness to mechanical stress tests. Figure 1.7 depicts the schematic diagram of the DAQ system developing for DS-20k experiment. The DAQ is a multi channel board hosting fast $14 - bit$ Analog to Digital Converter (ADC) and 125 MS/s sampling rate, linked to Field-Programmable Gate Array (FPGA) for digital signal processing. The analogue filter will minimize the rate of fake rates, depending on the SNR of the cryogenic readout electronics. The FPGA will choose the short pulse (case S1) or long pulse (case S2) path according to the length of the discriminator pulse. In case of S1 signal, a TDC algorithm will search for the time of the event and its amplitude. While in case of S2 signal, the corresponding samples will be down-sampled with a CIC filter to frequency compatible with the signal (about 10 MHz). The DAQ is trigger-less, with the system clock frequency of 1 Hz. The connection with this system and an external computer will be through a 1 $Gbit/s$ to 10 $Gbit/s$ Ethernet connection.

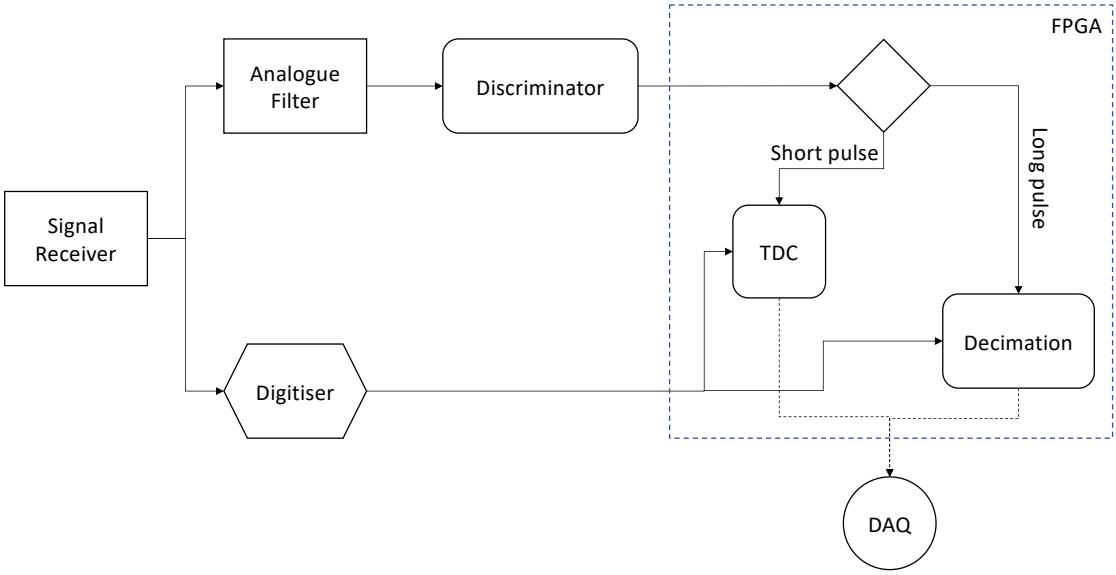


Figure 1.7: Schematic diagram of data acquisition system.

1.2 SiPM signal digitisation on-cold

In DS-20k, the current solution to readout SiPM sensors of the TPC are based on discrete electronics that provides 8280 analogue cable connection signals to the outside DAQ system [2]. This thesis addresses the technology and engineering challenges of future designs that implement the signal digitisation on-cold, where the SiPM sensor pulse is processed and digitised by CMOS integrated electronics working at cryogenic temperature. The digital data payload generated by the cold photoelectronics module can be further multiplexed and serialised, thereby reducing the number of fibers required for data transmission.

Two different approaches can be evaluated. The first case is based on cryogenic ADC [85], where a high resolution converter is placed after the analogue readout circuit and waveform digitisation is performed. In this case, the ADC must ensure a sampling rate high enough to allow signal analysis in the warm environment. Therefore, the DAQ system must be designed accordingly to the ADC in order to sustain the output data rate.

This work assumes that, using a more aggressive pixelisation of the photosensor, a simpler readout circuit based on event-discriminator and Time to Digital Converter (TDC) can be employed to perform a single-photon timestamping of the arrival time and charge information of the event detected by SiPMs. In this way, signal digitisation can be brought into the cold volume without the need of complex large dynamic range ADCs. Moreover this solution allows to reduce the single channel readout area, thereby reducing the sensor capacitance at the input of each front-end amplifier. As a consequence, from a system-level perspective, the same signal-to-noise ratio can be achieved with lower current per front-end channel, maintaining the overall power dissipation comparable to that required in solutions adopting analogue summing of SiPM signals. The output data rate is reduced to transmitting only relevant information of the detected event. This solution also reduces dramatically the complexity of the DAQ system, where a simpler FPGA is enough.

State of art of ASICs employing single-photon detection technique are showed and discussed in Section 2.2, in particular readout ASICs for analogue and digital SiPM. In Chapter 3 the design of a first prototype suitable for cryogenic SiPM readout is presented.

Chapter 2

Advanced readout concepts for photon detectors

Silicon Photomultiplier (SiPM) [26, 38] are solid-state light sensors which robustness, compactness and compatibility with magnetic field, high photodetection efficiency and gain make them strong candidates for a wide range of applications and detectors in the fields of high-energy physics [72], medical imaging [73, 15, 80], dark matter detection experiment [42, 23] or automotive [10].

In this chapter a brief introduction of SiPM working principle is given and examples of read-out architectures are presented.

2.1 Silicon photomultipliers

SiPMs are solid-state devices based on two dimensional arrays of 100 to several 10000 Single-Photon Avalanche Diodes (SPADs) with typical dimensions between $10 \times 10\ \mu m^2$ and $100 \times 100\ \mu m^2$ [64]. The single SPAD is a photo-diode based on a silicon junction that is biased beyond the breakdown voltage and operates in Geiger mode.

A photon absorbed in the depletion region of the SPAD generates an electron-hole pair. These charge carriers thanks to the high electric field applied to the diode, initiates the so called impact ionization effect[1] that produces other electron-hole pairs. Thus, an avalanche of charge carriers cross the SPAD generating a signal from a single photon. The bias voltage of the SPAD must be quenched in order to be able to detect another photon. The schematic circuit of SiPM is depicted in Figure 2.1. The single SPAD cell is defined by the sensitive area where the photons are absorbed and by the quenching resistors.

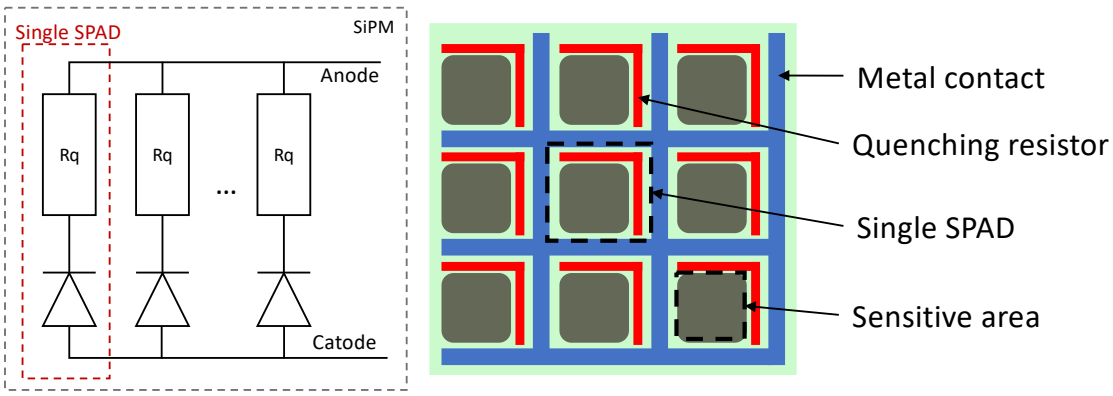


Figure 2.1: Electric model of SPAD on the right. On the left the time response of the circuit.

The signal generated by the SPAD cell is always independent of the number of photons that have been absorbed. Therefore, each SPAD generate the signal of a single photon (1 Photon Electron (PE)). Figure 2.2 depicts an equivalent circuit model of a SPAD and the pulse shape in time delivered by this circuit. The capacitor C_j is the SPAD

[1]Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other electron-hole pairs.

diode, R_s is the series resistance, R_q is the quenching resistance and V_{br} is the breakdown voltage, where V_{bias} is greater than V_{br}.

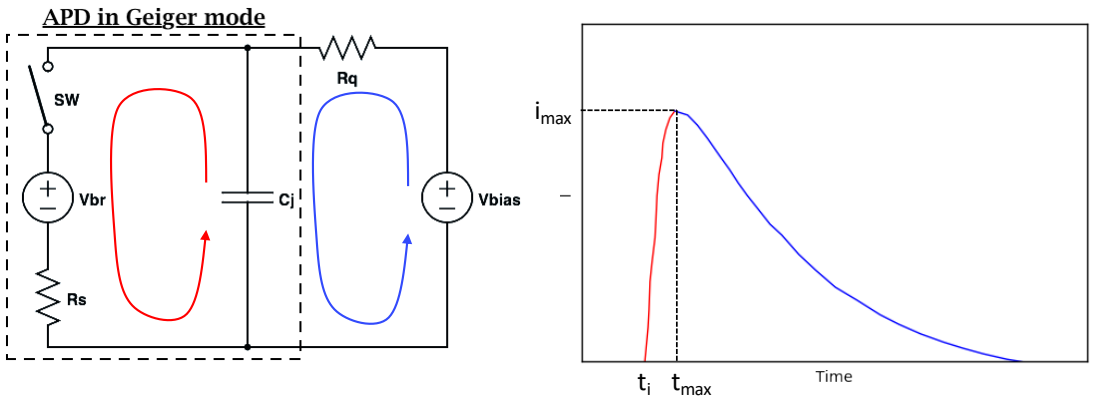


Figure 2.2: Electric model of SPAD on the right. On the left the time response of the circuit.

Closing the switch SW simulates the detection of a photon and the avalanche signal through the C_j capacitance is generated with a fast component according to Equation 2.1. When the switch SW is open, the diode is recharging in the slow component according to the Equation 2.2. Therefore, the output signal is characterised by two components, a fast and sharp signal, followed by a slow and long tail. This tail is primarily due to the recharge that flows through the quenching resistor. The maximum amplitude, which is the signal of 1 PE, is proportional to the over-voltage applied to the circuit as defined in Equation 2.3.

$$i_{fast}(t) = 1 - e^{(\frac{-t}{RsCj})} \tag{2.1}$$

$$i_{slow}(t) = e^{(\frac{-t}{RqCj})} \tag{2.2}$$

$$i_{max} = \frac{Vbias - Vbr}{Rq + Rs} \tag{2.3}$$

The gain value of the SPAD gives the amount of carriers flowing during the avalanche phase. Considering the electrical model in Figure 2.2 is it possible to define the gain value as:

$$Gain = \frac{(Vbias - Vbr)\, Cj}{q0} \tag{2.4}$$

Where *q0* is the electron charge of $1.602 \cdot 10^{-19}$ C, the voltage difference *Vbias-Vbr* gives the over-voltage applied to the SPAD cell and *Cj* is the diode capacitance. Typically, the gain value is in the order of 10^6 thus generating a well defined photon pulse above the noise level. Attention must be paid to the *Vbias* voltage that may change over temperature, while *Cj* is proportional to the size of the SPAD diode. A bigger cell gives a higher gain and a better photon number resolution, but it is slower to recharge. The well-defined gain gives the analogue SiPM very good photon number resolving capabilities, which can be estimated by the amplitude spectrum. SiPMs with large areas generate typically smaller signal amplitude due to the bigger grid capacitance and parasitics capacitance on the long interconnections between the sensor and the bonding pads that act as a low pass filter on the output signal.

2.1.1 Photon detection efficiency

Photon Detection Efficiency (PDE) defines the probability of a SiPM to detect a photon and can be expressed as the ratio between the number of photons detected and the total number of photons impinging on the detector:

$$PDE = \frac{N_{ph\_detected}}{N_{ph\_arrived}} = QE \cdot P_{Trig} \cdot FF \tag{2.5}$$

Where QE is the quantum efficiency of photoelectron conversion, P_{Trig} is the avalanche triggering probability and FF is the fill factor of the pixel. The QE is the probability a photon generates an electron-hole pair once it falls in the sensitive area of the SPAD. This depends on the reflectivity of the silicon surface and if it has been coated with an anti-reflection material. The P_{Trig} is the probability to generate an avalanche later a charge carrier. In silicon this parameter is associate to the ionization coefficient which increases by electric field, and it is higher for electrons rather than for holes. The fill factor depends on the geometry of the single SPAD, and can be expressed as the ratio between the sensitive area over the total area of the sensor. This value increases with the cell size. Combining the doping profiles for the p/n junction and the absorption

depth in silicon, it is possible to develop different flavours of SiPMs depending on the wavelength of photons [6, 60, 65].

The Single Photon Time Resolution (SPTR) is one of the important parameters that define a SiPM. This value includes the timing jitter of the detector. The SPTR is important parameter that defines the maximum resolution achievable in Time-of-Flight measurements Time-of-Flight (ToF) in high energy physics and medical application or low-light detection experiments. Normally this parameter assumes a value in the range of 180 $ps - 50\ ps$ depending on the sensor size. [5].

SiPMs can be designed in an analogue or digital fashion way[36, 69, 86, 54]. Both solutions allows to count and detect events with good sensitivity and time resolution in the order of picoseconds [43].

2.1.2 Dark Count, After-Pulsing and Cross-Talk

The SiPM is affected by dark noise pulses that are a production of spontaneous Geiger discharge in a SPAD in absence of photon detection. Figure 2.3 depicts a cross-section of an SiPM and shows how different dark noise source can be present inside the sensor.

The primary noise in an SiPM is identified as Dark Count Rate (DCR) and it happens when a SPAD spontaneously generates an avalanche from free charged carriers. This type of noise follows a Poisson distribution, and the generated output signal is very similar to a photon generated pulse. This noise is essentially a consequence of a thermal effect that increases with the temperature. The presence of trap levels in the band gap introduced by crystal impurities facilitates the thermal generation. This effect is well described by the Shockley-Read-Hall generation–recombination model[74]. At low temperature, the band-to-band tunnelling effect is dominant, and it is intensified in the presence of a strong electric field, since the P_{Trig} probability increases proportional to the excess bias voltage. The DCR can be dominant in application with low intensity photon detection, limiting the timing performance of the overall system.

The noise pulses generated after a primary avalanche gives rise to correlated noises [39, 4]. The first case is the After-Pulsing (AP) and it happens when a carrier remains trapped in some impurities of silicon during the primary avalanche. When the carrier is released after a certain amount of time, it generates a second avalanche. The AP

amplitude can be equal to 1 PE or lower depending on when the second avalanche occurs, if after or during the quenching phase of the primary avalanche. The probability to generate an AP can be calculate as:

$$P_{AP}(t) = P_{TC}\frac{e^{-t/t_{lt}}}{t_{lt}}P_{Trig} \tag{2.6}$$

WhereP_{TC} is the trap capture probability, which depends on the presence of impurities in the silicon and on the gain of the sensor, t_{lt} is the trap life time, which depends on the energy level of the trap in the band gap, and P_{Trig} is the trigger probability. The P_{TC} and P_{Trig} increase linearly with the over-voltage, therefore the AP probability increases quadratically with the excess bias.

Another case of correlated noise is the Cross-Talk (CT) event that occurs when an avalanche generated in a SPAD triggers avalanches in the neighbouring cells. The SiPM output generated by this phenomenon has amplitude equal to 1 PE or higher depending on how many SPAD have been activated. There are two different categories of CT. If the signal occurs at the same time of the primary pulse is the case of Direct Cross-Talk (DiCT), while if the signal occurs with a delay with respect to the primary pulse, it is called Delayed Cross-Talk (DeCT).

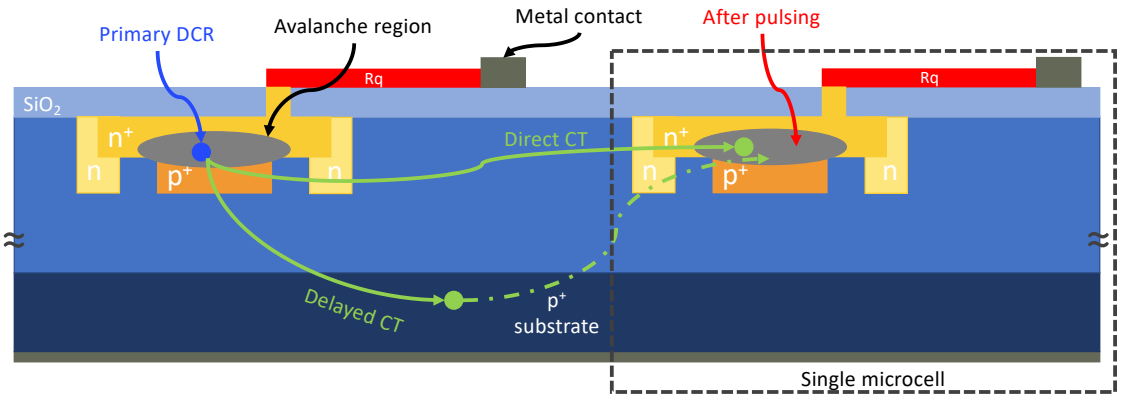


Figure 2.3: SiPM cross-section showing different dark noises: After-pulsing, Dark count rate, Direct and Delayed Cross-Talk.

In Figure 2.4 the dark noise measured in a RGB-HD-HRq SiPM developed by FBK [1] is reported. Each point represents the peak amplitude of an event, normalized to the height of the single-cell signal, as a function of the time distance from the previous event. In the plot, dark noise pulses are grouped depending on the time and amplitude. The primary DCR with 1 PE amplitude follows a Poisson distribution. The majority of AP is distributed in an amplitude between 0.5 PE and 1 PE with a time interval between 50 ns and 200 ns from the first event. The DiCT cross-talk effect has the same time distribution as the primary DCR but with amplitudes higher than 1 PE. While, DeCT occurs very close in time to the first event in a time interval between 5 ns to 20 ns.

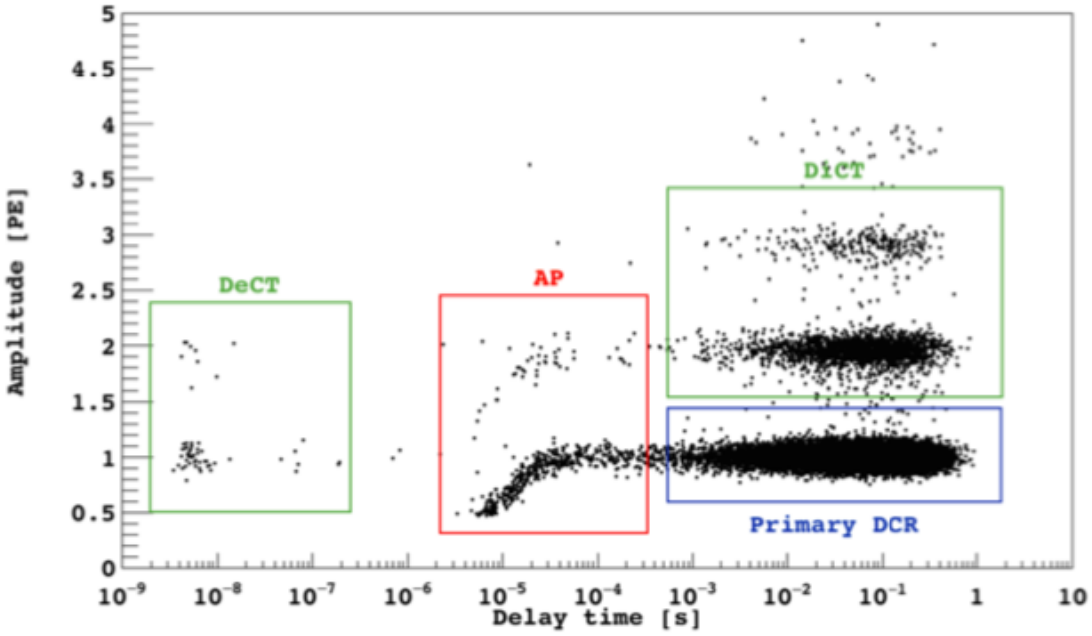


Figure 2.4: Distribution of peak amplitude versus time since last event for an RGB-HD-HRq SiPM operating at 40 K and 4 V of over-voltage in the absence of light. It is possible to identify the different noise components of the SiPM response described in the text: DCR, DiCT, DeCT and AP.

2.2 Analogue SiPMs

In the analogue SiPM type, each SPAD is connected in parallel via passive quenching resistor to a common readout, and the SiPM provides the current sum of the single Geiger discharge pulse. Figure 2.5 shows the schematic diagram of readout architecture of an analogue SiPM, where the sensor is connected to an external ASIC embedding discriminator and/or integrator. The performance of analogue SiPMs is affected by the parasitic capacitance of the long interconnection between the cells and the bonding pads, which degrades the performance of the sensor. Besides, a dedicated readout circuit must be carefully implemented in order to digitise the analogue SiPM pulse. Since the output is in the mV range, the single photon detection could be difficult because the pulse can be easily affected by electronic noise.

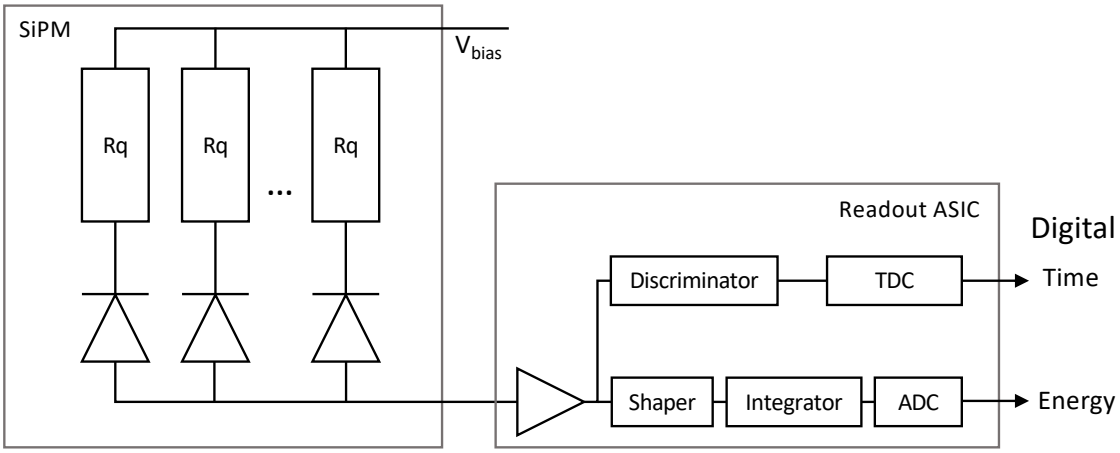


Figure 2.5: Schematic block of an analogue SiPM readout.

The Front-End (FE) electronics used to readout SiPM sensor must preserve the fast rising edge of the pulse generated from the detector in order to obtain a good time measurement. In case of SiPM sensors, the amplifier implemented in the FE have to deal with large load capacitance and high bandwidth, therefore the classic Charge Sensitive Amplifier (CSA) commonly used in a radiation detector cannot be implemented. The feedback capacitance employed in the CSA must be in the range of pF in order to deal with the gain of theSiPM sensor, which is not very practical in a multichannel readout IC implemented in standard CMOS technologies. Moreover, due to the fast leading edge of the pulse signal, after the CSA a faster shaper is needed, able to reconstruct

the fast signal component to be forwarded then to the discriminator. In less demanding applications where there is a low gain sensor, low total input capacitance and less stringent timing accuracy, the readout based on CSA can be a good solution due to its very good noise performance. In case of time measurement, the readout circuits are based on Leading Edge Discriminator (LED) where the rms of the detected time (σ_{time_event}) depends on the slope of the output signal of the FE and the threshold value as shown in the following equation:

$$\sigma_{time\_event} = \frac{\sigma_{FE}}{\frac{dVout}{dt}\,|_{Vout=Vth}} \tag{2.7}$$

Where σ_{FE} is the rms output noise of the FE electronics. In the next section different approaches of readout will be showed and discussed for both energy and time measurement.

2.2.1 TIA

The most common approach to readout SiPMs is to implement a Transimpedance Amplifier (TIA). This circuit is a current to voltage converter, and it is implemented using one or more operational amplifiers. Figure 2.6 depicts an example of this circuit coupled to an SiPM sensor. Large bandwidth may allow to preserve the fast rise time of the SiPM pulse and to obtain hence a good time measurement. A stability problem may occur in case of high capacitance of the sensor, that combined with the feedback resistor (R_F) introduces a low frequency pole at the amplifier. This problem can be mitigated by inserting a compensation capacitance in parallel to the resistor, limiting the close loop bandwidth and therefore reducing the timing accuracy of the circuit. Energy information can also be extrapolated from the TIA output signal using an integrator based on an active filter which requires a voltage to current conversion.

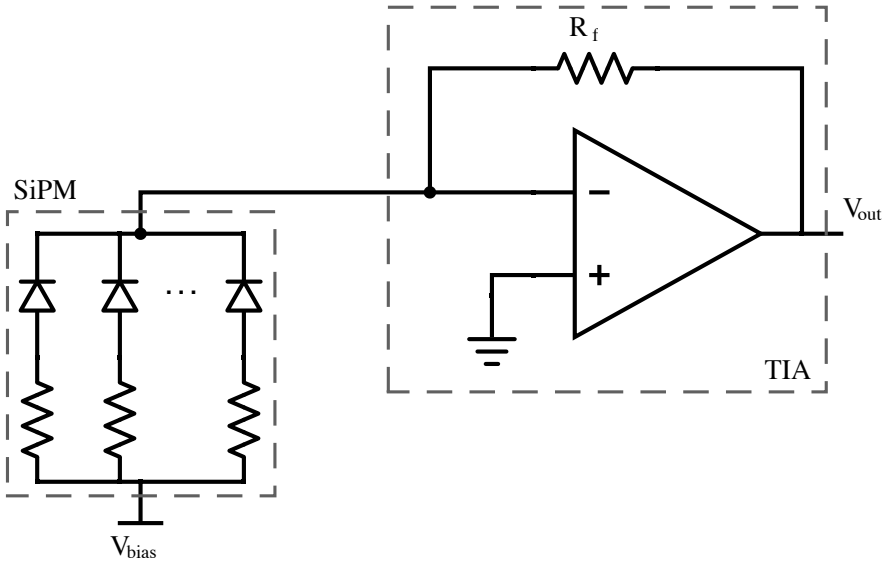


Figure 2.6: Example of Transimpedance amplifier coupled with SiPM sensor.

2.2.2 Voltage mode

The voltage mode readout implements a voltage amplifier as showed in Figure 2.7, where the amplified output is forwarded to an integrator for energy measurement and to a comparator for time measurement. In order to obtain a good timing performance, also in this circuit, the fast rise slope must be preserved at the output of the amplifier. Therefore, large bandwidth must be ensured by the FE. The R_{IN} resistance showed in the schematic has an important impact on the output signal of the SiPM. High value of this resistance slows the tail of the pulse reducing the event rate sustainable by the sensor and inducing possible pile-up effects. While a lower value of R_{IN} allows a faster discharging of the pulse and improves timing resolution limiting the baseline variation. The gain of the amplifier must be designed large enough to be processed by the integrator and comparator. This kind of circuit is not effective in application where low level light must be detected, since in order to obtain a large gain, it needs large power consumptions. In case of a large dynamic range of the input signal, a voltage mode solution can be applied. ASICs that implemented voltage mode readout are SPIROC [16], EASIROC [19] and PETA[34].

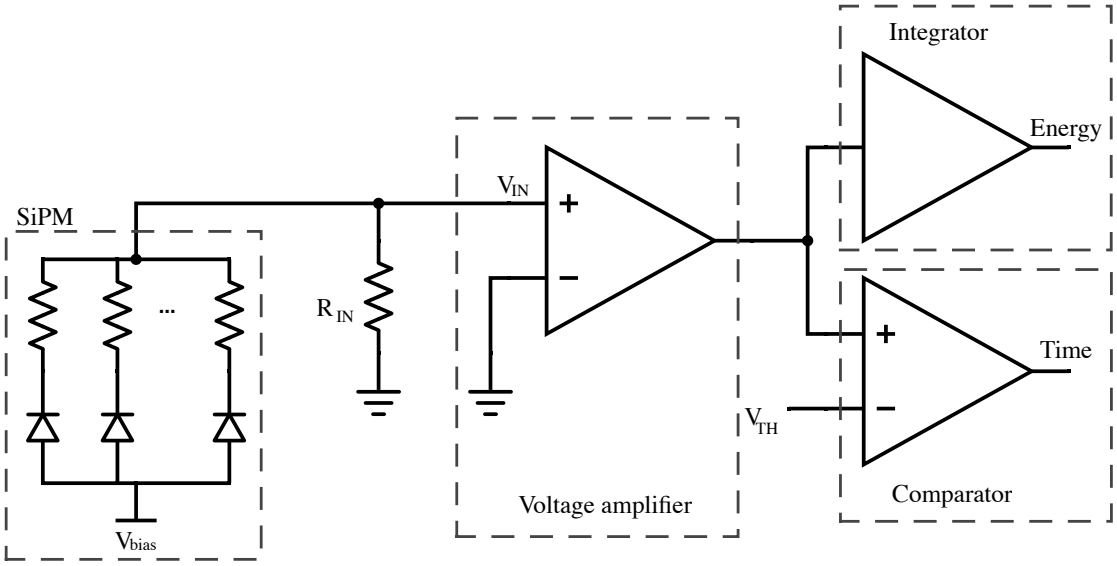


Figure 2.7: Example of voltage mode readout, using an integrator for energy measurament and comparator for time measurament.

2.2.3 Current mode

The most common solution to readout SiPM detectors are based on current mode preamplifiers. Figure 2.8 reports an example of a schematic using this readout mode. The output signal of the buffer is a high impedance replica of the sensor signal that can be reproduced with different scaling factors: K_1 for the fast component of the pulse that will be used to determine the time measurement and K_2 for the slow component that will be used for energy measurement. Using current mode amplifier gives the advantage in terms of time measurement thanks to the large bandwidths that can be achieved due to the absence of high impedance nodes. A major drawback of this approach is given by the bias current source that reduces the output dynamic range of the common gate amplifier. The NINO [61, 9] ASIC is implemented with a current mode amplifier.

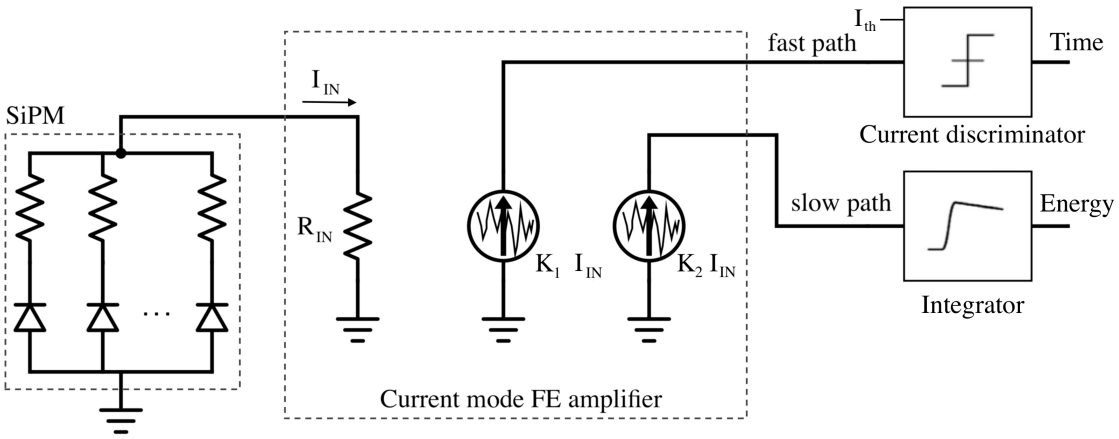


Figure 2.8: Example of current mode readout, using an integrator for energy measurement and comparator for time measurement.

The regulated common gate transimpedance amplifier is one of the most used circuit to reduce the input resistance of the preamplifier $1/g_{m1}$ of a factor equal to the loop gain of the applied feedback $g_{m2}R_2$. This loop feedback allows to find a good trade-off between low R_{IN}, power consumption and noise. Since the main noise contribution is given by the current of M_2, the output noise can be reduced increasing g_{m2} with respect to g_{m1}. An example of regulated common gate amplifier can be found in TOFPET2 ASIC [37].

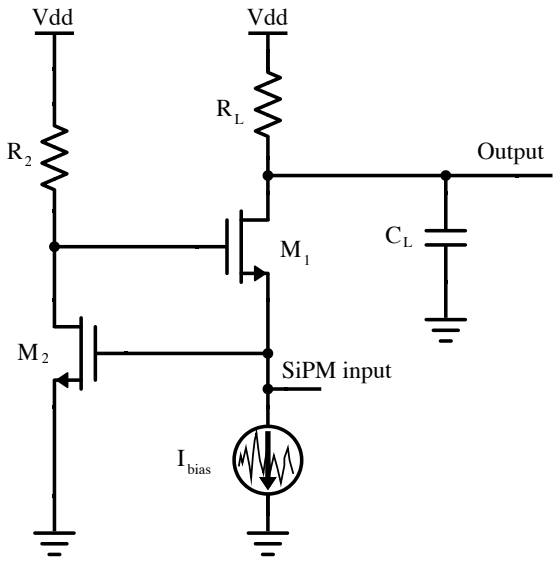


Figure 2.9: Example of regulated common gate circuit.

2.2.4 Energy measurements

The energy measurement of an event is information that can be extracted from the SiPM pulse and depends on the charge associated with the signal. The simplest way is to perform integration of the current pulse of the sensor. Depending on the type of preamplifier, there are different circuits. In voltage mode FEs the integration measurement can be done by means of a slow shaper cascaded to the preamplifier. This circuit is implemented with a passive RC network or with an active filter. Depending on the application requirement, the shaping time can be between 25 ns to 200 ns. In case of a Silicon Photomultiplier (SiPM) current pulse with a long tail, the peaking time of the shaper must be long enough in order to integrate the full input signal. In current mode FE the integration measurement of the current signal is performed by means of passive RC network. Other solution use CSA without resistive feedback and performs integration in a chosen time window. There is energy that has to be measured, therefore a peak detection circuit may be implemented in order to find and store the peak voltage of the integrator in both current and voltage mode FE the peak of the integrator output. An ADC can also be implemented at the output of the integrator in order to digitise the information and transfer it easily to the outside electronics.

In applications where the linearity of the energy measurement is not of interest, it is possible to evaluate the information presented during a Time-over-Threshold (ToT) measurement. The charge generated by the sensor is associated to the time duration of the pulse over the threshold of a discriminator. In some case two thresholds are used, the first one very low in order to obtain a good timing of the fast component of the pulse, while the second threshold is higher in order to improve the energy resolution. The energy measurement obtained with this method is accomplished from time measurements using Time to Digital Converter (TDC), which means that the same circuitry can also be used to both time and energy evaluation. The Figure 2.10 depicts an example of ToT technique, where the time over threshold duration is proportional to the amplitude of the input signal. There are approaches that improve the ToT accuracy. In this case, the output pulse of the FE is stored in an integrator capacitor in a fixed time window, and then with a constant current the capacitor is discharged in a time proportional to the integrated charge.

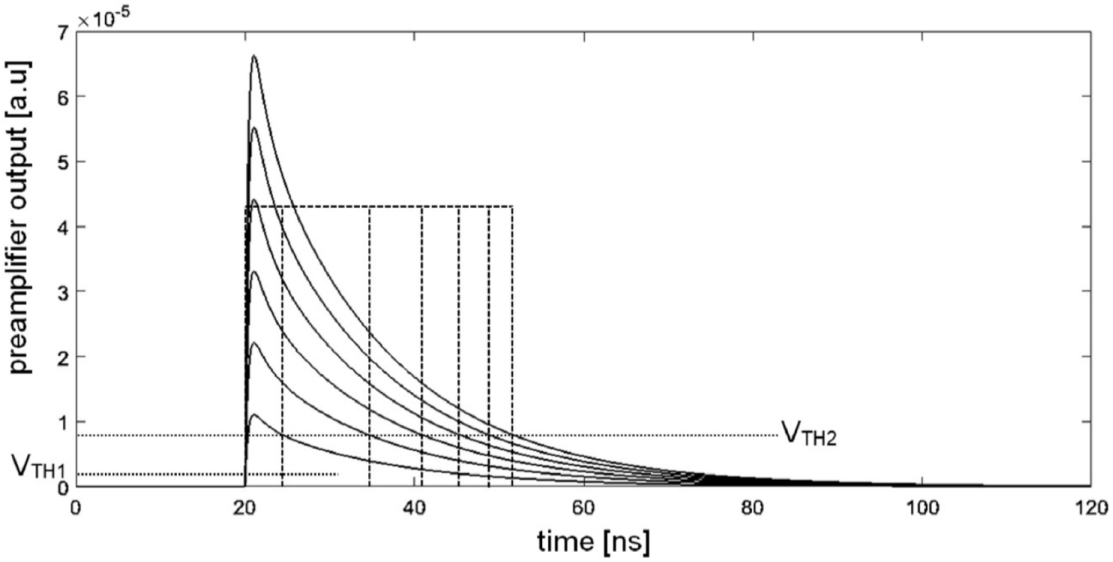


Figure 2.10: Time-over-threshold technique for energy measurement [20].

2.2.5 Time measurement

In applications where the arrival time of the event is particularly relevant, the current signal from SiPM sensor must be properly amplified and shaped in order to maintain the step rising edge of the signal. This implies high bandwidth of the FE and low electronic noises. One of the most used time pick-off methods is Leading Edge Discriminator (LED) technique, where a fast voltage comparator following the preamplifier generates the output signal with a very sharp transition when the FE output goes over the threshold. This trigger signal indicates the arrival time of the event, and thanks to a Time to Digital Converter (TDC) this information is represented into a time-stamp. To avoid triggers due to noise signal, hysteresis may be added to the discriminator as a result of the amount of positive feedback. In current mode FE, the 'fast path' of the amplifier is compared with a current threshold through a current discriminator, avoiding the use of a current-to-voltage converter.

The TDC is used to measure the time difference between two signals with sufficient resolution. The ΔT time period, defined by the *Start* signal and the *Stop* signal, is converted into a digital data format. TDCs can be both analogue and digital based circuit. The first case allows better accuracies to be obtain, while the second case is often preferred due to its flexibility in IC.

Analogue TDC can be based on ramp interpolator circuit which is often used to measure time interval between 10 *ns* and 200 *ns*. A simplified block diagram of this circuit is reported in Figure 2.11. The time difference is converted to an analogue voltage using a ramp generator and a Sample&Hold circuit. After that the amplitude is digitised through an ADC and a timestamp is obtained. The time resolution usually is achievable in the range of 1 *ps* to 10 *ps*. This kind of circuit is simple to be designed and compared with other solution has low power consumption.

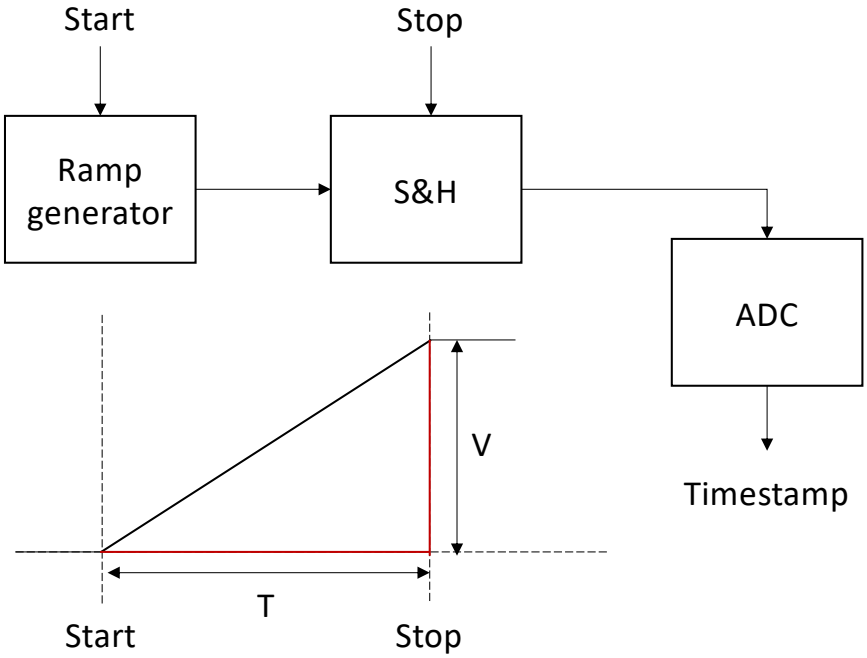


Figure 2.11: Ramp interpolator scheme diagram. The ΔT period is defined by the Start and Stop signals. The ΔV defines the time amplitude to be digitised.

The digital TDC is based on tapped delay line which uses a chain line of D-Flip-Flops (FF)s. An example of this circuit is reported in Figure 2.12. The delay of each cell is well defined and it is equal to all cells. When the *Start* signal arrives, it is propagated through the line. The *Stop* signal is used to latch all D-FFs. The input signal is sampled at each cell and a bit output is generated. The count of bits at logic-1 defines the ΔT time interval between the *Start* signal and *Stop* signal. The delay of each D-FF may be affected by skew during the production phase. Therefore, this kind of circuit must be carefully designed in order to respect the timing constraints and obtain a good linearity.

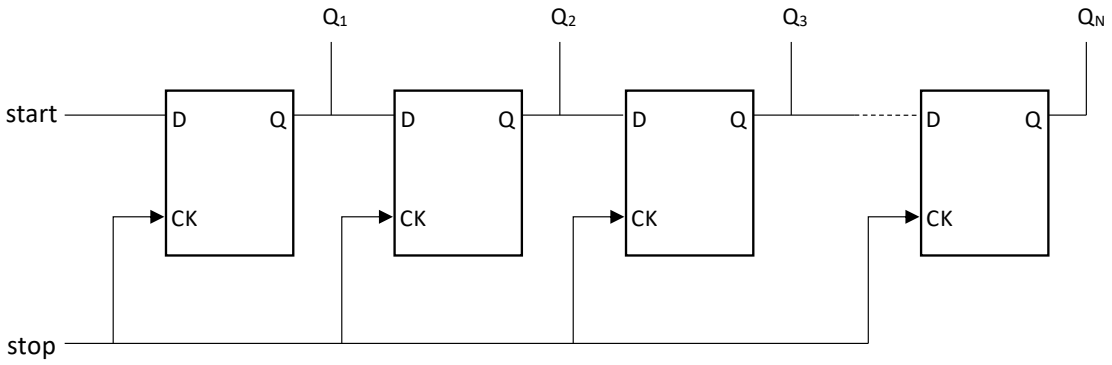


Figure 2.12: The tapped delay line uses n D-FF placed in series which each component has a well defined time delay. The Start signal is delayed through the line and when the Stop signal arrives samples the Q_N output.

One of the main issue related to LED solution is the time walk, where the trigger output signal depends on the rising time of the pulse giving an accurate arrival time. The Constant Fraction Discrimination (CFD) circuit solves this problem where essentially eliminates amplitude-depended time walk for signals having consistent rise times [68]. The Figure 2.13 depicts two pulses with the same shape and time. In the left case, the time is detected when the signal overcomes the threshold. While in the right case, the time is detected using a CFD discriminator circuit.

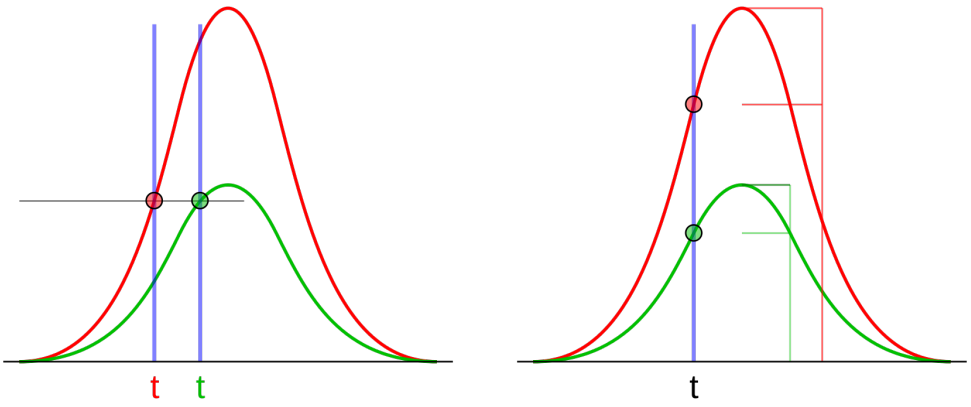


Figure 2.13: The different signal amplitude overcome the threshold at two different time. The CFD generates the same arrival time independently by the signal amplitude. [32].

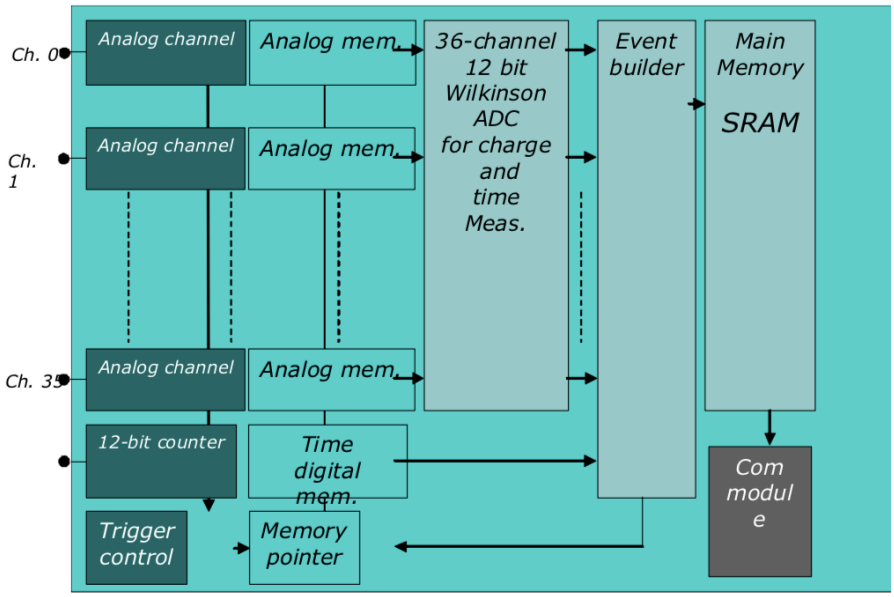
The long tail of SiPM dark pulses may cause fluctuation of the baseline inducing a

bad time resolution of a good event when overcome the threshold of the discriminator. The Differential Leading Edge Discriminator (DLED) technique solves this kind problem compensating the tail of the SiPM signal through pole-zero cancellation filters. The rise time of the SiPM signal is not affected by this fast return to zero, but as major drawback the electronic noise is increased by the contribution of this filter. The time constant of the zero must be tuned depending on SiPM sensor.

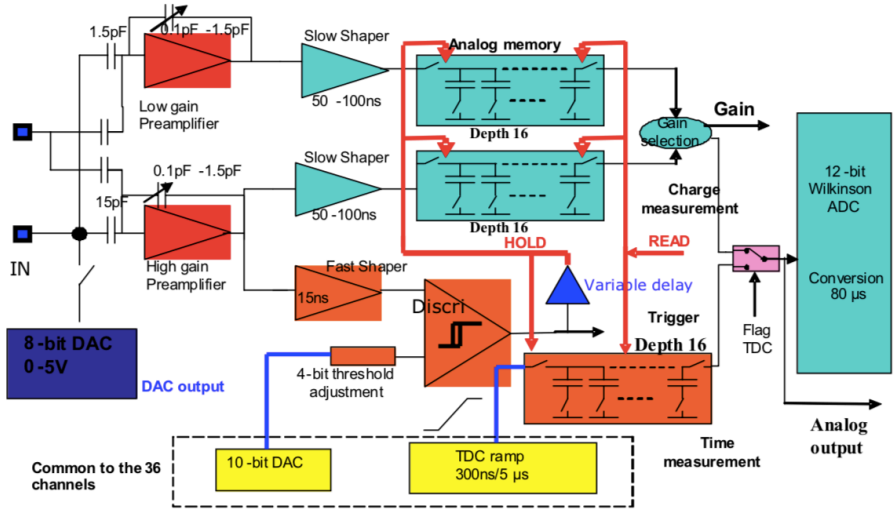
A very good time resolution can be obtained using a Switched Capacitor Array (SCA) [67]. The SiPM signal is propagated through a ring oscillator, made by a chain of inverter, while capacitors are used to store temporarily the analogue signal which is then converted using an ADC.

2.2.6 SPIROC2

The SiPM Integrated Read-Out Chip (SPIROC) is a chip developed for International Linear Collider prototype hadronic calorimeter [51]. This ASIC is designed in $0.35 \mu m$ technology and occupies an area of $7.2\ mm \times 4.2\ mm$ for total power consumption of $25\ \mu W$ per channel. This chip is designed with 36-channel input front end circuits where each of them includes two variable preamplifiers that allows to manage a dynamic range between 1 to 2000 photoelectrons, then two variable $CRRC_2$ slow shaper and two 16-deep Switched Capacitor Array (SCA) are used to store the analogue time when a trigger occurs. The time resolution that is able to achieve is $1\ ns$. The ADC conversion is performed using a 12-bit Wilkinson converter. The discriminator threshold voltage is programmed coarsely through a 10-bit DAC common for all channels and then is tuned finely in each channel using a 4-bit DAC. Figure 2.14 reports the schematic diagram of the full chip and a schematic diagram of the single channel. The readout is processed in three different steps. The first one is the acquisition phase where a valid event is stored in an analogue memory, while the time measurement is stored in a coarse digital memory and a fine analogue memory. Then, there is a conversion phase where the stored data is converted for each column and stored in a memory in order to free the logic for a new event. The last phase concerns the readout. In this phase, all the converted data are read in a daisy chain fashion from Ch0 to Ch35, and they are sent to a DAQ system.



(a)



(b)

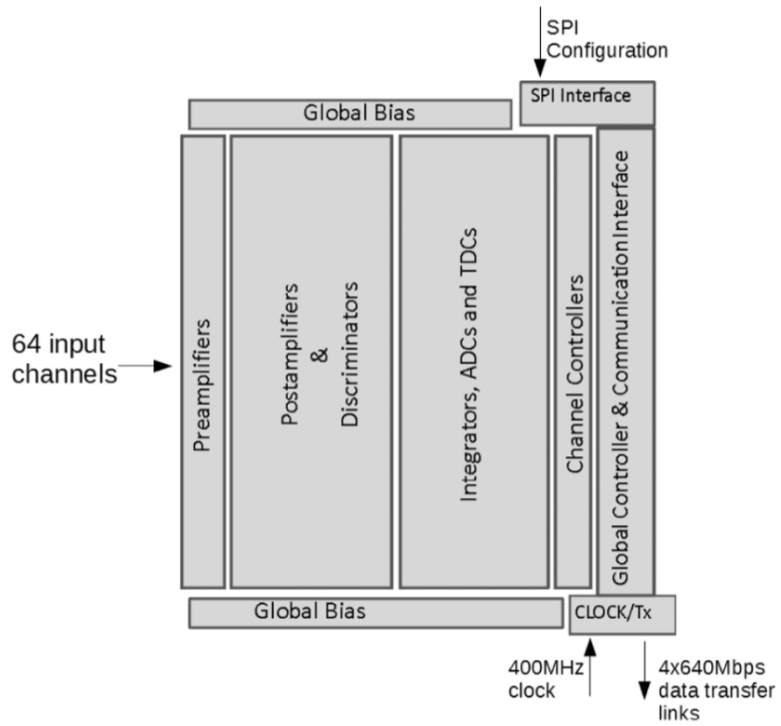
Figure 2.14: Schematic diagram of SPIROC ASIC, full chip (a) and single channel (b) [16].

2.2.7 TOFPET2

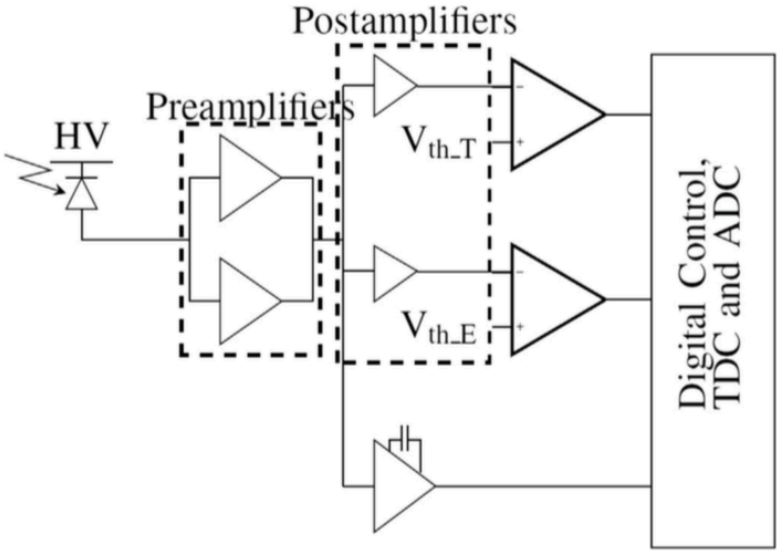
The TOFPET2 is an ASIC, developed in CMOS 110 nm technology. The chip is designed for Time-of-Flight (ToF) measurement in PET applications [18] and it is optimized to provide digital information of the energy and ToA of the detected event. The system clock frequency is set to 320 MHz allowing a 640 $Mbps$ of data transmission through LVDS link drivers. The chip also works at 400 MHz clock frequency in order to improve resolution for the digitisation. TOFPET2 is designed with 64 channels and a schematic diagram of the full chip and of the single channel is reported in Figure 2.15.

The single channel performs timing measurement based on threshold detection using a fast discriminator. The threshold can be programmable in the range $0 - 300$ mV with a maximum resolution of 2.5 mV. Then two discriminators are used to minimise background events. The first threshold can be set in the range of $0 - 600$ mV to reject dark counts, while the second threshold is used to suppress low energy events with a maximum value of 250 keV. The ToA is digitised using a dual ramp Time to Digital Converter (TDC) that allows a time binning of 30 ps. The time information is first stored in an analogue buffer of four capacitors, and then it is converted using a Wilkinson ADC. The energy measurement is performed through a QDC. The same capacitors used for timing conversion are used to integrate the input charge, and the digital information is obtained with the second Wilkinson ADC. The maximum dynamic range is 0 pC to 1500 pC with a resolution of 8 pC. However, thanks to digital configuration, it is possible to achieve a better resolution of 6 pC for a reduced dynamic range of 0 pC tp 1100 pC.

The TOFPET2 ASIC uses a dedicated DAQ to readout digitised data. The chip is configured using SPI interface connected to an FPGA.



(a)



(b)

Figure 2.15: Schematic diagram of TOFPET2 ASIC, full chip (a) and single channel (b) [18].

2.3 Digital SiPMs

In parallel to the analogue SiPM, there is a line of research that studies the possibility of integrating the SPAD, recharge, quenching and digital readout in the same microcell. This device is named a digital SiPM. In this type of sensors, each SPAD is connected to its own active quenching resistor and readout circuit. This type of sensor has a unique feature that allows to target a single SPAD and turn off cells that have high dark count rate. Figure 2.16 depicts the architecture of a dSiPM, where the single SPAD generates a digital trigger that can be used to feed a photon counter for energy measurement or it can be used to perform time measurement through a Time to Digital Converter (TDC). This solution has the advantage to reduce the distance between the sensor and electronics, eliminating the SPAD to output timing skew at the high output capacitance compared to the analogue SiPM. However this kind of solution is still limited in several aspects. The readout electronics occupies a not negligible area that reduces the fill factor of the SiPM sensor to $50\% - 80\%$, obtaining thus a lower PDE. Furthermore, the digital SiPM is developed using CMOS technologies, for which the impurities and defect of fabrication process may increase the DCR of the sensor. The digital SiPM has the advantage to integrate the bias voltage on the same die, and combined with a direct breakdown voltage measurement completely compensate for the temperature dependencies of the PDE of the sensor.

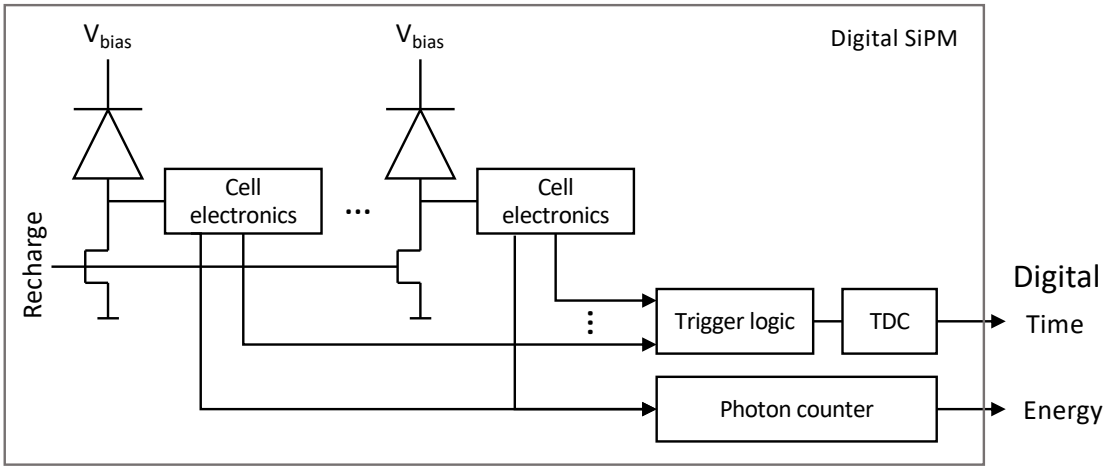


Figure 2.16: Schematic block of a digital SiPM readout.

2.3.1 Philips Digital Photon Counter

The Philips Digital Photon Counter (PDPC) DPC3200-22 is a digital photon counter that is developed employing 2×2 pixel arrays for a total of 3200 micro-cells. The Time to Digital Converter (TDC) and acquisition controller is shared among the four SPADs as depicted in the schematic block diagram in Figure2.17. The acquisition phase starts when an event is detected in any of SPAD cell, and the control logic generates a digital data packet containing the photon counts and the timestamp of the trigger signal.

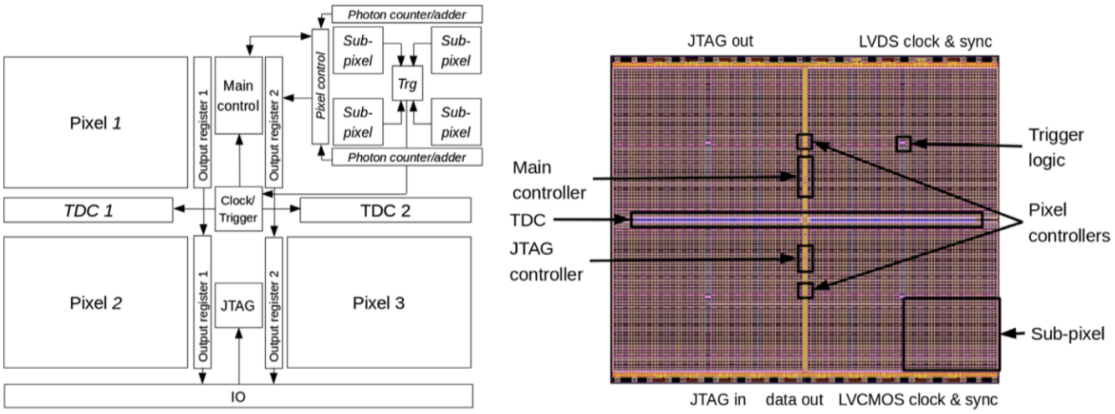


Figure 2.17: On the left the DPC3200-22 digital SiPM block diagram. On the right the layout diagram of the sensor [35].

The micro-cells consist of a group of two SPAD of $55.66\mu m \times 64\mu m$ sharing the same electronics, in order to increase the fill factor of the cell. The FF of the single SPAD cell is 82.9%, while the FF of the micro-cell is 77.7$. The electronics embeds the active quenching resistor and recharge unit, a 1-bit memory to turn ON/OFF the cell, the trigger network and data line drivers for photon counting. All the trigger generated in micro-cells are grouped first in a sub-pixel trigger and then in a pixel trigger.

The TDC start signal is dictated by one of the four pixel trigger, while the stop is generated from a reference clock. The TDC works with clock frequency of 100 MHz allowing a time binning of 23.5 ps. The generated time-stamp is saved in a 9-bit register. In order to avoid metastability problem due to the overlapping of the start and stop signal, there is a second TDC that uses a complementary clock. In this way there is at least one TDC that generates a valid timestamp. Moreover, the two timestamps generated for an event can be used to characterize the TDCs.

2.3.2 SPADnet photosensor

The SPADnet photosensor is a fully digital SiPM fabricated in in 130 *nm* CMOS Image Sensor (CIS) technology, that embeds 8×6 pixels for a chip size of 9.85 *mm* $\times$ 5.45 *mm*, where each pixel comprises 720 SPADs for a dimension of $650.5\mu m \times 517.2\mu m$ with a FF of 42.9%. The full chip operates at 100 MHz clock frequency, and it consumes 120 *mW*. The timestamp is generated at the pixel level employing two 12-bit TDCs that achieve a time binning of 64 *ps* [17]. A picture of this sensor is depicted in Figure 2.18. The top pads are used only for test purposes, while the normal operation of the sensor is verified through the bottom pads.

The SPAD had a DCR lower than 1 $Hz/\mu m^2$ and a PDE over 30% with an over-voltage of 1.4 *V*. The trigger generated from the single cell is grouped in a mini-SiPM trigger used to perform time measurement through two TDCs.

SPAD's trigger inside each mini-SiPM are grouped in a single trigger output which is used to perform time measurement through the two TDCs. The TDCs works in anti-parallel mode in order to guarantee a continuous conversion. The digital data are then transmitted externally through fast I/O circuitry. The data output contains energy and arrival time of the detected event. The characterization of this digital SiPM can be found here [66, 17].

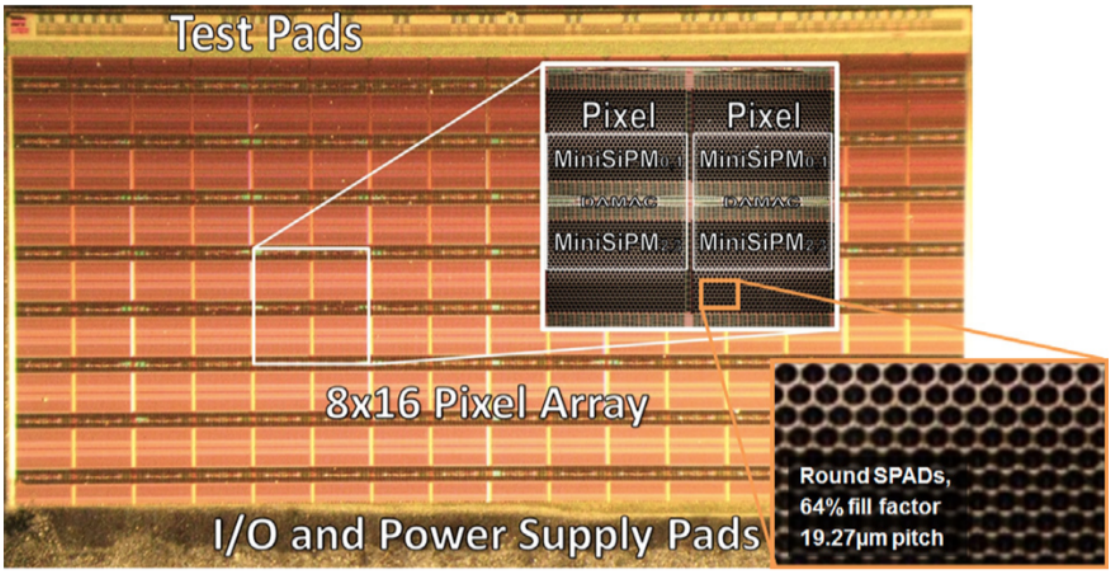


Figure 2.18: Photography of the SPADnet sensor chip [17].

2.3.3 3D-SiPMs

The 3D-SiPM is a type of sensor where the SPAD cell is stacked over the electronic circuit which is designed in CMOS technology. This solution allows to place the electronics readout very close to the photon sensor cell with all the advantages of digital SiPMs but at the same time the SPAD can achieve a very high fill factor. The Figure2.19 depicts the architecture of 3D-SiPM, where the SPAD sensor is connected to the electronic readout circuit Through Silicon Via (TSV). The CMOS chip embeds the Quenching Circuit (QC), the Time to Digital Converter (TDC) and digital readout. The sensor area and the electronics chip must be designed in order to be of compatible size.

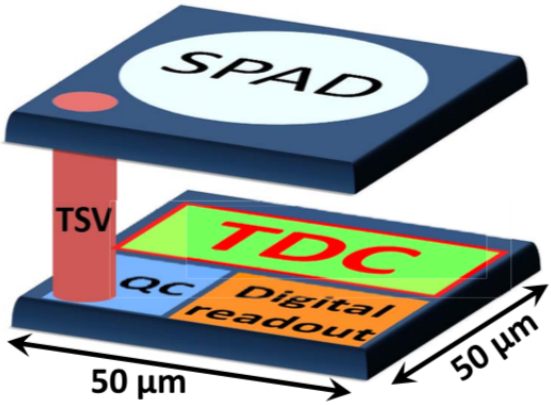


Figure 2.19: 3D-SiPM architecture, the SPAD is connected to the readout electronics through silicon vias (TSV) [71].

A first implementation of the CMOS chip suitable for 3D integration has been fabricated in TSMC 65 *nm* obtaining promising results. The QC is a passive quenching with an active recharge and achieves a 7.8 *ps* FWHM SPTR [57], while the TDC is based on a ring oscillator-based Vernier with a timing jitter of 6.9 ps rms [71]. The first results of a 2D version of a single pixel implemented with the TDC and QC circuits, has obtained a 17.5 ps FWHM SPTR [56]. Figure2.20 depicts the layout picture of this first prototype where each part of the CMOS chip is well marked.

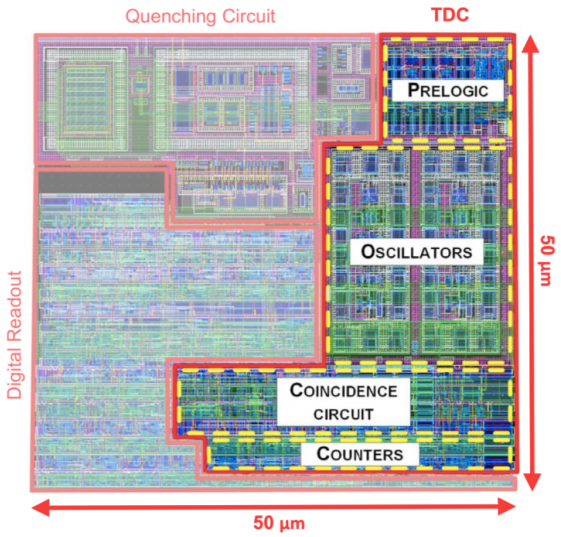


Figure 2.20: Layout of the CMOS chip designed in 65 nm technology.

Following the promising results obtained with a single pixel channel, a full chip implementation of CMOS readout ASIC of 1.1 $mm \times 1.1$ mm, with 256 pixels has been reported in this paper [55]. The arrays are arranged in 16×16 pixels, where each of them has a dimension of 65 $\mu m \times 65$ μm. This size has been chosen in order to fit the electronics circuit and at the same time allows to achieve a good time resolution and FF of the SPAD sensor. Figure2.21 reports a photograph of the ASIC with 256 pixels. Each pixel is implemented to be vertically integrated with SPAD sensors in order to obtain a full 3D-SiPM. The SPAD sensor and 3D integration is under development in a custom technology at Teledyne Dalsa Semiconductor Inc. (TDSI).

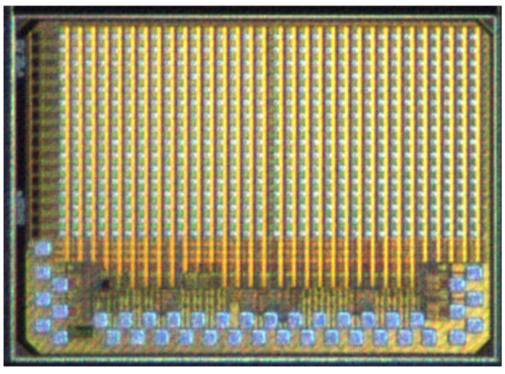


Figure 2.21: ASIC with 256 pixels for 3D SiPM implementation.[55].

In Figure 2.22 is depicted the layout of the single pixel channel, where in yellow is defined the 3D bonding area, in red the QC, in blue the energy counter and in orange the Vernier TDC.

The readout phase can be performed periodically, between 1 μs to 4 ms or on an event-driven basis. In the latter mode, the SPAD cells have an imposed period of time where they can generate a trigger after a photon is detected, events generated from DCR should be minimised. The chip embeds 326 32-bit registers that are used to configure the ASIC and enable or disable each of the pixel's TDC and QDC. The data from each pixel is read in one clock cycle, for a total of 1 μs to readout the full array. The output data is a 64-bit word per pixel and includes the TDC timestamps, global time, pixel address and local energy counter. In case all the 256 SPADs are triggered, the total transmission time to an external FPGA lasts for 69.5 μs at the system clock frequency of 250 MHz.

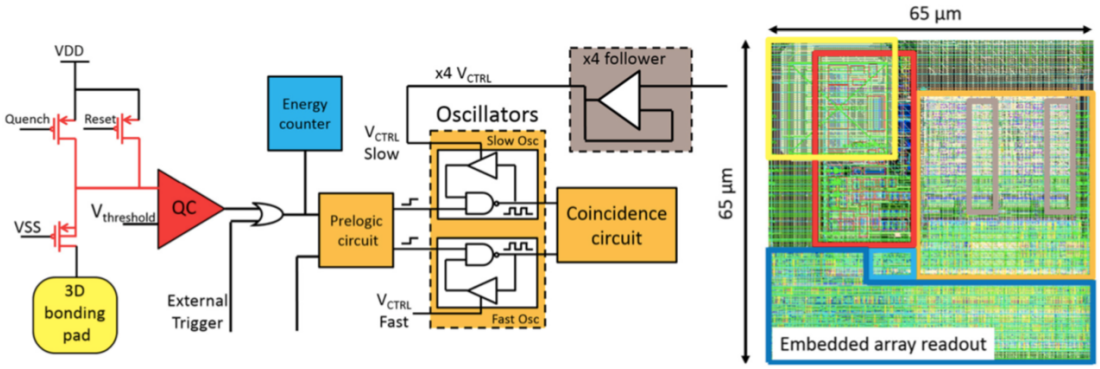


Figure 2.22: Schematic diagram and layout of the single pixel channel. The pixel has a dimension of 65 $\mu m \times 65$ μm [55].

Chapter 3

Design of an innovative low power ASIC for SiPM readout

A Low-power Circuit for Optical Readout (ALCOR) is an ASIC designed to readout SiPMs at cryogenic temperature. The chip is composed by 32 pixels that perform single photon timestamp at the maximum system clock frequency of 320 MHz. The full chip occupies an area of 4.95×3.78 mm^2. While the single pixel has a dimension of 500×500 μm^2 for a total power consumption less than 10 mW. ALCOR will give useful insight on the performance of complex mixed-signal front-ends employed at cryogenic temperature. This chip is a first prototype for a future ASIC to be implemented with 3D-SiPMs. This chapter will describe in details the architecture and the functionality of ALCOR chip.

3.1 Motivation and Specification

A Low-power Circuit for Optical Readout (ALCOR) is a mixed-signal CMOS ASIC for the readout and digitisation of signals produced by SiPMs and optimised for operation at cryogenic temperature. One application for which the chip is envisaged is the readout of new generation photon-detection modules to be used in large dark-matter detectors.

ALCOR has been designed considering the specification of the SiPM sensors employed in the DarkSide-20k (DS-20k) experiment, taken from the paper [2]. The single photo sensor channel reads an area of 25 cm^2 for a maximum photon event of 40000. The Figure 3.1 shows a Python simulation of a S2 signal generated in the DS-20k, which is read from a 24 cm^2 SiPM sensor area. The number of photons is so large that the resulting output signal is a pile-up of events. This pile-up is also caused by the long tail which is generated during the quenching phase of the SPAD sensor. In this way, it is almost impossible to distinguish one PE signal from the others.

ALCOR has been designed to perform single photon detection. In this approach, the SiPM sensor must be segmented into a sufficiently large number of pixels, so that the number of photons impinging on each pixel is small enough to avoid signal pile-up. In this context, given the low expected photon flux, a single pixel can still be a few square millimetres in area. A simple and low-power binary electronics can thus be used to perform single-photon detection and timestamp.

The Figure 3.2 shows a Python simulation in case of the S2 signal is read from a smaller sensor area equal to 1 cm^2. This sensor segmentation is the finest sensor area achievable with DS-20k's SiPMs. It is possible to see that the PE number is decreased enough to perform single photon detection. Considering this simulation result, ALCOR has been designed to readout 1 cm^2 SiPM sensor area for an input capacitance of 5 nF, with a dynamic range between 0.2 pC and 4 pC. Further sensor segmentation allows the input capacitance of the FE to be reduced and thus and consequently to reduce power the power consumption.

ALCOR is the first prototype for cryogenic purpose, and it has been implemented using a 110 nm CMOS process. This technology node has been chosen thanks to its good performance, and allows at low production costs to achieve successfully all the required specification.

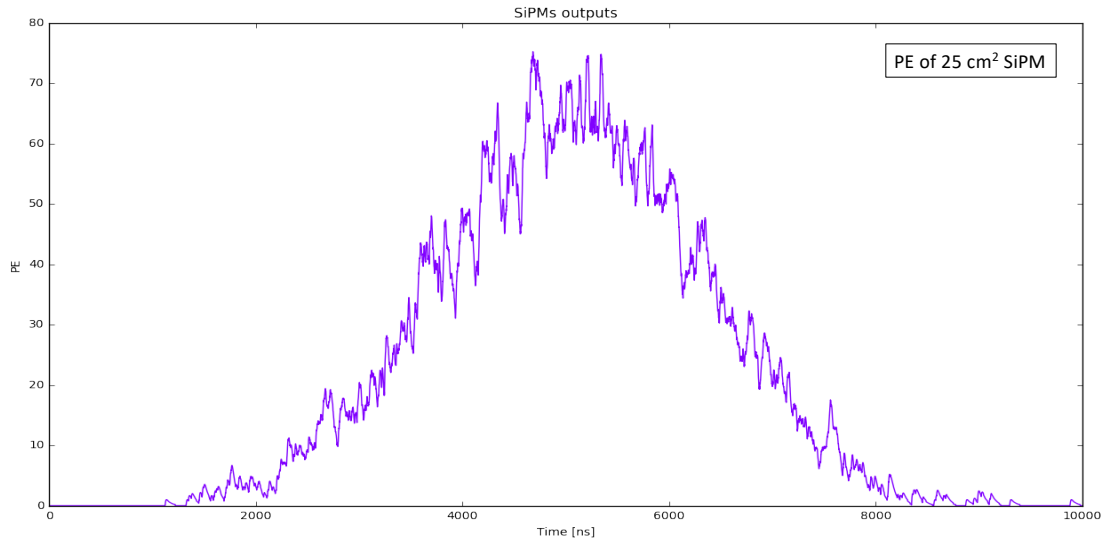


Figure 3.1: Python simulation of PE distribution over a SiPM of 24 cm^2. In this example there are 4000 PE.

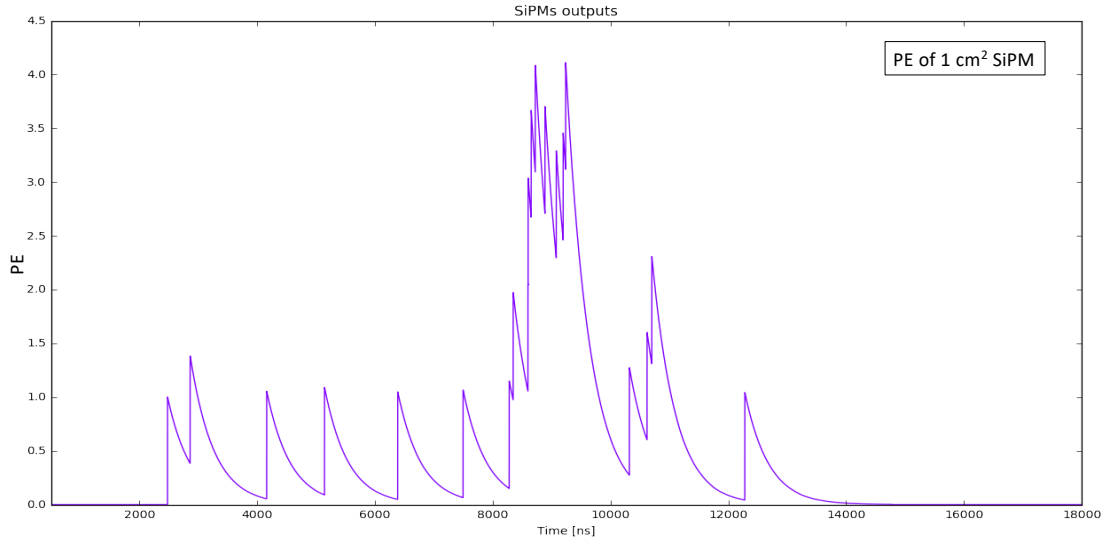


Figure 3.2: Python simulation of photo distribution over a SiPM of 1 cm^2. In this example there are 100 PE.

3.2 ALCOR

ALCOR is designed in a 32-pixels matrix of 8 columns and 4 rows. Each of those pixels is intended to readout a single SiPM signal. Figure 3.3 depicts the schematic block of the entire chip. The adopted architecture is a scalable solution that permits to increment the input throughput simply adding pixels on the column without changing the surrounding blocks. Moreover this matrix structure is implemented foreseeing to use the flip-chip bonding technique to connect the chip to the sensor, thus having a direct readout of the individual pixel by the corresponding front-end electronics that matches its size. However, since this is a first prototype, sensors are connected using a wire-bonding connection through the pads. In this way, the chip is more versatile and it can be employed with any SiPM regardless of the sensor geometry.

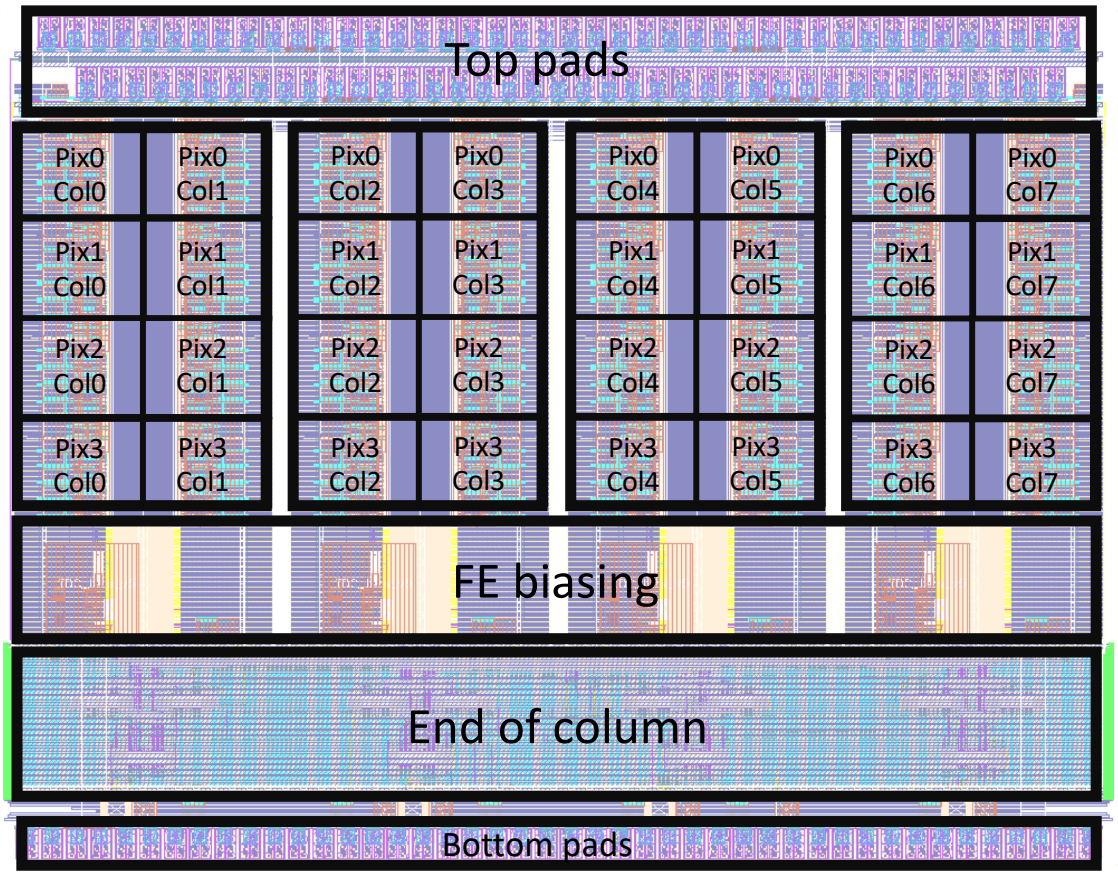


Figure 3.3: ALCOR full ASIC layout. It occupies a total area of $4.95 \times 3.78\ mm^2$.

Pixels on the same column are connected between them in a daisy chain network topology, where the address for each pixel is self assigned. The pixel address is defined by a two-bit zero register positioned above each column. *Pix 0* reads this register and assigns this value to its address, after which it increments it by one and transmits it to the next pixel. This operation executed for each pixel assigns easily all the addresses on the column. Most of the bias current and voltages needed for the analogue blocks are generated at the pixel level, but due to area limitation, some FE biases are defined in the bottom and transmitted in voltage mode along each column. The external Vref pad is used to provide the reference voltage from which the inner bias current and voltages are generated. The 32 pads placed in the top of the chip (Ispm) are used to connect sensors. Each of them provides the signal to a single pixel using M7/M6 metal connections. It is important to minimise the series resistance of these lines in order to avoid excessive noise contribution. In addition, four of the top pads (Debug) are used for debug purposes to readout FE and discriminator signals from *Pix0* in *Col0* and *Col7*. For test purposes it is possible to provide through the pad TP a test pulse to simulate an input signal and characterise each pixel control logic. The input and output pads are listed in the Table 3.1.

All the pixels communicate with the periphery of the chip, where the End-of-Column (EoC) acts as master and stores all the payloads that it receives from each column. Collected data are packed with Cyclic Redundancy Check (CRC) and 8*b*/10*b* encoding and transmitted serially to the outside world through 4 Low Voltage Differential Signaling (LVDS) drivers (q_0, q_1, q_2, q_3) placed at the bottom of the chip. The chip uses Serial Peripheral Interface (SPI) protocol (sclk, ss_n, sdi, sdo) to communicate with an external FPGA, the EoC is in charge to receive external configuration data and transmit it to each pixels.

Signal	Signal type	Description
sclk	Input	SPI clock
ext_clk	Input	System clock
ext_nres	Input	Reset, active low
ss_n	Input	SPI slave selector, active low
sdi	Input	SPI data IN
TP	Input	Test Pulse
Ispm_0 <3:0>	Input	SiPM input column 0
Ispm_1 <3:0>	Input	SiPM input column 1
Ispm_2 <3:0>	Input	SiPM input column 2
Ispm_3 <3:0>	Input	SiPM input column 3
Ispm_4 <3:0>	Input	SiPM input column 4
Ispm_5 <3:0>	Input	SiPM input column 5
Ispm_6 <3:0>	Input	SiPM input column 6
Ispm_7 <3:0>	Input	SiPM input column 7
sdo	Output	SPI data OUT
clk_out	Output	System clock
q_0	Output	LVDS col0, col1
q_1	Output	LVDS col2, col3
q_2	Output	LVDS col4, col5
q_3	Output	LVDS col6, col7
Vref	Input	Voltage reference
Debug<1:0>	Output	pix0-col0 FE debug
Debug<2:3>	Output	pix0-col7 FE debug

Table 3.1: Input and Output signal of Alcor chip.

3.3 Pixel Architecture

The pixel is designed as a single block and then replicated for the whole matrix. The layout of the pixel is shown in Fig. 3.4 and occupies an area of $500 \times 500\ \mu m^2$. The 2/3 of the total area is occupied by analogue circuits such as FE, discriminator and TDCs, while the remaining area is used for the digital circuits for pixel control logic and data transmission. In order to protect the analogue part from digital switching noise, every digital configuration signal is forwarded to analogue circuitry trough two cascaded inverters located in the analogue power domain. The input VFE is designed to operate with input capacitance up to 5 nF where the input charge goes in the range between 0.2 pC and 4 pC for a maximum rate of 5 MHz. The pixel that operates at the maximum system clock frequency of 320 MHz achieves a time resolution of 50 ps for total power consumption lower than 10 mW. In applications where the power budget is relevant, the clock frequency domain can be reduced to 40 MHz at the expense of a greater time binning.

The electrical signal from the SiPM is conditioned by a RGC circuit that makes the input signal suitable for the dual-gain programmable pre-amplifier. While, two leading edge discriminators with configurable threshold generate the trigger CMOS signals that are fed to the pixel digital control block. The use of two branches with different amplifiers allows to exploit several degrees of freedom of the measurement. For instance, the branch called 'high' can be used for time measurement with a very low threshold voltage, which is also sensitive to noise; while on the branch called 'low' it is possible to apply a validation of the event, thus applying a higher threshold voltage and therefore be free from noisy signals. Moreover, due to the long tail of the pulse event generated by SiPM sensor, when the Pixel operates in ToT mode, the double branch allows to have one threshold very low in order to perform a precise time measurement, while the second threshold can be set higher in order to cut the long tail and obtain a measurement with low jitter. The Figure 3.5 shows the schematic block of the FE, where the signal *S0* is used to select the polarity of the signal, *VFE positive* blue branch and *VFE positive* red branch. The Gain1 and Gain2 signals define the gain amplification of output stages according to Table 3.2 where $LSB = 2\ mV$. The configuration of those signals is defined in Section 3.3.1.

The threshold V_{th1} and V_{th2} can be externally programmed per pixel. The nominal

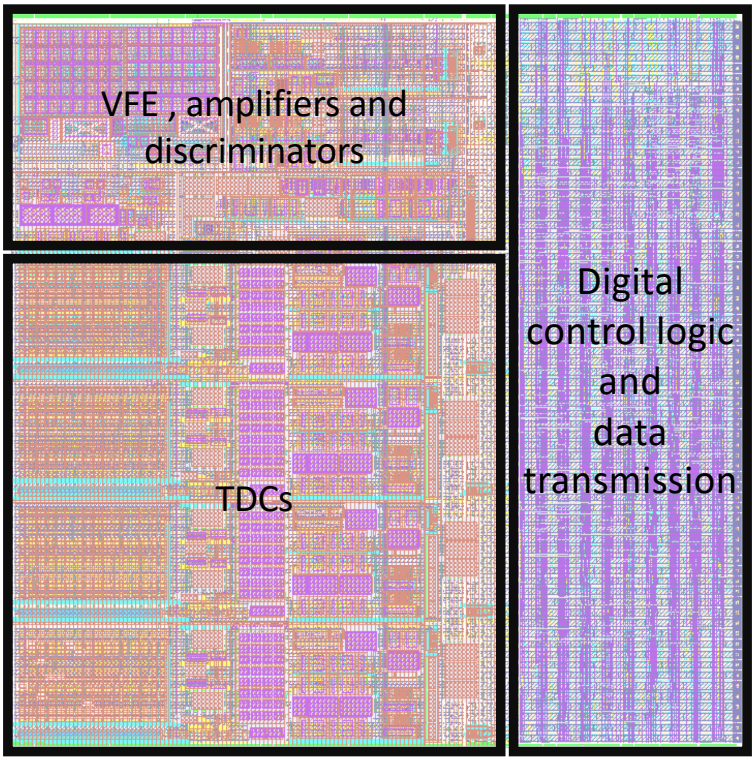


Figure 3.4: Pixel layout where the area of each block is defined. The total pixel area occupies $500 \times 500 \mu m^2$.

value of these voltages can be set from a minimum of 550 mV up to a maximum of 878 mV with a minimum step of 0.80 mV and a maximum step of 2 mV.

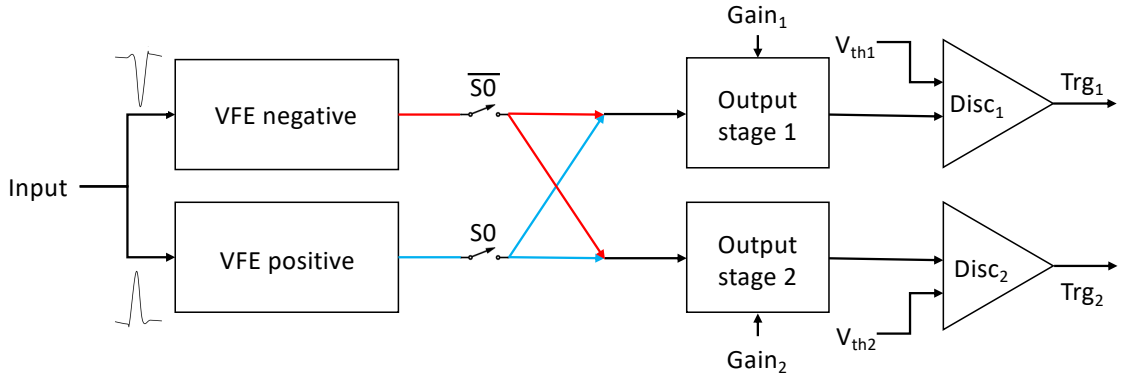


Figure 3.5: Front-End schematic block. The FE embeds input signal VFE with programmable polarity, two programmable amplifiers and two programmable discriminators.

$Gain_n$<1>	$Gain_n$ <0>	gain amplifier
0	0	$10 \cdot LSB$
0	1	$7 \cdot LSB$
1	0	$4 \cdot LSB$
1	1	$1 \cdot LSB$

Table 3.2: Describes how amplifier's gain changes according to $Gain_1$ and $Gain_2$ value.

The remaining blocks of the Pixel architecture are used to generate the timestamp. The block diagram of this digital logic is depicted in Figure 3.6.

The coarse timestamp is derived from a 15-bit binary counter on-pixel and it is saved at the rising/falling edge of the Trg_1/Trg_2 signals, according to the pixel operation mode. This counter at the maximum clock frequency generates a time window of 104857.6 *ns*, while the time window is 819200 *ns* if the minimum clock period is set.

The fine timestamp information is generated using a low-power TDC, based on analogue interpolation. The area available in the pixel allows to implement four TDCs, in this way the system control logic is able to achieve a 5 MHz trigger input rate in a single timestamping mode. The *TDC crtl* is in charge to enable the TDC according to pixel configuration. ALCOR is designed to be also configured in Time-over-Threshold (ToT) mode, used to compute energy measurement in case of single event or in Slew Rate (SR) mode to calculate the slew rate time of the analogue input signal. The event payload generated from each Pixel in the *Data control unit* contains timestamp and position information of the event detected. Each pixel also manages the data that it receives from the up pixel or configuration signal from the bottom pixel. The address is self-assigned using pixel address received from the above node. The *Pixel configuration unit* communicates with the EoC and it processes the configuration signal and sets the pixel accordingly.

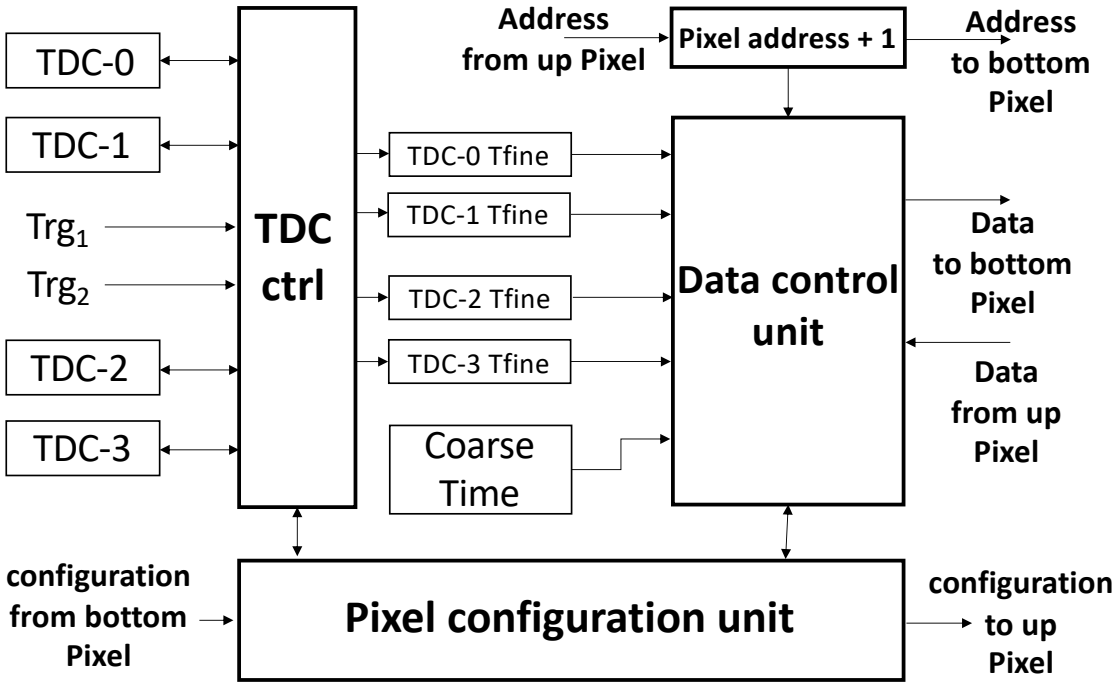


Figure 3.6: Pixel schematic block diagram. The Trg_1 and Trg_2 are the trigger signal generated from the FE. Each pixel contains the digital control logic, data ADC formatting, four low-power TDCs, fine and coarse counters.

3.3.1 Pixel configuration

The configuration phase is executed through an FPGA that is connected to SPI interface of ALCOR chip. Each pixel can be configured independently using the address shown in the schematic block diagram in Figure 3.3. The configuration state for discriminators' threshold voltage, amplifiers bias, TDC settings and pixel operation mode are generated at pixel level and stored respectively into four Pixel Configuration Register (PCR) of 16-bit each, placed in the *Pixel configuration control* block. Together with the pixel address of 3-bit is included the PCR address of 2-bit length. The PCR registers are defined as:

- **PCR0** defines the coarse value for TDC's fast current for each TDC. This register stores the digital value that will be converted through DAC in voltage.
- **PCR1** defines the fine value for TDC's fast current for each TDC. This register stores the digital value that will be converted through DAC in voltage.

- **PCR2** defines the threshold V_{th1} and V_{th2} voltages of discriminator according to the equation:

$$V_{th} = V_{offeset} + LEDAC \cdot LSB \tag{3.1}$$

  Where the offset is defined by the LEDACVth register, LEDAC is the value of LE1DAC/LE2DAC register and LSB is defined by the LEDACrange as reported in Table A.5.

- **PCR3** defines the pixel operation mode (OpMode), the gain (Gain1, Gain2) and offset (Offset1, Offset2) of amplifiers and input polarity (Polarity).

An example of the pixel configuration phase is depicted in Figure 3.7. The *PCRaddress* signal received from the EoC contains the pixel address (index <4:2>) and the PCR register address (<index 1:0>) to be configured. In the example, the EoC sends a configuration signal to Pixel-1 and is configuring the PCR3. The *PCRwrite* signal is transmitted from EoC and is used to notify the pixels to read the *PCRdata*. Changing the PCR address value embedded in *PCRaddress* it is possible to configure also PCR0/PCR1/PCR2.

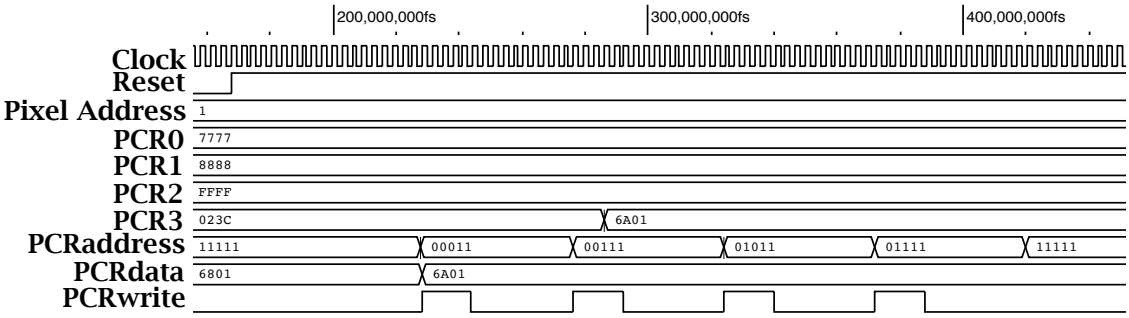


Figure 3.7: Pixel configuration simulation. This time diagram reports the configuration of the PCR3 register of Pixel1. Each configuration is target with the PCRaddress, which contains the Pixel address and PCR address and the PCR data.

Global analogue bias settings are configured in the Bias Configuration Register (BCR) placed in the EoC and then they are generated in the *Fe biasing* block and distributed in voltage mode to each column. The BCR is a combination of two registers that defines the bias setting of two columns:

- **BCR_0** defines bias for the TDC comparator (iblatchDAC), TDC (iTDC) and the test-pulse circuit.

- **BCR_1** defines FE discriminators bias (ib_sF, ib_3, ib_2), FE polarity (S0),

The configuration packet format of PCR and BCR registers are reported in the Appendix A.1.

3.3.2 Pixel operation mode

The pixel operation mode defines the timestamp generation according to the discriminator signal. There are five possible settings:

- **OFF**: The pixel is turned OFF, it stops generating data while keeping data transmission between pixel active. This operation reduces the power consumption of the digital blocks. Besides this, different OFF modes disable or enable the FE.
- **Leading Edge Trigger (LET)**: This operation mode generates a time-tag on the rising edge of the trigger, thereby the chip provides the time-of-arrival information for each event. In this context, we call “”trigger“” the digital pulse provided by the discriminator following the front-end amplifier when a signal above threshold is detected. In this case TDCs are enabled in a round robin fashion when a new trigger occurs. In case all TDCs are in a busy state, the coming events are counted as lost.
- **Time-over-Threshold (ToT)**: This operation mode generates a time-tag on the rising edge of the trigger and a time-tag on the falling edge of the trigger. The difference of the two time-tags gives the time over threshold. In case of a single photon, off-line analysis allows to retrieve charge measurement of SiPM signal. TDCs are set to work coupled, TDC-0/TDC-1 and TDC-2/TDC-3, in this way off-chip computation can easily recover TDC data belonging to the same event.
- **Time-over-Threshold (ToT)$_2$**: This operation mode is equal to ToT mode, unless it manages two triggers. The pixel generates a time-tag on the rising edge of the first trigger and a time-tag on the falling edge of the second trigger, thereby allowing for a ToT measurement using triggers generated from amplifiers with different gain settings. In case of long SiPM signal, this operation mode allows to optimise the accuracy of the charge measurement reducing the jitter on the tail.

- **Slew Rate (SR)**: This operation mode generates a time-tag on the rising edge of the first trigger and a time-tag on the rising edge of the second trigger. TDCs work coupled, TDC-0/TDC-1 and TDC-2/TDC-3. The difference of time-tags measures the slew rate of input signal. This is suitable to test the front-end and tune the parameters of amplifiers and discriminators. Moreover, this operation mode can be used to reject the dark count using the first trigger as a timestamp and the second trigger as event validation.

The timing diagram in Fig. 3.8 illustrates the behaviour of the trigger signals Trg_1/Trg_2 and TDC indexing for each one of the operation modes mentioned above. When the TDCs work is coupled, they are considered a single computational unit.

The *TDC ctrl* is designed using four different Finite-State Machine (FSM) which are selected depending on the operation mode.

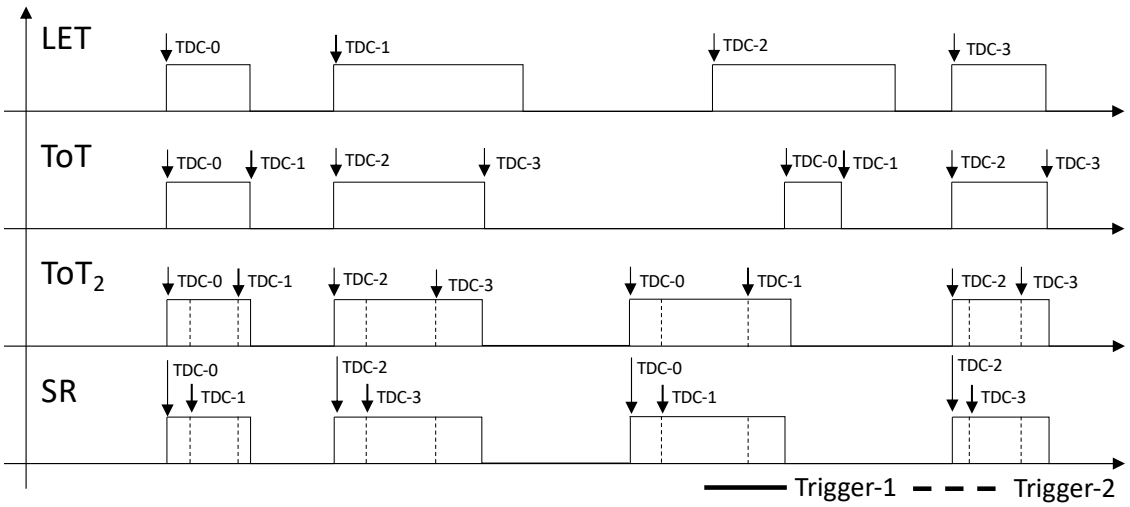


Figure 3.8: The TDCs are enabled accordingly to the operation mode. The LET and ToT modes use only the Trg_1, while the ToT_2 and SR modes use both Trg_1 and Trg_2 triggers.

The input signal of the pixel is the SiPM sensor output. However, ALCOR includes a test mode where an external TP is provided to characterise and configure each pixel properly. This signal can be forwarded to the pixel control logic or to the analogue FE. The bits in position <12:9> of PCR3 are used to define the operation mode and to select the input. Configuration values are listed in Table 3.3. The pixel power-on state is LET mode, which is a safe-mode that allows to initialise the chip without incurring errors.

When the Pixel operates in ”OpMode_TP_TDC” operation mode, the TP signal is sent directly to the *TDC ctrl* of the pixel as a trigger signal, this allows to test the functionality of TDCs and digital logic. While in ”OpMode_TP_FE” mode the TP is forwarded to the FE where a circuit simulates a SiPM signal to test the amplifiers and the discriminators. The test mode is suitable to characterise and configure each pixel properly.

PCR3 <12:9>	Operation mode	Description
0000	OFF	Control logic OFF, FE disabled
0001	LET	Sensor signal to Front-end
0010	LET_TP_TDC	Test Pulse to control logic
0011	LET_TP_FE	Test Pulse to Front-end
0100	ToT	Sensor signal to Front-end
0101	ToT_TP_TDC	Test Pulse to control logic
0110	ToT_TP_FE	Test Pulse to Front-end
0111	OFF	Control logic OFF, FE enabled
1000	OFF	Control logic OFF, FE enabled
1001	ToT_2	Sensor signal to Front-end
1010	ToT_2_TP_TDC	Test Pulse to control logic
1011	ToT_2_TD_FE	Test Pulse to Front-end
1100	SR	Sensor signal to Front-end
1101	SR_TP_TDC	Test Pulse to control logic
1110	SR_TP_FE	Test Pulse to Front-end
1111	OFF	Control logic OFF, FE disabled

Table 3.3: The bit in position 12 to 9 of PCR3 are used to define the operation mode of the single Pixel.

3.4 TDC behaviour

The Time to Digital Converter (TDC) is a circuit commonly used to perform a digital representation of the time. This circuit allows to obtain a *ps* time resolution employing a low power analogue interpolation. Figure3.9 depicts a simplified model of the TDC circuit implemented in ALCOR. In the idle state, SW_{fast} and SW_{slow} switches are closed while $\overline{SW_{fast}}$ and $\overline{SW_{slow}}$ switches are open. In this mode, the current in both branches flows to the ground. When a trigger signal occurs, $\overline{SW_{fast}}$ is closed and SW_{fast} is opened, for as long as it is the time interval to be measured. In that frame the C_{fast} capacitor is charged with the I_{fast} current and a *fast ramp* is generated linearly where the amplitude

is proportional to the time to be converted:

$$V_{fast} = \frac{I_{fast}}{C_{fast}} \Delta T \tag{3.2}$$

The conversion starts when $\overline{SW\_slow}$ is closed and *SW_slow* is opened. The capacitor C_{slow} is linearly charged with the I_{slow} current and the curve is label as *slow ramp*. A counter measure the clock period that the *slow ramp* takes to reach the same voltage amplitude of the *fast ramp* and this is the fine time measurement:

$$T_{fine} = \frac{C_{slow}}{I_{slow}} V_{slow} \tag{3.3}$$

The Interpolation Factor (IF) defines the time binning that a TDC may achieve. This can be easily calculates as:

$$IF = \frac{T_{fine}}{\Delta T} = \frac{C_{slow}}{I_{slow}} V_{slow} \frac{I_{fast}}{C_{fast} V_{fast}} \tag{3.4}$$

Considering that the voltage amplitude is the same and capacitors are equal, it can be easily deduced that IF depends only on the current ratio. So, depending on the clock period, the time binning is defined as:

$$TDC_{time\_binning} = \frac{CLK_{period}}{IF} \tag{3.5}$$

When the *slow ramp* reaches the same voltage amplitude of the *fast ramp*, comparator's output changes from logic-0 to a square signal with the same frequency of the system clock in order to provide a synchronised signal to the logic system. This signal determines the end of the conversion and closes the *reset* switch. All the capacitors are discharged and prepare the whole system for a new conversion.

The fast current and slow current are defined by the configuration register PCR0 and PCR1, as discussed in Section 3.3.1. The fast current follow the equation:

$$I_{fast} = ((2 \cdot 59) + cDAC\_TDC) \times LSB \tag{3.6}$$

Where the *cDAC_TDC* is the voltage value defined in the PCR0 register and the LSB

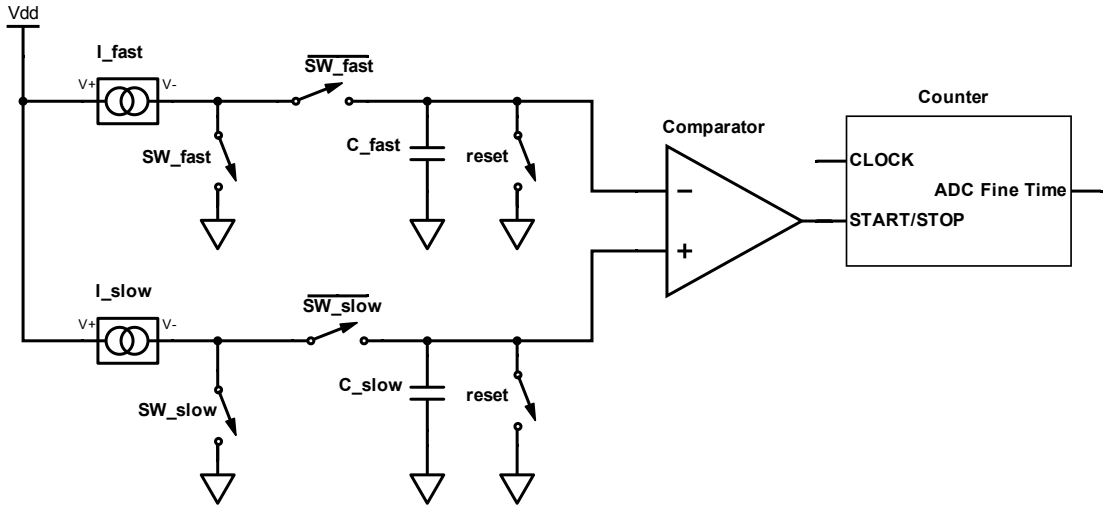


Figure 3.9: TDC schematic circuit.

value is defined by the *iTDC* current in the BCR register. The slow current depends on the *cfg_I_ratio* configuration signal and LSB value:

$$I_{slow} = \begin{cases} LSB \cdot 1 & Iratio =' 1' \\ LSB \cdot 2 & Iratio =' 0' \end{cases} \tag{3.7}$$

The Figure 3.10 depicts simulation results of TDC circuit combined with the *TDC control* logic. Here, capacitors are set equal to 480 fF, and LSB = 210 nA. Therefore, the I_{fast} current is set equal to 27 μA and I_{slow} equal to 420 nA. This configuration defines a current ration of 64 achieving thus 50 ps of time binning at 320 MHz. In particular application, that needs a better fine measurement, the I_{slow} current can be halved to 210 nA, obtaining an IF of 128 that generates a time binning of 25 ps.

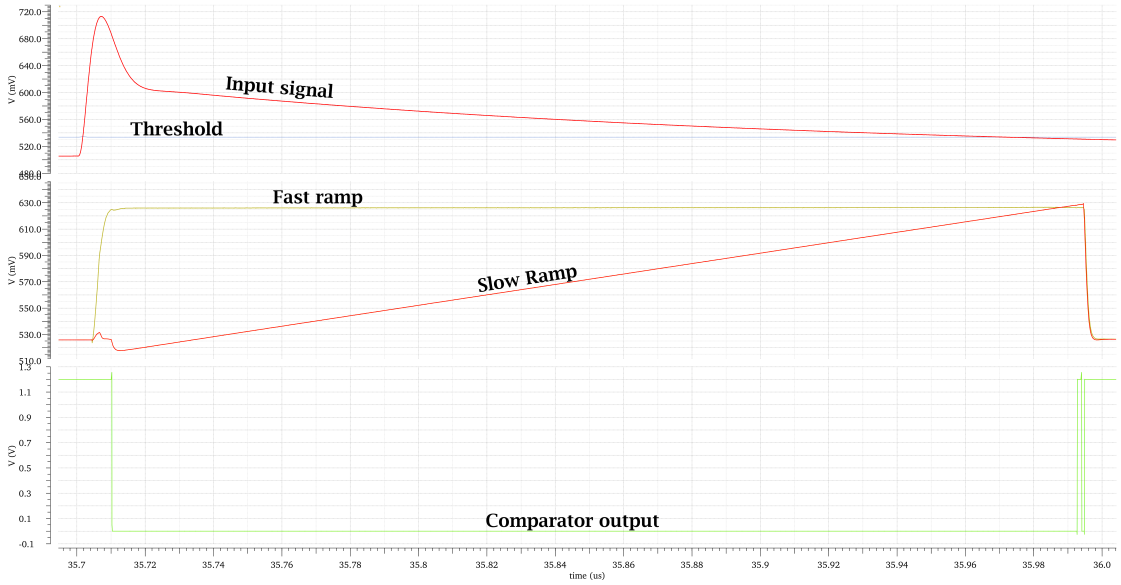


Figure 3.10: TDC simulation.

3.4.1 TDC operation range

In ALCOR chip, the fine time interval of interest is calculated in the clock period, and it goes from the trigger arrival time to the first clock rising edge. However, fine time measurement very close to the clock edge is difficult to be performed and may not be so accurate. Therefore, if the trigger occurs immediately before the clock's trailing edge, the fine measurement is performed till the first clock rising edge (Fig. 3.11). Otherwise, in case the trigger occurs immediately after the trailing edge of the clock, the fine time lasts till the second clock rising edge (Figure 3.12). This extra time measurement of a clock period will be then removed from the off-chip timestamp calculation, as discussed in Section 3.5. The time interval $[T_1 - T_0]$ can therefore assume a value in the range of $\frac{1}{2}$ clock period and $1\frac{1}{2}$ clock period.

TDCs are simulated providing 350 TPs have been provided as trigger, with a phase shift of 15 *ps* from one input to the other. This input stimulation generates all possible $Time_{fine}$ scanning completely the clock period. Simulation results, reported in Figure 3.13, show the linearity of the TDC behaviour, without loosing ADC counts. The minimum T_{fine} should be equal to the time binning, but the curve denotes a systematic

error that introduces an offset to all counts. Most probably this is due to the propagation delay of the signal transmission between the control logic and the analogue TDC. The minimum and the maximum counts are the boundaries that indicate the fine time interval of interest. Subtracting these two values, the result is equal to the IF of 128 (Equation 3.8). To represent the ADC value, a register of 8-bit is more than enough. Although, as the simulation introduced an offset, real behaviour at cryogenic temperature could increase this systematic error. So, to prevent this case, one more bit can be added through a *cfg_safety_bit* signal that increases the fine counter register to 9-bit. The Table 3.4 defines briefly the fine counter register length depending on the configuration signals defined by the End of Column Configuration Register (ECCR) (see Appendix A.1). These configuration signals are common to all the columns.

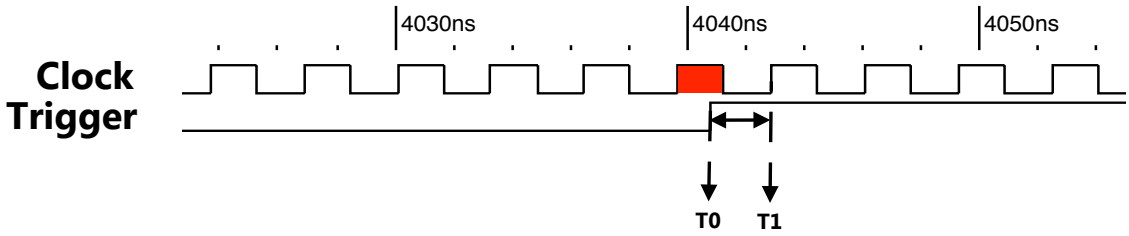


Figure 3.11: In case the trigger occurs in the red area of clock period, immediately before the trailing edge, the fine measurement is measured from the trigger arrival time till the first clock rising edge.

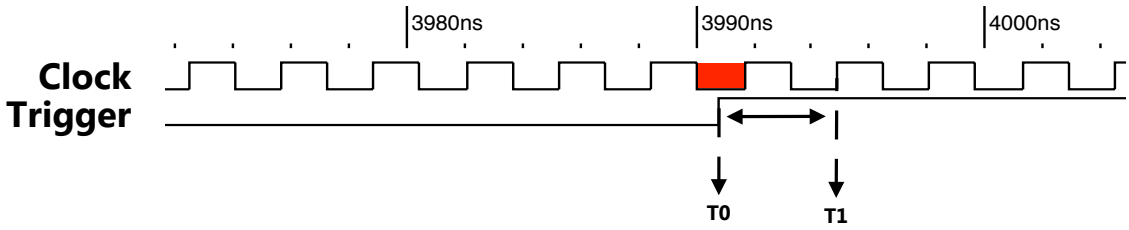


Figure 3.12: In case the trigger occurs in the red area of clock period, immediately after the trailing edge, the fine measurement is measured from the trigger arrival time till the second clock rising edge.

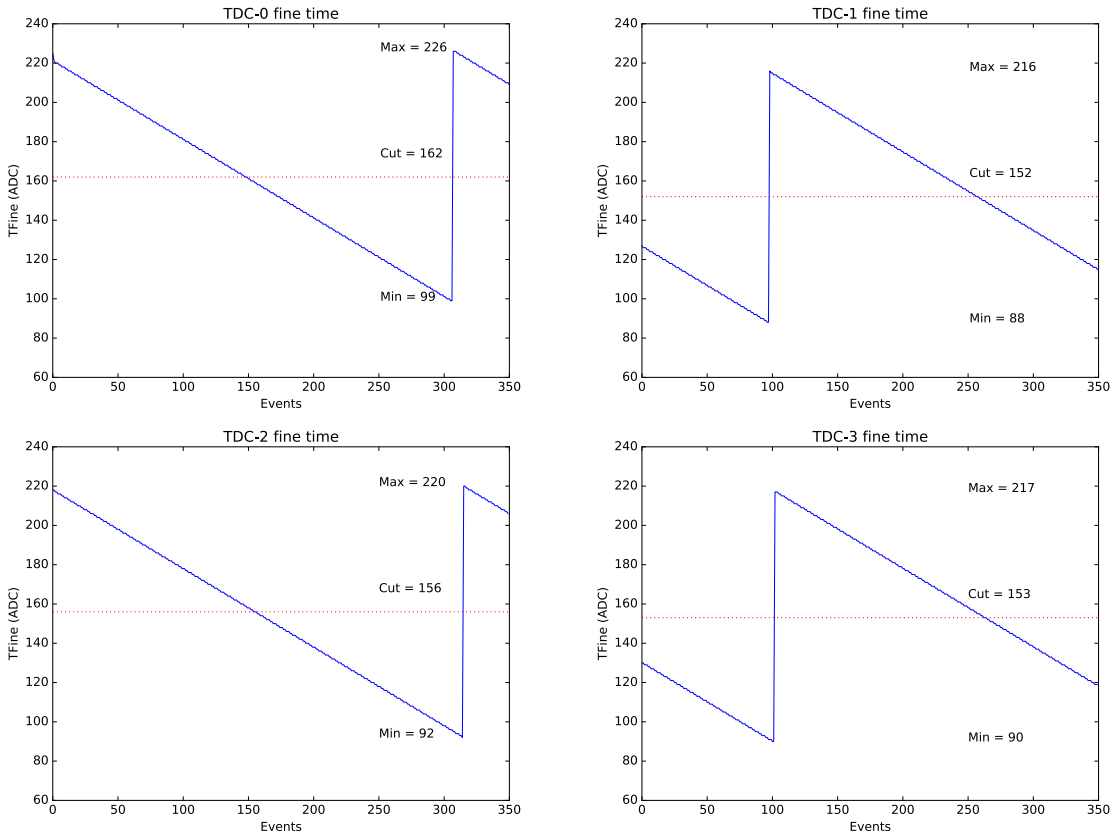


Figure 3.13: Simulation of a TDC with 128 ratio counter.

$$I.F. = TFine_{max} - TFine_{min} \tag{3.8}$$

		cfg_I_ratio	
		0	1
cfg_Safety_bit	0	7-bit	8-bit
	1	8-bit	9-bit

Table 3.4: The Fine counter register bit length, changes according to cgf_I_ratio and cfg_Safety_bit.

The results showed in graphs will be used to calibrate the TDCs. In particular, the *cut* line defines the threshold where the $Time_{fine}$ counts above this value have measured the time of a trigger that occurred after the clock's trailing edge. The extra counts of 1 clock period will be removed to all these values.

3.4.2 Simulation

TDCs and pixel logic have been simulated using mixed-signal tools that combine the analogue circuits and the digital control logic. These simulations are useful to test the time accuracy obtained with the data payloads. As a first simulation, the pixel has been set in LET_TP_TDC mode, providing a train of TP with a time delay of 15 *ps* from one signal to the other. The TDCs are set with a current ratio of 64. The generated payloads are read and saved in an external file. All the simulations are performed with a system clock frequency of 320 MHz. Then data are processed using a Python script reported in Appendix A.3.1. Figure 3.14 reports histograms of time difference between the timestamp generated by pixel and the arrival time retrieved in a simulation, with a binning of 50 *ps*.

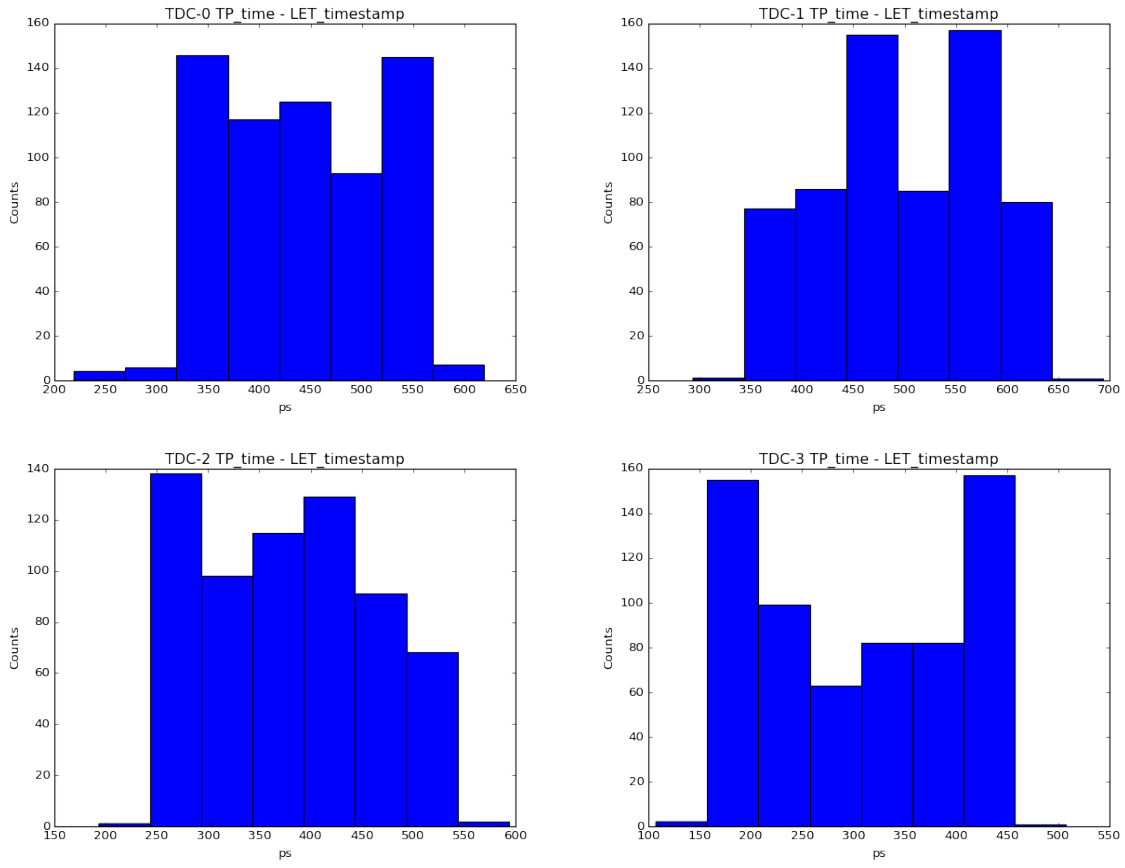


Figure 3.14: Arrival time of an event expressed as time difference between pixel timestamp and simulation timestamp.

The behaviour of each TDC is very similar, there is a systematic error that shifts the histogram of $\sim$ 200 *ps*. This is mostly due to signal propagation delay between digital control and TDC. While the spread of $\sim$ 400 *ps* is a consequence of a not linearity of *fast ramp* and *slow ramp* of TDCs' capacitors for every measure.

With the same set of TP input, the pixel has been also tested in ToT_TP_TDC mode. Time measurement results are depicted in the histogram of Figure 3.15. The graph on the left reports ToT measured with TDC0 and TDC1, while the graph on the right reports ToT measured with TDC2 and TDC3. The TP provided to the pixel lasts of 95 *ns* it is well measured by the TDC, only $\sim$ 2.70% of events have a mismatch of one clock period. This is principally due to events that are very close to $Counter_{cut}$ threshold, and therefore they cannot be easily discriminated. In the Appendix A.3.2 there is the Python script used to generate the ToT measurement. The same script can also be used to calculate SR time.

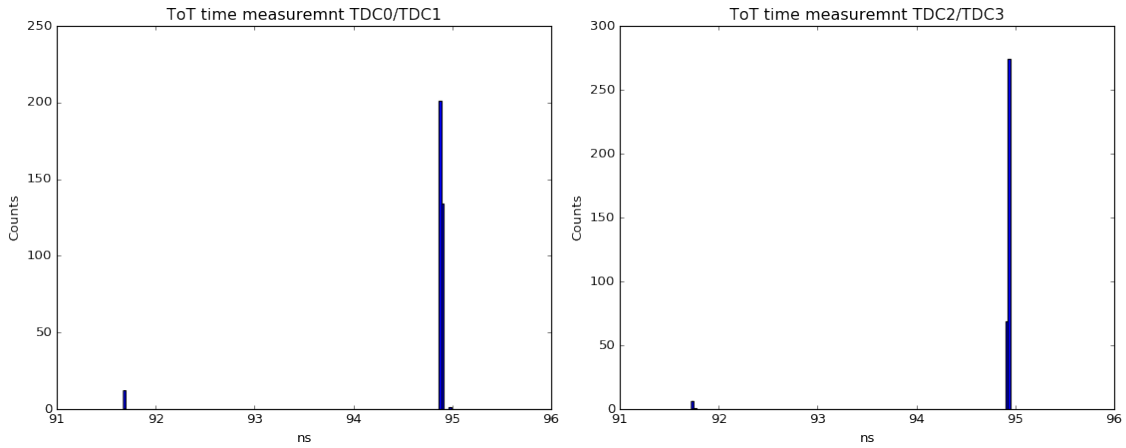


Figure 3.15: Time-over-Threshold simulation performed with a train of TP signal, with a time delay of 15 *ps* between one signal to the other.

3.5 Data payloads format

Alcor is designed to generate a 32-bit data payload at every event brought out by SiPM sensor. The pixel generates a data containing the position tag in terms of *Column ID* and *Pixel ID*, the *TDC ID* of four TDCs that performed the fine time measurement and the time stamp expressed as *Coarse counter* and *Fine counter*. Since every pixel reads only one sensor, the position tag also identifies the SiPM from which the event

has been detected. The ID of the TDC (2-bit) used for the fine-time generation identifies rinsing/falling edge of trigger when the pixel operates in TOT/TOT_2, or Trg_1/Trg_2 when in SR mode as shown in Figure 3.8. Whenever all four TDCs are in a busy state, new triggers will be discarded, the number of the lost events are counted in a dedicated register on-pixel. The Data Control block handles the payload generation and storage, as well as the data pixel-to-pixel data transmission to the EoC. Generated data words are first stored in a register, one for each TDC, and then they are queued in a FIFO register (depth=4). In case of FIFO saturation, lost payloads are counted in a second lost-event register on-pixel. All informations are wrapped in the Status word, which is generated only on request from EoC and it is done to all pixels at the same time. This payload contains also a Single Event Upset (SEU) counter that says how many errors have been produced by the radiation effect. The data formatting of the two payloads are showed in Figure 3.16.

Event word

Column ID	Channel ID	TDC ID	Coarse counter	Fine counter
3 bits	3 bits	2 bits	15 bits	9 bits

32 0

Status word

Column ID	Pixel ID	Lost event counter	Lost e.w. counter TDC1	Lost e.w. counter TDC2	Lost e.w. counter TDC3	Lost e.w. counter TDC4	SEU counter
3 bits	3 bits	6 bits	4 bits	4 bits	4 bits	4 bits	4 bits

32 0

Figure 3.16: Event-word and status-word payloads.

The arrival time wrapped in the payload refers to a time window of 2^{15} clock period length. Therefore, EoC during the data transmission to the outside world includes also a time window counter that gives a relative time value. The arrival time of the event in a certain time window can be calculated following Equation 3.9, where the coarse counter is multiplied by the clock period and then it is subtracted with the $Time_{fine}$ obtained in the Equation 3.10. This value is calculated considering the $TDC_{time\_binning}$ that can be 25 *ps* or 50 *ps* depending on TDC current ratio settings. As explained in Section 3.4, in order to remove counts greater than one clock period, the $Counter_{cut}$ must be subtracted

from the TDC fine counts.

$$Time = Counter_{coarse} \cdot CLK_{period} - Time_{fine} \tag{3.9}$$

$$Time_{fine} = \begin{cases} Counter_{fine} \cdot TDC_{time\_binning} \; ; \quad Counter_{fine} < Counter_{cut} \\ (Counter_{fine} - Counter_{cut}) \cdot TDC_{time\_binning} \; ; \quad Counter_{fine} \geq Counter_{cut} \end{cases} \tag{3.10}$$

3.5.1 Special payloads

The pixels's control logic includes some watchdog timers that perform a checking on the trigger input duration and on the TDC conversion time. When the pixel operates in ToT/ToT$_2$ mode, it may happen that the trigger input signal remains stuck at $'1'$ and it can be caused by the FE, discriminator or by the SiPM sensor. In this case the logic waits an amount of time equal to 2^{15} clock periods, after that a payload with *Fine counter* fixed to $0x000$ and *Coarse counter* of the rising edge trigger is generated, as showed in Figure 3.17. In SR mode, in order to compute the slew rate measurement, there must ensure the presence of both triggers, Trg$_1$ and Trg$_2$. In the case only the first signal arrives, the control logic waits for the second signal till the trailing edge of the first trigger. After this amount of time, the payload that has been generated of the first point is discarded.

Column ID	Pixel ID	TDC ID	Coarse counter	Fine counter
---	---	--	c.c. of the rising edge	000000000

Figure 3.17: When a pixel operates in ToT/ToT$_2$ mode, Control logic waits the trailing edge of the trigger for 2^{15} clock periods from the rising edge of the trigger. If the timers reaches the maximum value this payload is generated off-pixel to notify the problem.

Another important check is executed on the duration of the TDC conversion. When the *Fine counter* register reaches its maximum value of $0x1FF$, it means that the TDC's comparator did not stop the counter. This error may happen if the slow ramp is not properly settled in such a way as to reach the fast ramp within the maximum counts. This can be solved by tuning the slow ramp current using PCR0/PCR1 registers. To

notify this kind of problem, the logic waits for the full-scale of the fine time counter, that can depend on the configuration settings showed in Table 3.4. At the end of this time, the special payload showed in Figure 3.18 is generated, where *Fine counter* is filled with ones. This control is done independently of the specific operation mode.

Column ID	Pixel ID	TDC ID	Coarse counter	Fine counter
---	---	--	----------	111111111

Figure 3.18: Event-word generated when the f.c. reaches its maximum value and TDC doesn't give a stop conversion signal. The f.c. stores a value that cannot be obtained from a time conversion.

3.6 Data transmission

The data transmission of the payloads is managed by the *data control* of the pixel that is in charge of wrapping the data and communicating with the EoC. Pixels on the same column are connected in a daisy chain network, and the generated data is transmitted downwards pixel by pixel until they reach EoC. Due to the physical distance between EoC and pixels, signals transmitted from the periphery of the chip may not be in phase with the pixel's clock. Therefore, synchronisation circuits have been included in each pixel to synchronise handshake signals. This circuit has been included in the Test Chip (TC) and is shown and discussed in the Chapter 4.2.2. Payload that a pixel generates can be data type or status type. The first one is transmitted by request from the pixel, while the second one is only on request from the EoC.

3.6.1 Data payload

Data payloads ready to be sent off are first stored into a FIFO of 4 position depth, then a request is made from the pixel to EoC. In order to avoid starvation from other pixel, just one payload per pixel is transmitted for each request. The timing diagram of the control signals and the data of a pixel is shown in Fig. 3.19-a. The custom protocol applied for the data transmission starts with a *"write request"*, this signal is generated from each pixel whenever there is data ready to be transmitted. The EoC to suspend any

further write requests responds with a *"freeze"* signal that it is propagated through all the pixel columns. From this time on, the periphery is ready to receive data and informs all pixels that have made the write request with the *"write enable from EoC"* signal. This signal is sent through the pixel column and enables the data transmission to all pixels ready to send data. The write token signal, referred to as *"Pixel write enable"* in the time diagram, is asserted by the pixel entitled to write the data bus and propagate to the bottom pixels. The pixel with a higher address starts the data transmission. Payloads are sent in parallel at the same time, and the transmission lasts for 6 clock cycles in order to ensure EoC the correct sampling and avoid bits transition. When a pixel is not transferring its own data, it simply forwards data coming from the upper pixel as shown in the time diagram. To avoid overlapping of data, the EoC needs at least 3 clock cycles between two data transmissions. In an idle state, output signals are all set to one.

An example of data transmission is reported in Figure 3.19-b. This is a simulation of a single column where all pixels are sending data to EoC. Starting from *Pixel 3* the communication ends with *Pixel 0*. This time diagram shows how data are transmitted from one pixel to the other, and in cases where the pixel is physically far from the periphery, the signal delay propagation is more evident.

3.6.2 Status payload

The status payload is generated only on request by EoC, whenever there is a need to control the condition of the pixel in terms of event loss, data payload loss and SEU events detected. The status request involves all pixels on the column, therefore all this phase lasts for 33 clock cycles. Figure 3.19-c depicts the time diagram of status transmission, starting from the *Status request* made by the periphery, follows a *Freeze* signal long 2 clock cycles that suspends any request from pixels. From this time on, each pixel communicates its own status payload. The write permission is managed by the token *Pixel write enable*. The pixel with a higher address has the priority to transmit data. The status transmission lasts for 6 clock cycles, and from one payload to the other there are 3 clock cycles of idle data. Analysing the data on the time diagram, the *Pixel 3* has generated *"0D00000"*, which means that the pixel lost 16 events during all the simulation. When the pixel concludes the status transmission, all the registers are reset to zeros.

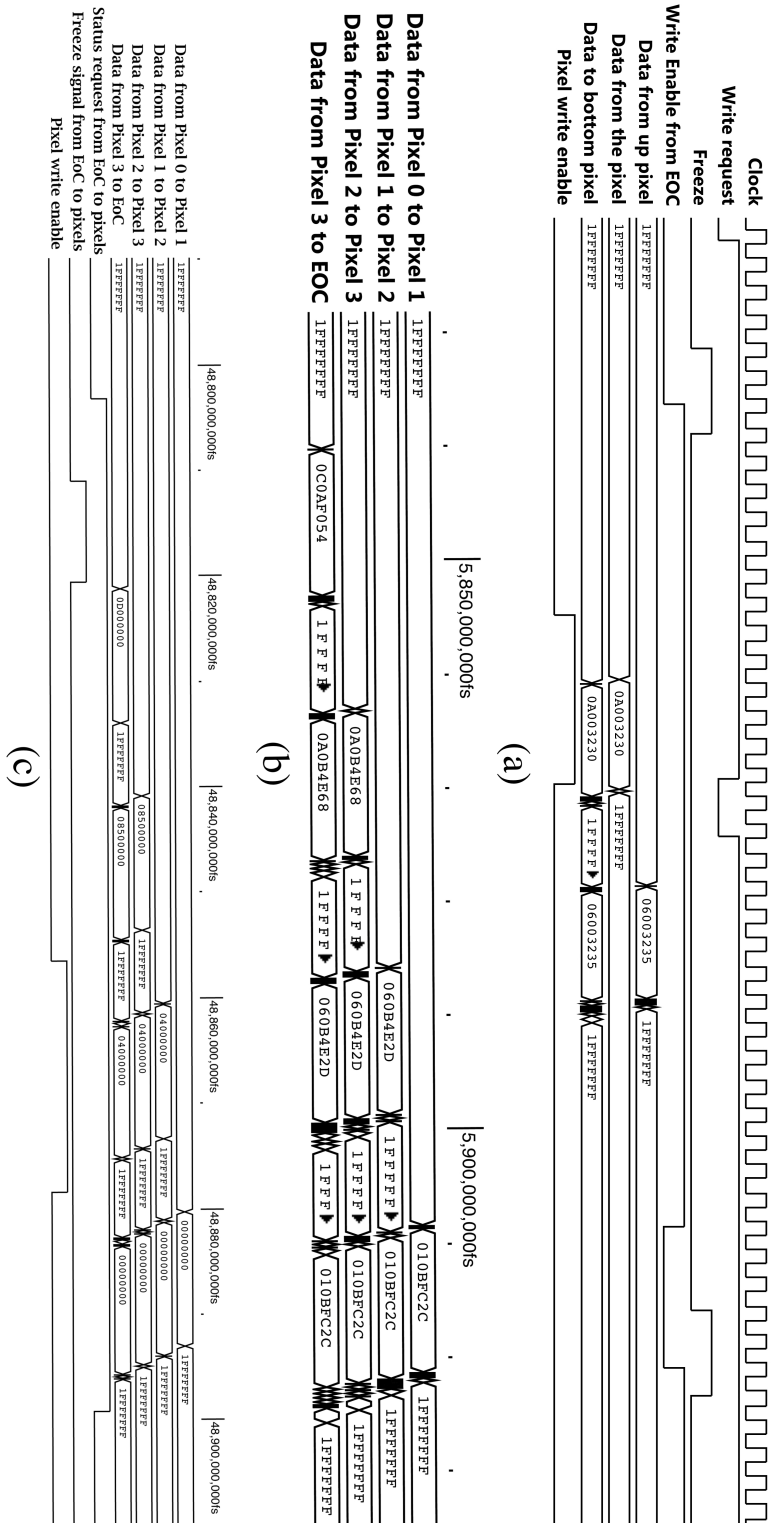


Figure 3.19: Timing diagram of: (a) data transmission protocol between pixel and EoC, (b) data transmission between pixels, (c) status data request and transmission between pixel and EoC.

3.7 End of Column

The End-of-Column (EoC) is an interface block placed in the periphery of the chip that communicates with the external world on the one end and the pixels on the other. The routing of all the signals between the End of Column logic and the pixel matrix has been done buffering every connection from pixel to pixel in order to avoid the use of very long nets requiring strong and large drivers. Furthermore, adopting this routing scheme, one can easily manage the signals skew and delay propagations by the use of automatic place and route tools.

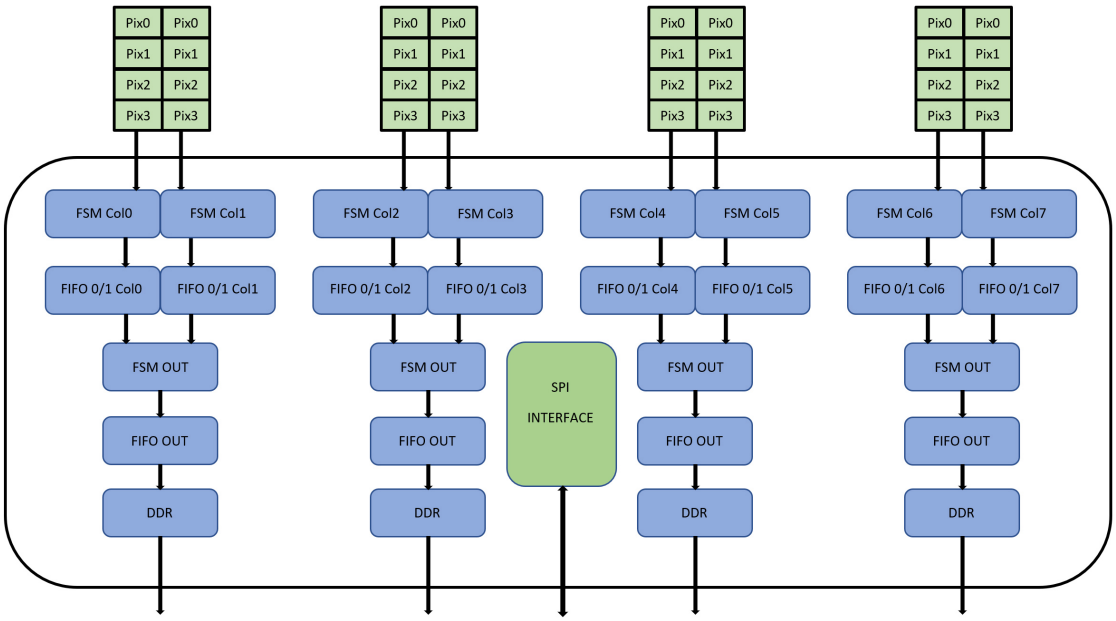


Figure 3.20: Schematic diagram of EoC data storage and transmission.

A dedicated FSM for each column performs the scan of the column in order to read only pixels which have valid stored data. To do this, a handshake logic has been implemented between pixels and End of Column controller (see Section 3.6). Thanks to this mechanism, only pixels having stored data take the ownership of the bus, optimizing the readout time, and only one payload per pixel can be extracted within each readout cycle, in order to prevent buffers overflow in other pixels. During the readout cycle, other incoming data can be processed and stored in order to be extracted in the following readout cycle. The whole readout system is very efficient in terms of data loss, but the time order of the events can't be preserved because it strongly depends on their

timing and position distribution. In addition, the number of internal buffers and the readout scheme increase the probability of having unsorted data.

In order to avoid ambiguities in the time reconstruction, it is necessary to regroup data frame inside the correct turn of the coarse counter. To do this, the End of Column hosts a local copy of the coarse counter. The value of MSB is used to tag events of type 0 and events of type 1 (depending of the MSB bit) in two different FIFOs. Another FSM then performs the data merging reading FIFOs 0 and 1 for two columns, in order to write the output FIFO with encapsulated double column data with headers status words and trailers every coarse counter cycle.

3.7.1 SPI interface

The communication between the ASIC and the FPGA is provided by a Serial Peripheral Interface (SPI) where the ASIC is slave.

According to SPI protocol, it uses a *SCLK* port to provide the serial clock, the *SDI* and *SDO* ports for the serial data IN/OUT and the *SS_n* for the slave select (active low).

The SPI port makes use of LVDS signals and since there is a direct connection between Application specific integrated circuit (ASIC) and FPGA, there is no need to implement a three-state *SDO*, therefore this port is held low when inactive. SPI serial clock frequency can be set up to 20 MHz, which corresponds to the system clock frequency divided by 16 (clock period 50 ns). The Clock Polarity (CPO) and Clock Phase (CPHA) have been set to 0 and 1 respectively and Figure **??** shows the resulting timing diagram, with the most significant bit transmitted first.

The SPI word, shown in Figure 3.22, is composed by 4-bit commands and 16-bit payload. The bit indexed from 16 to 19 have been inserted in order to give time to the receiver to decode the 4 command bits.

During a write operation (from master to slave) the *SDO* forwards the command and the payload from *SDI*, in order to check if the data has been received properly. During a read operation the *SDO* forwards the command bits followed by the corresponding 16-bit data value. Table 3.5 shows the SPI commands decoded by the ASIC. Most significant bit indicates the read/write operation: MSB = 0 (write), MSB = 1 (read).

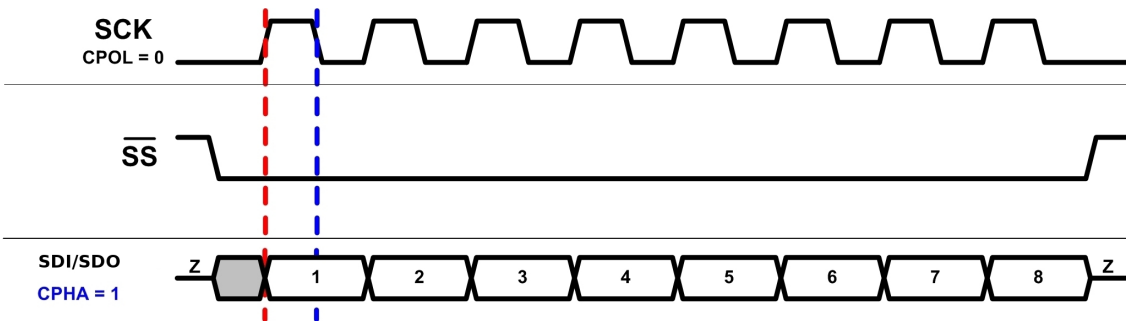


Figure 3.21: SPI interface timing diagram.

SPI Command	Not used	Payload
4 bit	4 bits	16 bits

24 0

Figure 3.22: The SPI command word.

Value	Description
0/1 000	Write/Read Pointer Register
0/1 001	Write/Read Data Register addressed by the Pointer
0/1 010	Write/ Read SPI Status Register
0111	Reset EoC Status Register
1111	Read EoC Status Register

Table 3.5: SPI commands

The Control logic consists of a set of registers for the ASIC configuration and a monitor. The Pointer Register, Data Register and EoC Status Register have direct access to the SPI interface and read/write operations are performed by one transaction only. While the other registers must be addressed by the Pointer Register, thus read/write operation requires two transactions: the first one to set the Pointer and the second one to read/write the Data Register. During the second transaction, the local logic transfers data from the ASIC's register addressed by the Pointer to the SPI internal Data Register and vice versa. A dedicated address is used to require the SPI interface information through the SPI Status Register, reporting the status of the SPI slave. The SPI Status register has 16-bit defined in the Table 3.6 and it is used to report the SPI interface status. In case of proper operation, the Status Register should always be equal to 0.

Position	Description
15	1 during transmission from slave to master Reading SPI Status should be always 0 otherwise previous transmission failed
14	1 when Dara Register must be read
13	1 when Data Register has been overwritten
12	1 when Pointer Register must be read
11	1 when Pointer Register has been overwritten
<10:0>	Not used

Table 3.6: SPI Status Register content.

The SPI Pointer Register is used to address the data within three address spaces: Bias Configuration Register (BCR), End of Column Configuration Register (ECCR) and Pixel Configuration Register (PCR). In order to reduce the number of transactions required for the whole ASIC configuration, the SPI interface implements the auto increment address mode for both write and read operations. The bit in position 15 of the Pointer Register is reserved for this purpose, and when it is set to 1, the Pointer value is incremented at every SPI data transmission, always starting from address 0. The Figure 3.23 depicts the SPI word content depending on which register is addressed.

The content of BCR, ECCR and PCR registers are listed in the tables in Appendix A.1.

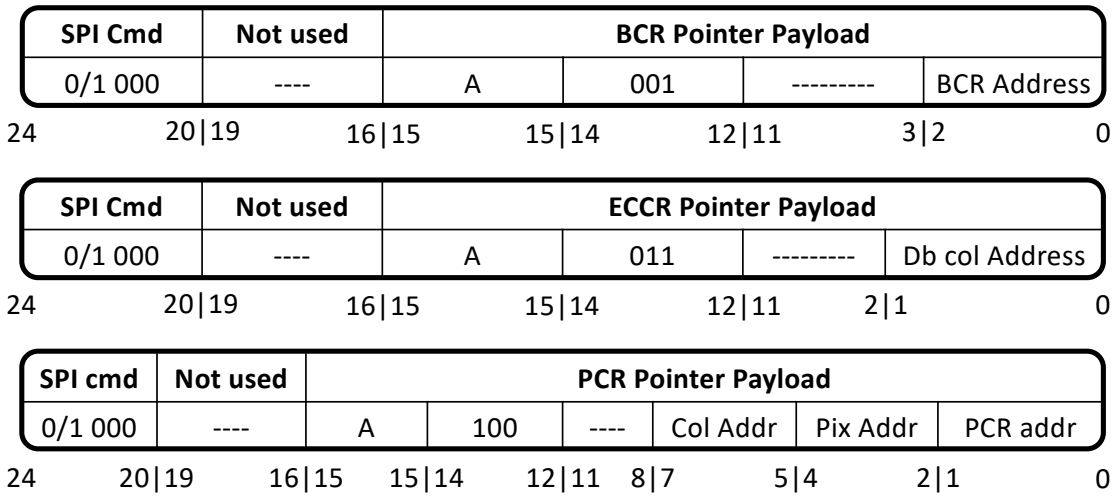


Figure 3.23: The SPI point addressing the BCR, ECCR and PCR registers.

3.7.2 Data encapsulation

The data stream includes K codes, which are 8b10b embedded symbols providing additional information. Table 3.7 shows the whole list of used symbols. Each K code is transmitted as a group of four in order to maintain the 32-bit data format.

The FIFO OUT size are 32x33 (32 data bits + K control), while the FIFOs 0/1 are 8x32 (8 words for FIFO MSB=0 and 8 words for FIFO MSB=1). The double column can be programmed through the SPI interface (ECCR register, bit 14) to send out Align comma codes. In this configuration, no other actions are performed until the align mode is not released. During normal data acquisition, the Idle comma is sent out whenever the End of Column output FIFO is empty, until new data is available to be transmitted.

Codes	Hex	Use	Description
28.0	1C	Frame header	New Coarse Counter frame
28.1	3C	Align Comma	Forced from SPI configuration
28.2	5C	Roll-over header	Coarse Counter roll-over
28.3	7C	Status header	Next words are Status
28.4	9C	CRC header	Next word is CRC
28.5	BC	Idle comma	EoC output FIFO is empty
28.5	DC	Not used	Not used
28.5	FC	Do not use	Can interfere with align comma

Table 3.7: K codes encoded with 8b/10b protocol.

An example of data stream is reported in Table 3.8, where together with the events payload and status payloads of pixels there are some additional information, like the status payload of the EoC shown in Figure 3.24 and CRC frames.

EoC OUT FIFO loss	EoC IN FIFO loss	Event counts
8 bits	8 bits	16 bits

Figure 3.24: Status word of End-of-Column.

According to the configuration register End of Column Configuration Register (ECCR) the insertion of the status words in the data can be skipped. Also, the EoC can be configured to work in raw data mode, where only data are transmitted to the serialiser

without any header, trailer, frame count, status or CRC values. Can be used during the test pulse insertion or for any other debug reason.

FIFO position	Data
1 (FPGA first received data)	K28.8 (Frame header)
2	Frame number (16-bit)
3	Event payloads Column 0
...	Event payloads Column 1
n	K28.2 (Coarse counter Roll-over header)
n+1	K28.3 (Status leader)
n+2	Status payloads Column 0 (x4)
n+6	Status payloads Column 1 (x4)
n+10	End of Column Status payload
n+11	K28.4 (Checksum header)
n+12	CRC value
n+13	K28.0 (New frame header)

Table 3.8: ALCOR output data stream.

3.7.3 Cyclic Redundancy Check

A 32-bit Cyclic Redundancy Check (CRC) is added to the data stream, in order to verify the data integrity after the serial link. The CRC is the reminder of the polynomial long division between the message and a generator polynomial. The polynomial form, which has been used for the CRC code, is the following:

$$CRC = X_{32}+X_{26}+X_{23}+X_{22}+X_{16}+X_{12}+X_{11}+X_{10}+X_8+X_7+X_5+X_4+X_2+X+1 \tag{3.11}$$

which the hexadecimal value is ”0x82608EDB”. This is the CRC32 implemented also in Ethernet communications. This CRC32 code has a Hamming Distance (HD) of 4 for messages up to 91607 bits, $HD = 3$ for messages up to 128 Kb (131072 bits) and $HD = 2$ for messages up to $(232 - 1)$ bits [48].

The receiver can verify the data integrity applying the same algorithm to the message and the received CRC code, the correct result for the computed CRC should be equal to 0. The EoC circuit updates the CRC code with every transmitted data and K code (the corresponding 32-bit hex value), with the exception of the Idle command

which is inserted after the output FIFO. CRC is initialized at ”0xFFFFFFFF” each time is transmitted and a new computation starts.

3.7.4 Double data rate output register

The FIFO readout of EoC are serial data transmission between the chip and the FPGA. This operation is performed through a Double Data Rate (DDR) serialiser per two column at clock frequency of 320 MHz, that guarantees maximum throughput of 640 Mb/s.

In order to achieve a DC-balanced output, data are encoded following the 8b/10b protocol, so the resulting bandwidth of the serial link, without the 8b/10b overhead, is 512 Mb/s. The input stage of the serialiser consists of the 32-bit data register. After that, the FSM, performs the byte selection, from byte 0 to 3, to send to the 8b/10b encoder. A single 8b/10b encoder maps each byte of the 32-bit bus of the EoC output FIFO, to the corresponding 10-bit symbols. In addition, setting the KI input signal within the incoming 32-bit data, the encoding circuit can generate any control symbol (comma symbols) expected by the 8b/10b protocol. Then encoded data are split in an even/odd bit position and sent to the shift registers. Parallel to serial conversion, it is performed by two different shift registers, one for even bits (triggered by the falling edge of the clock) and the other one for odd bits (triggered by the rising edge of the clock). The two serial data streams are multiplexed to the DDR output and the selection is done by the clock signal itself. The least significant bit is transmitted first, and the byte order is from 0 to 3.

3.7.5 Reset

The reset signal is an active low signal, and it has a dual purpose. Asserting this signal low for 10 clock cycles, it performs the Coarse Counter synchronous reset, while asserting this signal low for 24 clock cycles, it performs both the counter reset and the global reset of the whole chip, configuration values included. The internal reset signal remains asserted while the external reset is active. For a correct operation, two reset procedures must be separated for at least four clock cycles. The external reset signal must be set to high after power-on for at least four clock cycles in order to initialize

the state machine performing the reset operations, and it should be synchronous with the system clock. The Figure 3.25 depicts the time diagram of the reset process, where *cnt_n_reset_Pixel0* is the signal for counter while *n_reset_Pixel0* is the signal for global chip.

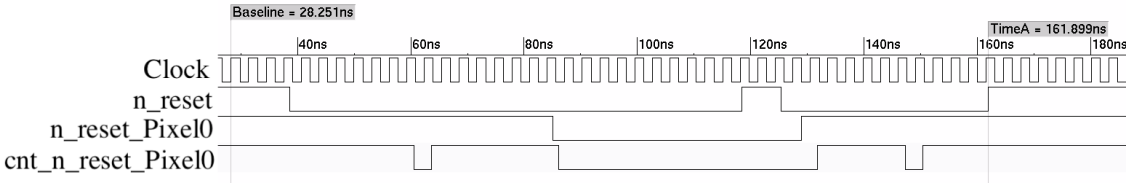


Figure 3.25: Reset time diagram of the ALCOR chip. Depending on the duration of the n_reset signal at the pixel level the registers (n_reset_Pixel)) or the course counters (cnt_n_reset_Pixel0) are reset.

3.8 Radiation protection

The main application where ALCOR is meant to be employed is not an experiment exposed to radiation. Nevertheless, the chip has been designed using rad-hard techniques to allow ALCOR to be also used in other contexts (e.g. space applications). A SEU event occurs when an ionizing particle has enough energy to change the state of a bit in a register from logic-0 to logic-1. This kind of error does not damage the transistor's or circuits' functionality [49] since it is possible to recover the correct behaviour with Single Event Upset (SEU) tolerant techniques.

Rad-hard solutions have been applied at the pixel level only on Pixel Configuration Register (PCR) and Finite-State Machine (FSM) in order to guarantee the correct behaviour of the chip in case of SEU. Two solutions have been adopted, Triple Modular Redundancy (TMR) for PCR registers and Hamming Code for the FSM state registers.

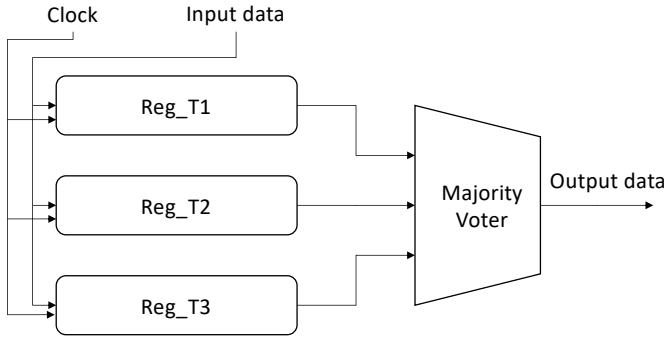
In digital simulation tools, it is possible to replicate a SEU event with a command that placed in the test-bench changes the bit value of a defined signal/register:

Code Listing 3.1: VHDL command to simulate a SEU event in a register

```
wait for 500 ns;
-- Sets the bit in 5th position of cfg_reg to logic-0
nc_deposit (source => ":PATH.cfg_reg[5]" , value => "0");
-- Sets the bit in 2nd position of cfg_reg to logic-0
nc_deposit (source => ":PATH.cfg_reg[2]" , value => "1");
```

3.8.1 Triple Modular Redundancy

Triple Modular Redundancy (TMR) is fault-tolerant solution where a sensible system is triplicated and the output is processed by a majority voting system in order to generate a single output. If one of the three system fails, the other two systems can correct and mask the fault. Figure 3.26 shows a practical example applied to registers where the input data is written into three different registers and the readout phase is performed following the truth table of the majority voter. More complex TMR solutions, foreseen the triplication of input and clock route in order to avoid SEU effects on transition signals.



Reg_T1	Reg_T2	Reg_T3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 3.26: Triple modular redundancy architecture applied to registers. The truth table on the right shows the output of the majority voter when a SEU affects one of the bit in one of the register. This bit is expressed in red colour, while the blue colour expresses the correct value.

A simulation example of the TMR implementation is depicted in Figure 3.27. The PCR3 register is triplicated, and the configuration value is stored in the three registers at time 318 *ns*. After a certain amount of time a SEU event is simulated in the bits position *PCR3_T2[11]*, *PCR3_T2[10]*, *PCR3_T2[9]*. However, the *PCR3_Out* is not changed, which means that the TMR is well-implemented and efficient. The TMR is a technique that occupies area and increases the power consumption. Thus, this solution can be applied only if the environment specification requires strong radiation protection, like in high energy physics or space experiments.

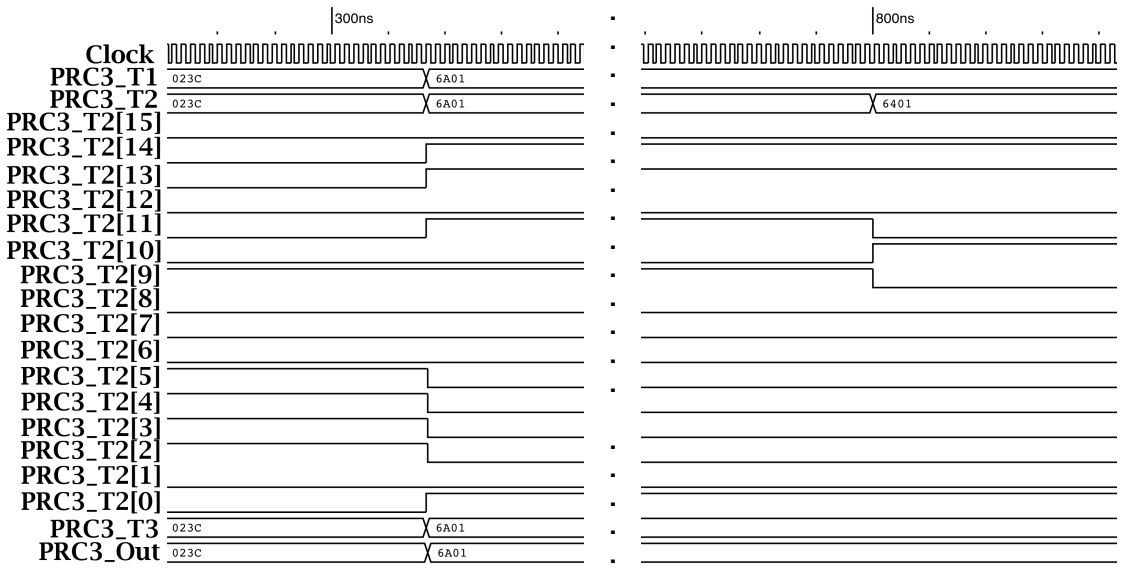


Figure 3.27: Schematic time diagram of TMR simulation. The PCR3 register is affected by SEU event on bit position 11 at time 800 ns. The SEU event does not affect the PCR3_Out which continues to generate the correct output.

One major drawback of TMR solution, is when a SEU event happens on the same bit position of two registers. In this case, the majority goes to the wrong bits, generating thus a value affected by radiation error. Therefore, in order to reduce the probability of SEU on the same bit registers, the floor-plan and placement routines maximise the allowed distance between the triplicate modules as show in Figure 3.28. The command *createInstGroup* defines logic boundaries on the layout, while *addInstToInstGroup* defines the registers that will be instantiated in those group regions. In this way triplicated registers are placed following physical position rather than routing algorithms.

```
createInstGroup tmrGroup1 -region 342 223 483 314
createInstGroup tmrGroup2 -region 342 314 483 404
createInstGroup tmrGroup3 -region 342 404 483 495

addInstToInstGroup tmrGroup1 {I_Pixel_ctrl/i_configuration/PCR0_int1*}
addInstToInstGroup tmrGroup1 {I_Pixel_ctrl/i_configuration/PCR1_int1*}
addInstToInstGroup tmrGroup1 {I_Pixel_ctrl/i_configuration/PCR2_int1*}
addInstToInstGroup tmrGroup1 {I_Pixel_ctrl/i_configuration/PCR3_int1*}

addInstToInstGroup tmrGroup2 {I_Pixel_ctrl/i_configuration/PCR0_int2*}
addInstToInstGroup tmrGroup2 {I_Pixel_ctrl/i_configuration/PCR1_int2*}
addInstToInstGroup tmrGroup2 {I_Pixel_ctrl/i_configuration/PCR2_int2*}
addInstToInstGroup tmrGroup2 {I_Pixel_ctrl/i_configuration/PCR3_int2*}

addInstToInstGroup tmrGroup3 {I_Pixel_ctrl/i_configuration/PCR0_int3*}
addInstToInstGroup tmrGroup3 {I_Pixel_ctrl/i_configuration/PCR1_int3*}
addInstToInstGroup tmrGroup3 {I_Pixel_ctrl/i_configuration/PCR2_int3*}
addInstToInstGroup tmrGroup3 {I_Pixel_ctrl/i_configuration/PCR3_int3*}
```

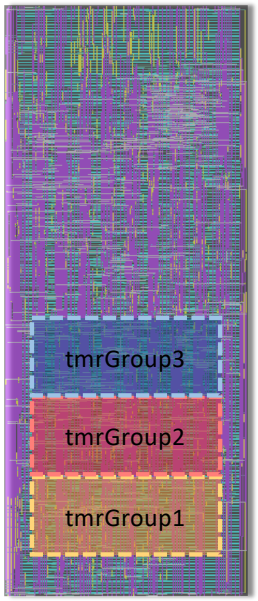


Figure 3.28: Implementation of TMR technique on layout phase of the design. On the left the code to implement during place and route phase. On the left an image of group implementation on the digital block of the pixel.

3.8.2 Hamming Code

Hamming code is one of the linear error-correction codes that is able to detect two bits error or a correct one bit error. This method introduces extra bits to data in order to perform parity bit check. As a general rule, the position of the parity bit in the encoded data is chosen in such a way that the index-XOR is equal to 0. Thus, index position 1,2,4,8 (in binary: 1,10,100,1000) is used as parity bits and is filled with bitwise XOR of data. The remaining index positions are used as data bits. Figure 3.29 depicts a scheme of a 4-bit register encoded in a 7-bit register. During the readout phase, a bit parity coverage operation is performed on the stored data. In case one of these operations results as logic-1, it means that there is a bit error. The index "C1C2C3" is used to point at the bit affected by SEU. As a general rule, data of n-bit length, the Hamming code is equal to k-bit length, where m is the number of parity bits:

$$k = 2^m - 1 \tag{3.12}$$

$$n = 2^m - m - 1 \tag{3.13}$$

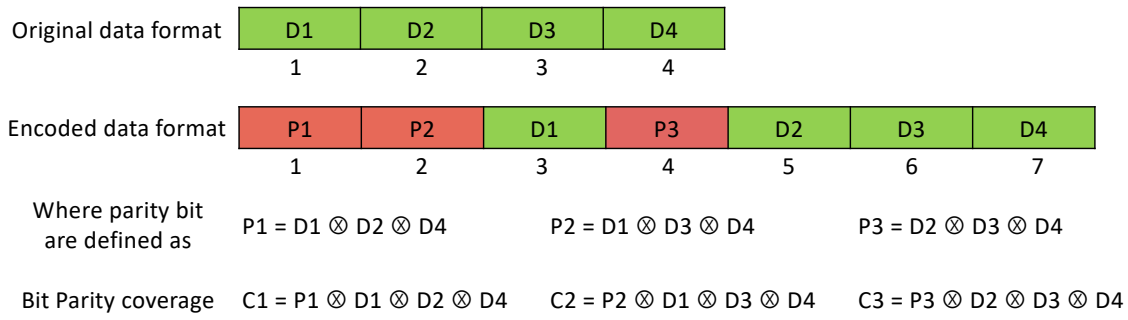


Figure 3.29: Implementation of Hamming code of 4 bit register to 7 bit register. The original data format is encoded in Hamming code including parity bits (P1/P2/P3) defined with bit-XOR operations. The bit parity coverage is used to index the bit affected by SEU event.

In ALCOR, Hamming code has been used to define the state registers of FSMs employed at the pixel level. This operation is done in the RTL code, where the state register is defined as constant and assigned with the encoded state. The Appendix A.2 reports an example of a Mealy FSM written in VHDL language, where the state registers are implemented with Hamming code. The example shows how to define the correct and wrong state, and how to implement the FSM architecture in order to detect SEU. The wrong register states are defined changing one bit per position from the correct state. The state diagram of this FSM is depicted in Figure 3.30, where green states are the correct nodes while the red states are the wrong nodes. The only way to access the wrong states is due to SEU event on the state register. Indeed, these states have no entry arrow but only an exit arrow that points to the next correct state in order to recover the proper behaviour of the FSM. When an SEU event happens in the state register, the FSM generates a signal to notify the radiation error and the normal output signal of the state is updated correctly. In the next state, the correct value of the state register is updated. The check and correction are done at each clock cycle in order to minimise the errors due to radiation particles. In case of SEU detection, this is counted and notified in the Status word, as explained in Section 3.5.

The time diagram depicted in Figure 3.31 is a post-layout simulation example of a FSM where the state register is affected by SEU event in *FSM_state[3]* bit position at simulation time 1990 ns. The *FSM_state* register changes from $0x33$ to $0x3\boldsymbol{B}$. Although the wrong bit is given, the next state and output are generated correctly, in this case

Read pixel stimulates the FSM and the state changes to a correct value of $0x2D$ at the simulation time 2020 *ns*.

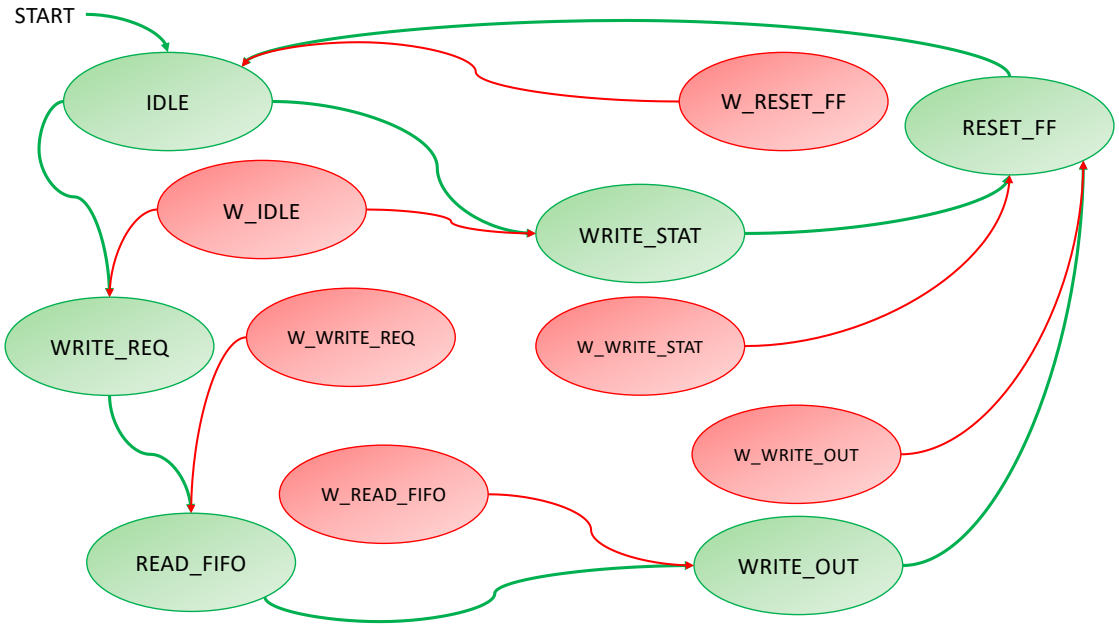


Figure 3.30: Post-layout simulation of Hamming code applied to FIFO readout. This FSM is defined with six states where the green nodes are the correct states, while the red nodes are the wrong nodes that are accessible only in case of SEU event on the state register. From the red nodes it is possible to restore the correct behaviour.

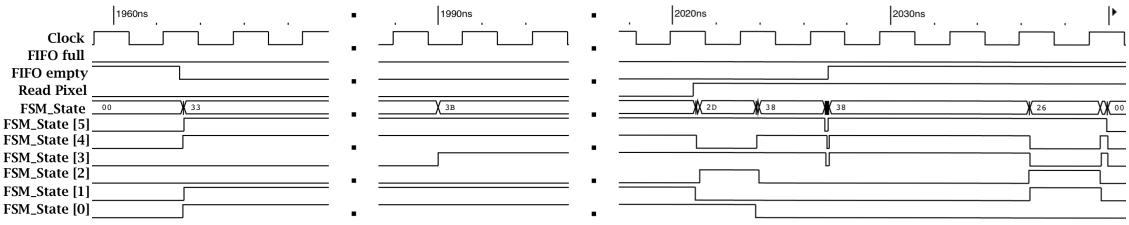


Figure 3.31: Post-layout simulation of Hamming code applied to FIFO readout FSM. This simulation example shows hot the state register is restored after a SEU event generated by simulation.

3.9 Conclusions

ALCOR is a versatile SiPM readout ASIC, the 32-pixel matrix structure makes this chip suitable for 3D integration with the silicon sensor. The first prototype is implemented to verify the behaviour of such a complex circuit at cryogenic temperature. The readout and data architecture are designed to be easily scalable to large matrices in the following version. The chip performs time-based measurements of the ToA and ToT of signals generated from a SiPM. Four low-power TDCs allows to achieve a time binning of 50 ps at the maximum system clock frequency of 320 MHz. An operation clock down to 40 MHz expands the usability of the chip for very low-power and low-rate applications with less stringent needs in terms of time resolution. The timestamps are internally multiplexed among all the pixels and serial data are transmitted through four LVDS at a data rate of 640 Mb/s.

This chip prototype, using a CMOS 110nm technology node, has been submitted to fabrication during Q3-2019.

Chapter 4

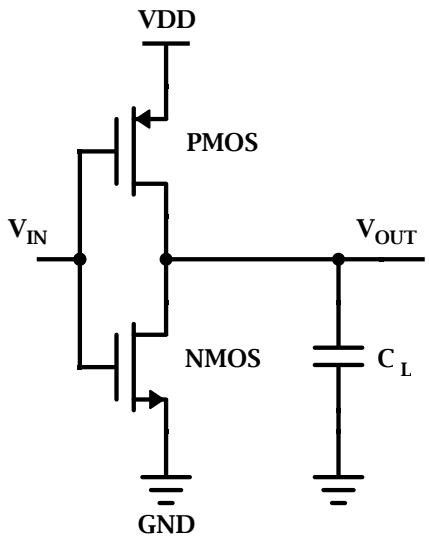
Silicon implementation and cryogenic characterisation of key IPs.

The advantage to place the readout electronics inside the detector near the sensor reduces the input capacitance at the input node of the Front-End (FE) amplifiers, thus minimising noise and improving the signal integrity. In Neutrino or Dark Matter experiments employing photosensors operating in liquid noble gases, the whole photodetector works at cryogenic temperatures. Extensive literatures demonstrate the advantages of the operation of the front-end readout electronics at low temperature. Specifically, decreasing junction temperatures improves the speed of transistors, noise and current drive [82, 25, 75]. Most of the failure mechanisms in the transistor that are temperature dependant such as electromigration, stress migration and thermal cyclic become negligible at cryogenic temperature. One of the major drawbacks of working at 77 K temperature is given by hot carrier degradation, which increases the threshold voltage and may induce an accelerated device ageing of the CMOS transistor[44]. The latter effect has been demonstrated in the recent studies, and can be partially mitigated in the analogue circuit by avoiding minimum length transistors and/or reducing the power supply voltage [45, 84, 63, 50].

4.1 Delay propagation in CMOS

In the digital domain, circuits are designed using standard cells already defined and characterised by the technology vendor. This implies that an accurate SPICE model of the transistors is not provided by the foundries. A reduction of the digital power supply, which would act on the minimization of the hot carrier degradation effect, is also limited by the library corner provided by the foundry, usually within a 5% range of the nominal power supply. Furthermore, transistor and digital standard cell models below $-40^{\circ}C$ are usually not provided by the technology vendor. Therefore, SPICE tools use extrapolated models to simulate circuits at 77 K temperature.

The delay time in a circuit can be characterised in view of the performance of a CMOS inverter which is a basic circuit composed by two MOSFETs as depicted in Figure 4.1. The majority of carriers in PMOS[1] transistor are holes while in NMOS[2] are electrons. When high voltage (logic-1) is applied to the input V_{IN}, the PMOS transistor does not conduct, while the NMOS transistor conducts pulling the V_{OUT} to ground. Opposite situation happens when low voltage (logic-0) is applied to the V_{IN}, the NMOS does not conduct, while the PMOS conducts pulling the V_{OUT} to VDD.



V_{IN}	V_{OUT}
Logic-1	Logic-0
Logic-0	Logic-1

Figure 4.1: Schematic circuit of a CMOS inverter.

[1] P-type source and drain diffuses on N-type substrate.

[2] P-type substrate with N-type source and drain diffused on it.

The propagation delay (t_p) of an inverter is defined as the average of the low-to-high (t_{PLH}) and the high-to-low (t_{PHL}) propagation time:

$$t_p = \frac{t_{PLH} + t_{PHL}}{2} \tag{4.1}$$

Where t_{PLH} and t_{PHL} are defined as time necessary for the output V_{OUT} to reach the 50% of voltage value after an input signal, as depicted in Figure 4.2. The 50% of voltage is defined as the mean value between the output high voltage (V_{OH}) and the output low voltage (V_{OL}). This measure is defined as threshold voltage (V_{TH}).

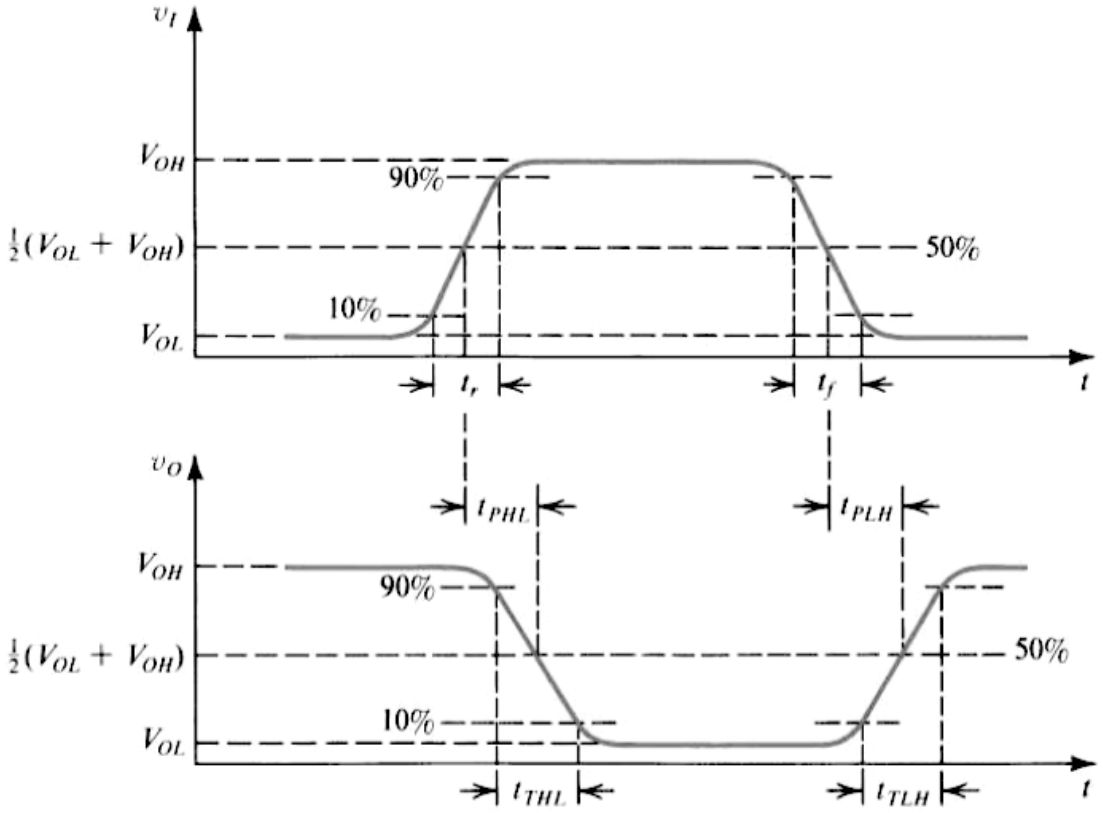


Figure 4.2: Schematic circuit of a CMOS inverter.

At the transistor level the propagation delay depends on the width (W) and length (L) of transistors, the mobility of electrons (μ_n) and holes (μ_p) in the channels and on the threshold voltage.

The low-to-high transition is expressed on the parameter of PMOS transistor, while the high-to-low transition is calculated considering the NMOS parameter:

$$t_{PLH} = \frac{C_L \frac{V_{OH}}{2}}{\frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_p(V_{OH} + V_{TH_p})^2} \tag{4.2}$$

$$t_{PHL} = \frac{C_L \frac{V_{OH}}{2}}{\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_n(V_{OH} - V_{TH_n})^2} \tag{4.3}$$

Where C_L includes the input capacitances, the parasitic drain/bulk capacitance and wiring capacitance, while C_{ox} defines the oxide capacitor of the transistor. Although, the equations do not consider the temperature variation on the propagation delay, and it has been observed at cryogenic temperature that there is an increasing of electron/hole mobility because of reduced carrier scattering due to lattice vibration. Moreover, due to the hot electron effect, the threshold voltage is also increased. Some electrons that may get enough energy to overcome the barrier between the body and the gate deposit negative charge on the gate, which leads to an increase in threshold voltage by increasing flat band voltage [84]. This variation is depicted in Figure4.3 where compared with temperature, the mobility increases exponentially, while the threshold voltage increases linearly.

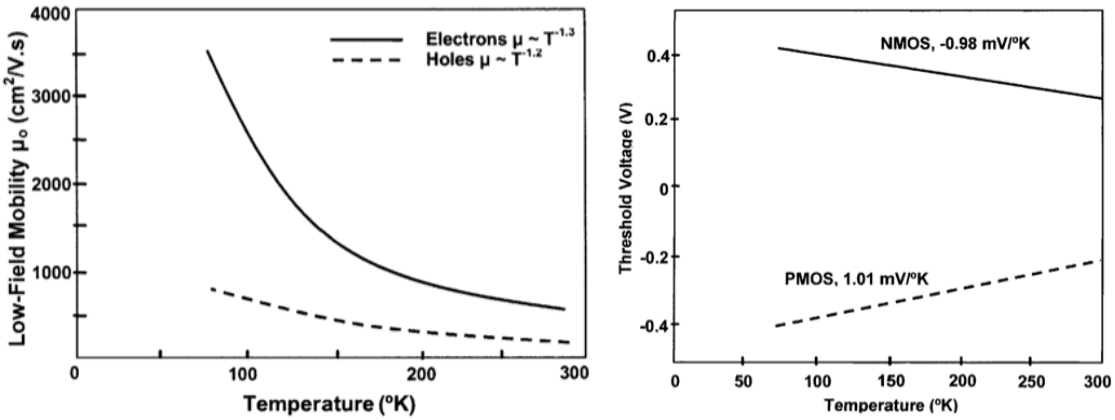


Figure 4.3: Variation of the mobility and threshold voltage when the temperature decreases.[81].

Considering Equation 4.2 and Equation 4.3, it is possible to assume that the propagation delay at low temperature may change depending on μ and V_{TH} variations. Therefore, a preliminary Application specific integrated circuit (ASIC) has been produced and this chapter will discuss of some significant digital circuit that have been tested and analysed at cryogenic temperature in order to compare the results with SPICE simulation.

4.2 The Test Chip

A Test Chip (TC) has been fabricated in order to assess the behaviour at cryogenic temperature of critical digital circuits. The layout of this ASIC is depicted in Figure 4.4, where a digital synchronisation and a clock buffer followed by a Low Voltage Differential Signaling (LVDS) transmitter are implemented. The ASIC includes also analogue circuits that will not discuss in this thesis.

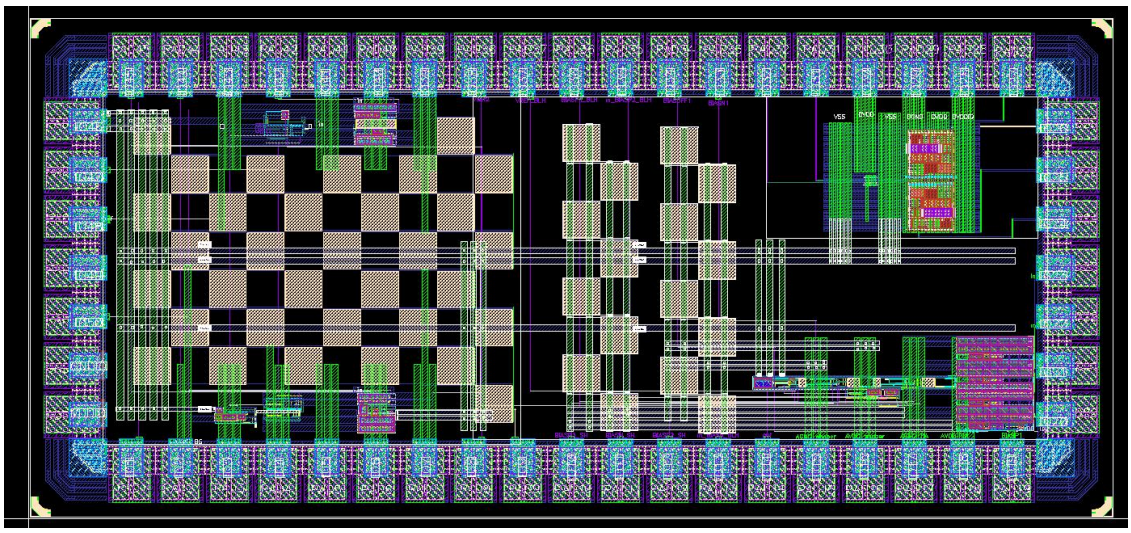


Figure 4.4: Layout of the Test Chip ASIC.

The LVDS driver is particularly interesting because it is a mixed-signal design combining digital gates with analogue circuitry, including blocks, such as the common mode feedback loop, which can be prone to stability issue. In addition, it employs transistors on two different power domains. The synchronisation circuit is a critical block of ALCOR because it has been implemented to synchronise hand shaking signals between

the single channel and EoC. A synchronisation delay error can lead to the loss of data and therefore may compromise the ASIC functionality. A dedicated test at cryogenic temperature is necessary in order to asses the functionality of this module and have a comparison with SPICE simulations.

4.2.1 Experimental Setup

The test setup allows to evaluate the timing performance of digital circuitry in both the room and cryogenic temperatures. Figure 4.5 depicts the schematic of the setup to test the ASIC that is wire bonded to a custom PCB. The test board is equipped with six SMA connectors, listed in the Table 4.1, in order to provide the clock and asynchronous signal and to read the readout LVDS output.

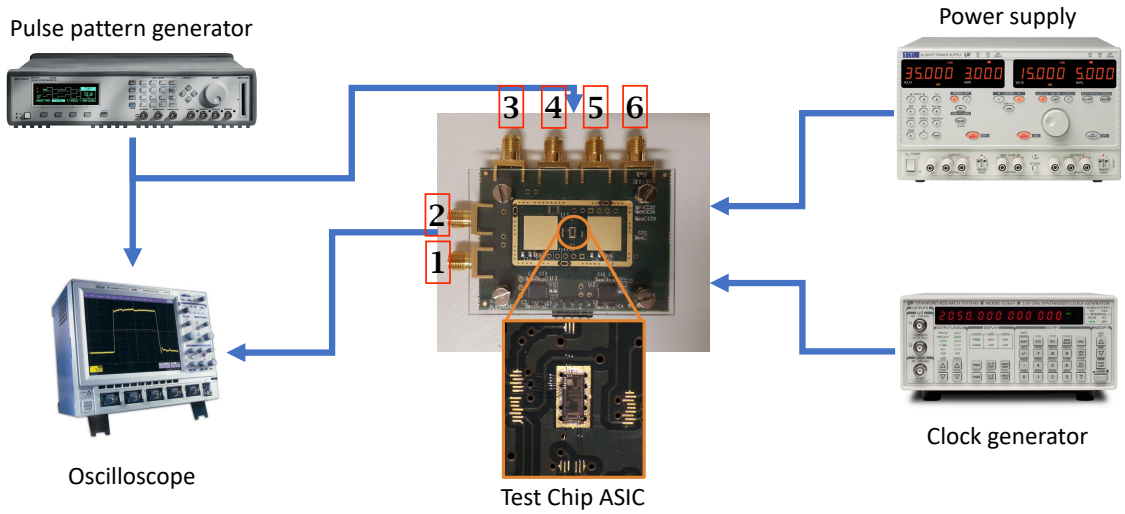


Figure 4.5: Test setup for the electrical characterisation of TC ASIC.

Two commercial LDOs are used to regulate the power supply of 4 V to 1.2 V for the digital circuits and 2.5 V for the LVDS transmitters. A clock and a digital pattern generator provide external stimuli, while the output signals are captured by an oscilloscope with sampling frequency of 10 GS/s [40, 77, 41, 58]. Figure 4.6 depicts the test at cryogenic temperature performed using liquid Nitrogen which has a temperature of 77 K very close to the liquid Argon temperature of 87 K. Thanks to SMA connectors, the cables were easily brought outside the dewar, reducing at minimum signal interference due to connections.

SMA port	Test Chip signal	Direction	Differential/CMOS
1	Synchronised (+)	Output	Differential
2	Synchronised (-)	Output	Differential
3	Clock (+)	Output	Differential
4	Clock (-)	Output	Differential
5	Asynchronous	Input	CMOS
6	Clock	Input	CMOS

Table 4.1: Input/Output SMA ports of the test board for testing digital circuits of Test Chip.

(a) (b)

Figure 4.6: Figure (a) depicts the test setup and the dewer used to perform test with liquid nitrogen. Figure (b) depicts the test board imersed completly in liquid Nitrogen. All the cable are bring outside the dewer as show in images.

4.2.2 Digital synchronisation circuit

The synchronisation circuit, designed using 110 *nm* technology standard cells, is implemented in ALCOR to synchronise the EoC configuration and data transmission signals with respect to the reference clock phase of the digital control logic in the channel. It is particularly important to asses the time performance of the circuit at cryogenic temperature as synchronisation delay errors may compromise the ASIC functionality. Figure 4.7 shows the schematic of the module in which the asynchronous input is sampled by two Flip-Flops (FFs) at different clock edges. Then the bitwise OR output is processed in two cascade FFs in order to minimise metastability signals [24, 47]. According to the arrival time of the asynchronous signal, there is a different synchronisation time that is depicted in Figure 4.8. If the input signal occurs immediately before the trailing edge of the clock, the synchronisation lasts for $1\frac{1}{2}$ clock period. While, if the input signal occurs immediately after the falling edge of the clock, the synchronisation lasts for $2\frac{1}{2}$ clock periods. The time difference of these two values is equal to 1 clock period.

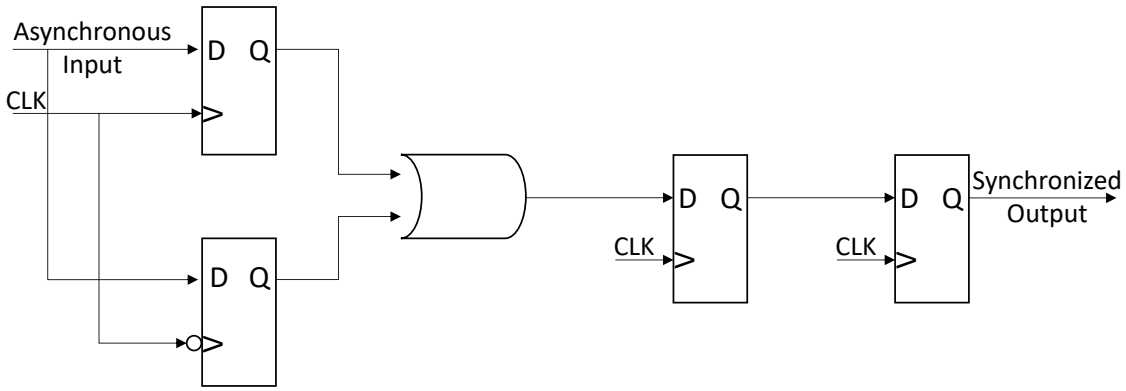


Figure 4.7: Schematic diagram of synchronisation module. The two FFs sample the asynchronous input signal with different clock phase. One FF samples at the rising edge of the clock, while the other FF samples at the falling edge of the clock. The synchronised signal is processed into a bitwise OR logic gate. Eventually, the outcome of the logic port passes through two FF in cascade that minimise potential metastability signals.

The pulse pattern generator provides the asynchronous signal of 250.1 μs period, while the clock frequency is set from 40 MHz up to the maximum value settable by the clock generator of 250 MHz. This test configuration allows to scan the clock period with the asynchronous signal and obtain different synchronisation time. The goal of this test is to measure the time delay observed at 77 K respect to room temperature,

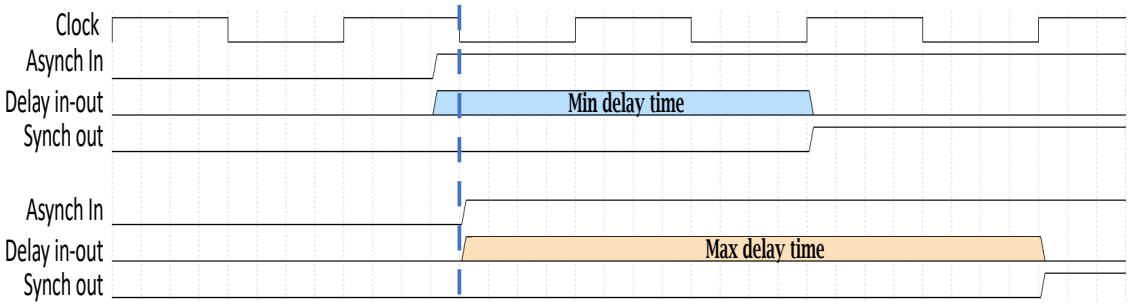


Figure 4.8: Time diagram of synchronisation module. Depending on the arrival time of the asynchronous signal, the synchronisation time of the input takes $1\frac{1}{2}$ if the signal occurs immediately before the falling edge of the clock, otherwise the synchronisation lasts for $2\frac{1}{2}$.

and if this time constraint can be predicted using SPICE models. It must be pointed out that full transistor models extracted at 77 K are not available for the used technology, therefore the simulator employs extrapolated parameters.

The time delay analysis is performed considering measuring maximum and minimum synchronisation time. These two delays are very clear and distinct values that are distinguished by the clock trailing edge as explained in the Figure 4.8. The correct behaviour of the synchronisation module is shown in the Figure 4.9, where the time window is linearly respected with an ideal curve, in both temperatures.

The time delay is calculated from the asynchronous arrival time to the synchronised output, and results are reported in the graphs in Figure 4.10 and in Figure 4.11. Measured values are showed as a continuous line while test values are showed as a dash line. It is possible to observe that the experimental value presents a systematic error due to the cable connection delay of $\sim 5.73\ ns$. Removing this constant value, the curves are nearly overlapped, demonstrating a superimposed trend. From this it is possible to assume that the analogue simulator approximates reasonably well the experimental behaviour of the circuit at 77 K.

The time measurement at cryogenic temperature shows a minor delay time, this can be well evaluated in the time difference graphs in Figure 4.12 and in Figure 4.13 for maximum and minimum synchronisation time respectively. In the first case the delay goes in a range between $\sim 420\ ps$ and $\sim 540\ ps$, while in the second case the delay goes in a range between $\sim 430\ ps$ and $\sim 580\ ps$. The simulated curve is almost linear over all

the x-axis values, while the tested value has some spikes at higher frequency probably due to instrumentation accuracy used to perform the test. Nevertheless this does not affect the behaviour of the synchronisation module, and the measurements show that no particular issue with the synchronisation circuit should be expected at 77 K.

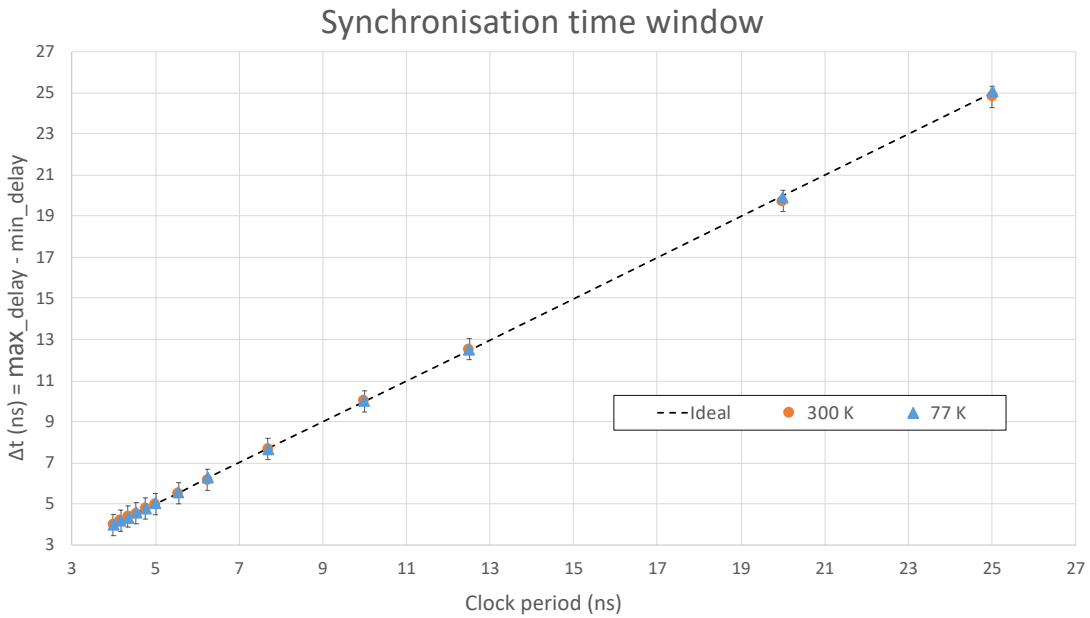


Figure 4.9: The time window of the synchronisation module is respected in both 77 K and 300 K temperatures. The points lay on the ideal curve within the error bar.

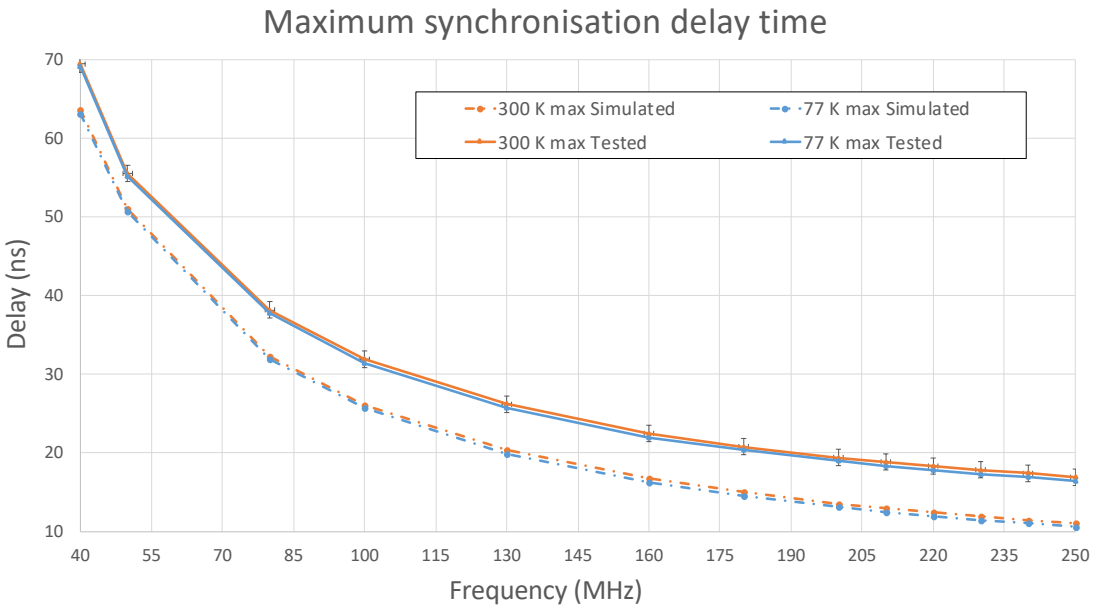


Figure 4.10: Maximum delay time between input signal and synchronised output signal. Graphs show results of simulated (dashed line) and measured values (continuous line) at two different temperature, 300 K and 77 K. In both graphs the blue curves and the orange curves are nearly overlap, showing the same trend.

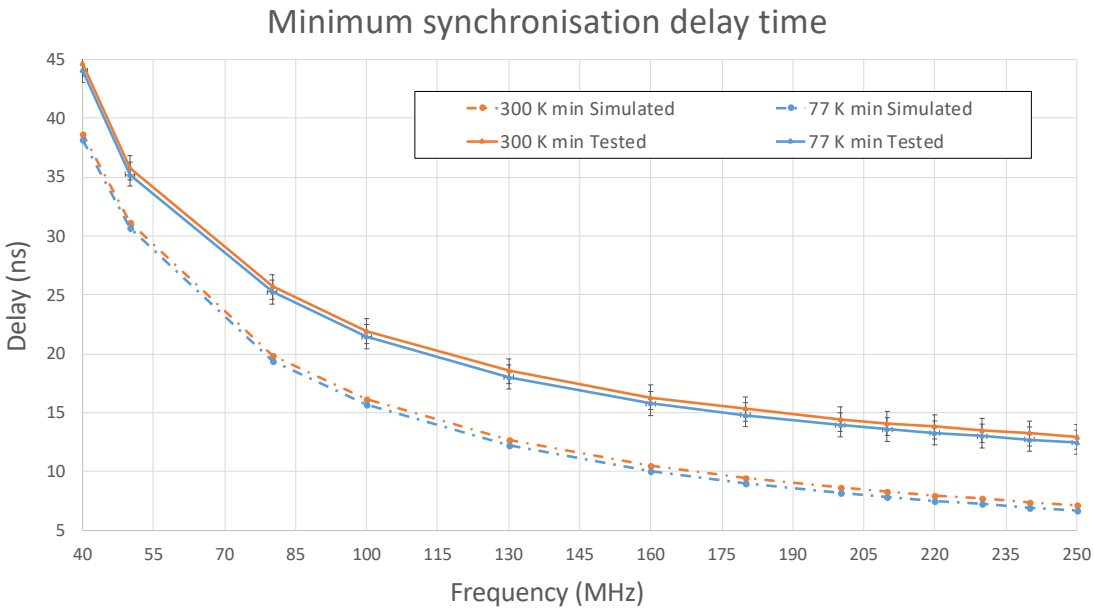


Figure 4.11: Minimum delay time between input signal and synchronised output signal. Graphs show results of simulated (dashed line) and measured values (continuous line) at two different temperature, 300 K and 77 K. In both graphs the blue curves and the orange curves are nearly overlap, showing the same trend.

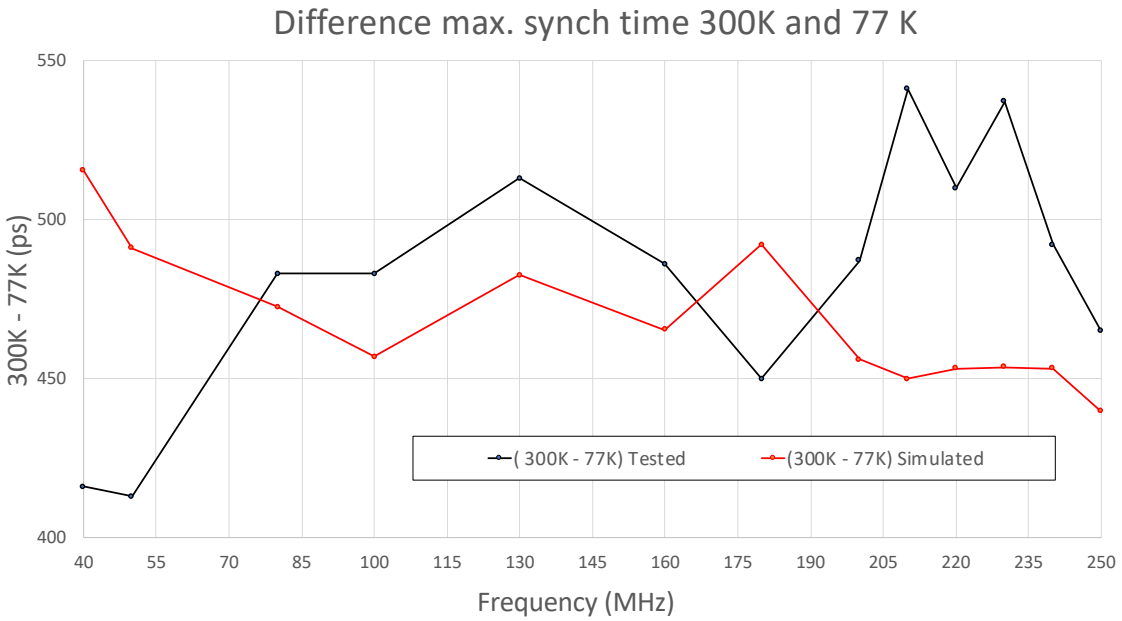


Figure 4.12: Results of maximum synchronisation delay expressed as time difference between temperature for both tested (black line) and measured (red line) values.

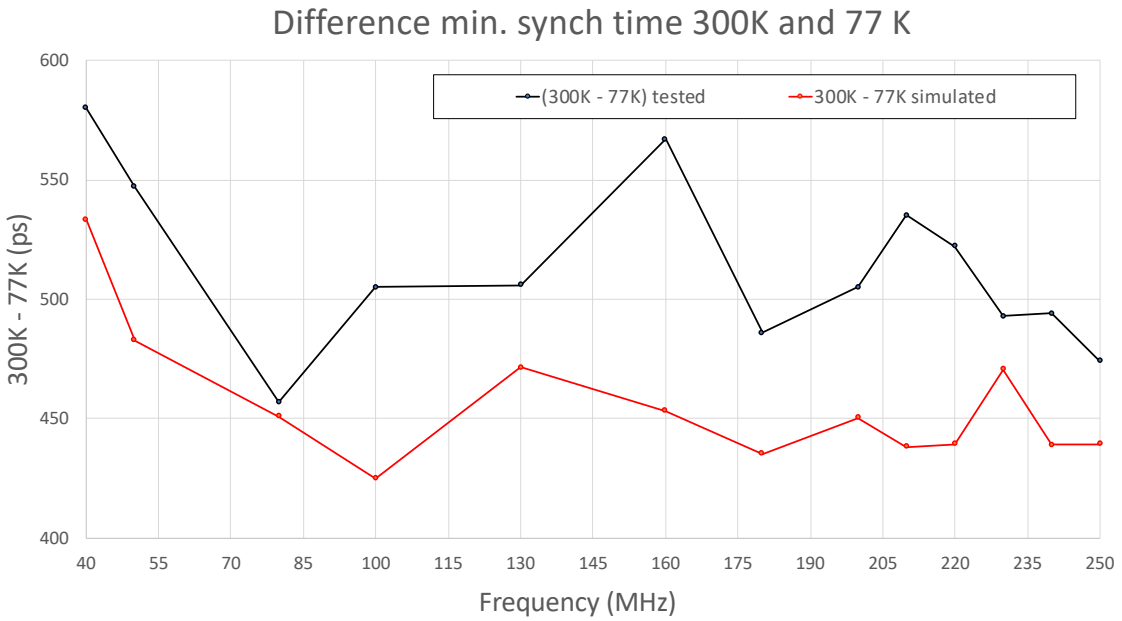


Figure 4.13: Results of minimum synchronisation delay expressed as time difference between temperature for both tested (black line) and measured (red line) values.

4.2.3 Low Voltage Differential Signaling

The Low Voltage Differential Signaling (LVDS) is a driver for high speed signalling single-ended to differential standard data transmission, and it operates at low power [46]. It is a point-to-point connection that can achieve very high data rates in the order of Gigabits per second (Gb/s). The use of LVDS reduces the effects of common-mode noise because the signal is read as the difference of the two voltages, any common noise on both lines is subtracted at the receiver. This also rejects the crosstalk effect of neighbouring lines. The standard differential signal is centred at 1.25 V common voltage, while the output swings between 1.05 V and 1.45 V. On the test board a 100 Ω termination resistor is used to match the impedance of the transmission line that connects the receiver to the driver.

The schematic diagram of the LVDS circuit implemented in the TC is depicted in Figure 4.14, where the *DataIN* is the input and *Out_neg*/*Out_pos* are the differential outputs. The *VCMREF* is defined by a voltage divider that sets the node to $\frac{DVDD}{2}$ V. While the current *VbiasP* and *VbiasN* feed the driver stage, and they are defined by switches *M1* and *M2* respectively. The cross-coupled inverter, defined by *M3* to *M6* switches, defines the input signals of the driver stage.

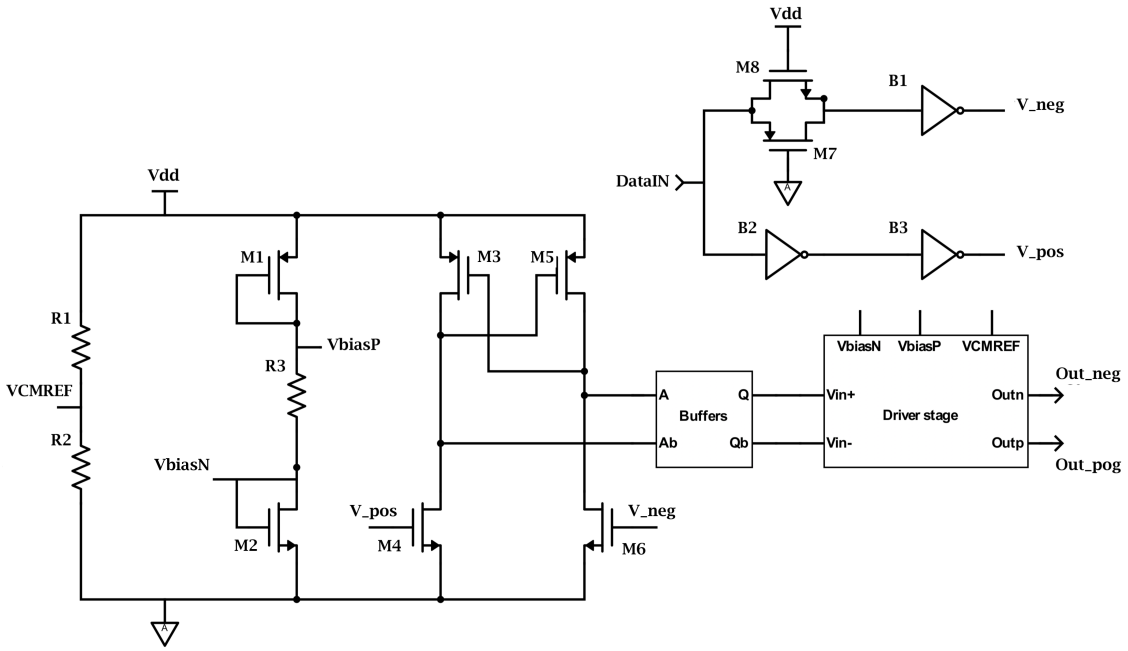


Figure 4.14: Schematic diagram of the LVDS transmitter.

The driver stage circuit, depicted in Figure 4.15 is designed with a Briged-Switches Current Sources (BSCS) which is composed by two current sources (*M12*/*M9*) and four switches (*M4*/*M5*/*M10*/*M11*) connected in a bridge formation. When a logic-1 is applied to the input *Vin+* and a logic-0 is applied to the input *Vin-*, the switches *M5*/*M10* are ON, while *M4*/*M11* are OFF in this way *OUTn* sinks the current and *OUTp* sources the current. Providing the opposite input the output signal is reversed (*M5*/*M10* are OFF and *M4*/*M11* are ON). This circuit needs to work properly, it needs a power supply of $DVDD = 2.5\,V$.

A Common Mode FeedBack (CMFB) loop amplifier is used to fix the output common voltage to 1.2 V DC level. CMFB is a differential pair stage with current mirror load, which compares the output common mode voltage on *R2*/*R3* nodes and the *VCMREF* voltage reference provided externally. The amplified error is then fed to the current source *M3* that closes the loop. The *R1C1* filter is a Miller compensation over *M3* current source to guarantee enough phase margin.

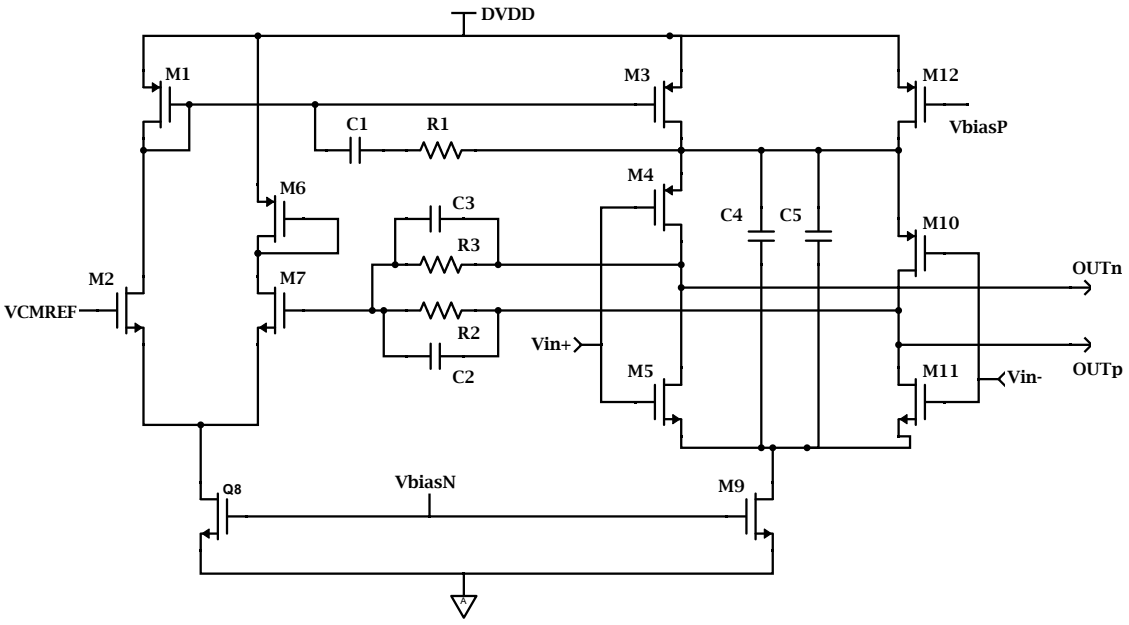


Figure 4.15: Schematic diagram of Drive Stage of the LVDS transmitter.

The LVDS driver transmitter has been tested providing a Non-Return-to-Zero (NRZ) bit stream of a PseudorRandom Binary Sequence (PRBS) of $2^{31} - 1$ pattern length to the digital buffer and the differential output is then monitored and analysed through the oscilloscope. The input data rate has been set considering the minimum and maximum working frequency of the ALCOR chip showed in Chapter 3.2 , 40 MHz and 320 MHz. The PRBS allows to stress the driver with a sequence of random bits that allows to generate the eye diagram reported in Figure 4.16. The parameters of these eye diagrams are listed in Table 4.2 for 40 MHz and Table 4.3 for 320 MHz. The Level 1 and Level 0 are respectively the mean value of the logical 1 and logical 0 of the transmitted data. Rise/fall time is the measure of the transition of the data from 10% to 90% level on the upward/downward slope of the signal. Eye amplitude, eye height, eye width and eye signal-to-noise ration have been determined as follow:

$$Eye\ Amplitude = Level1 - Level0 \tag{4.4}$$

$$Eye\ Height = (Eye\ Level1 - 3\sigma) - (Eye\ Level0 - 3\sigma) \tag{4.5}$$

$$Eye\ Width = Tmin\ Right\ Cross - Tmax\ Left\ Cross \tag{4.6}$$

$$Eye\ S/N = \frac{Eye\ Level1 - Eye\ Level0}{\sigma_{\text{Level1}} + \sigma_{\text{Level0}}} \tag{4.7}$$

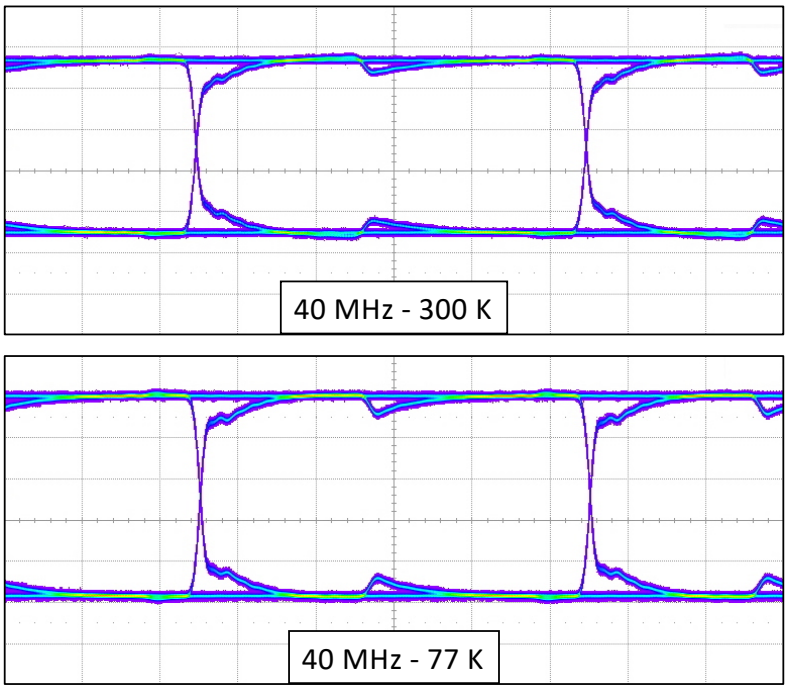
Considering eye diagrams at 300 K and 77 K, there is an increasing of the eye amplitude of $\sim$ 14% at cryogenic temperature in both 40 MHz and 320 MHz frequency domain. At low temperature there is also an increasing of rise/fall time of $\sim$ 15% at 40 MHz and of $\sim$ 30% at 320 Mhz. The eye S/N ratio and eye width remain constant showing very similar behaviour while the temperature changes.

	40 MHz (@300 K)	40 MHz (@77 K)
Level 1 (mV)	389	451
Level 0 (mV)	-396	-459
Rise Time (ps)	627	728
Fall Time (ps)	574	686
Eye Amp (mV)	785	910
Eye Height (mV)	635	730
Eye Width (ns)	24,84	24,74
Eye S/N	15,70	15,17

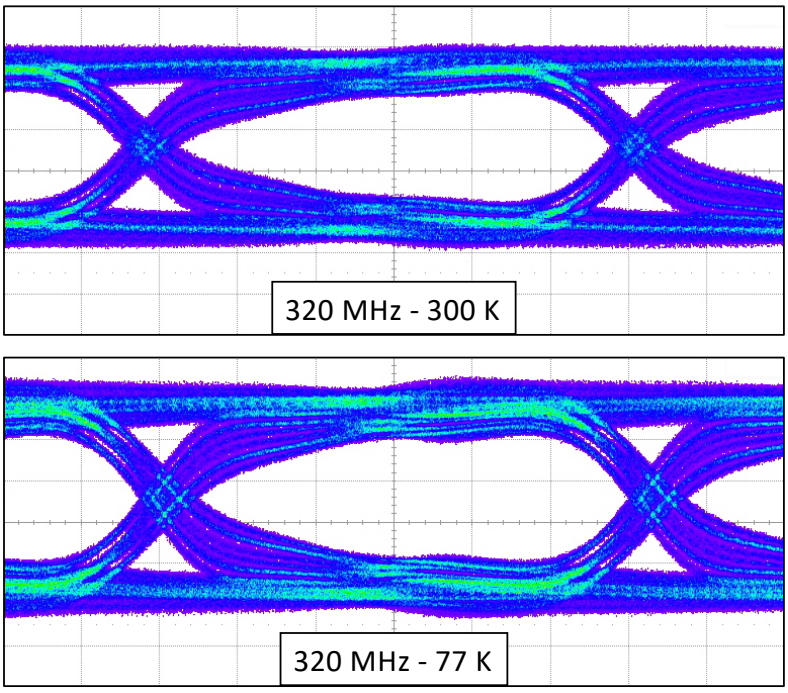
Table 4.2: Eye diagram measurements of LVDS driver, with data transmission at low frequency.

	320 MHz (@300 K)	320 MHz (@77 K)
Level 1 (mV)	394	465
Level 0 (mV)	-405	-467
Rise Time (ps)	522	752
Fall Time (ps)	597	838
Eye Amp (mV)	799	932
Eye Height (mV)	196	212
Eye Width (ns)	2,63	2,52
Eye S/N	3,97	3,88

Table 4.3: Eye diagram measurements of LVDS driver, with data transmission at high frequency.



(a) X: 5 ns/div, Y: 200 mV/div



(b) X: 500 ps/div, Y: 200 mV/div

Figure 4.16: Eye diagram of LVDS transmitter driver at two different frequency: (a) 40 MHz and (b) 320 MHz.

4.3 Conclusions

The Test Chip (TC) allowed to perform a preliminary test at cryogenic temperature giving an important insight into critical digital circuit blocks and LVDS transceivers. Results obtained with the synchronisation circuit are very promising, in particular because they demonstrate that the extrapolated SPICE model at 77K is valid. This is despite the fact that the technology vendor does not provide the digital standard models and library characterisation for 77 K temperature corners. These test results have been used to complete the design of ALCOR ASIC.

The experimental results of the LVDS transmitter shows a good response at high and low data frequency data transmission and demonstrate its adequate operation at 77 K for the intended application of ALCOR.

Chapter 5

Design of smart integrated networks for large area photo-sensors readout.

Future physics experiments looking for very rare events, such as weakly interacting massive particles or neutrino-less double-beta decay, will call for a light detection module with a very low radioactive background [76, 3, 59, 79, 53]. In particular, those experiments will employ SiPM, which has proven to be a very mature technology with interesting characteristics in terms of compactness, low biasing voltage and dark-count rate and relatively high PDE for the UV spectra. These systems employ a large area of sensors in the order of several m^2, thus on detector digitisation and optimised data transmission techniques, allowing for the minimisation of the photodetector volume and signal cabling and interfaces will be at a premium. This chapter presents the architecture and system-level considerations of a CMOS distributed-sensor network designed for the readout of large areas solid-state photodetectors in future dark matter and neutrino experiments using noble gas detectors. This preliminary work focuses on a solution based on a matrix of 24 SiPM sensors 3D assembled on top of a CMOS monolithic active substrate, which embeds an equivalent number of readout nodes and provides the signal and power interconnect. Each node digitises the signal produced by the SiPM and transmits the data to the neighbouring pixel. A method for data transmission and acknowledgement that maximises the yield in case of signal node failure has been adopted. The VHDL of the pixel data control was synthesised, and the simulation results of the RTL netlist are presented.

5.1 Motivation

This work addresses the data transmission and control of a CMOS active substrate for large area sensor integration on future liquid noble detectors looking for very rare events. The simplified scheme of a radiation detector sensor network is illustrated in Figure 5.1. In this implementation, the signal produced by the photosensor is first amplified with a Front-End (FE) circuit and then it can be digitised with an analogue charge or time converter depending on the application requirements, as discussed in Chapter 2. The generated payload is then stored on a local register bank, and the sensor control adds data to any payload received from previous sensors. This is a simplified system that allows to perform digitisation on-chip of sensor signals. This embodiment assumes that sets of sensors are organised in a daisy-chain network, and data is propagated using a shared bus buffered at every sensor. This study is based on the PDM module of 24 SiPM sensors developed by the DarkSide-20k (DS-20k) Collaboration. The solution proposed by this thesis assumes that the sensors are a flip-chip mounted on top of a CMOS active substrate that embeds 24 readout sensors with the aforementioned architecture. In this way, each pixel reads an area of 1 cm^2. This principle is illustrated in Figure 5.2, data, clock and/or control, power and SiPM bias could be assembled to the substrate using advanced bonding techniques, and they are shared among all the pixel on the same substrate. The technological aspects of the CMOS fabrication and sensor integration are not within the scope of this work, which otherwise focuses on the architecture of the control logic and data multiplexing and transmission schemes. Such a Distributed-Sensor Network (DSN) is thereby a pixel-based fully connected bidirectionally topology suitable to readout large area of SiPMs, where signal integrity, data rate and cable management become a relevant issue. Each pixel performs signal processing and produces digital data to be dispatched outside the network. The data transmission and format, and preliminary simulations are performed in order to test the reliability of the network due to node failure. Iterating on the percentage of failure, which will be a function of the total active area, the typical yield and maturity of the target CMOS technology node and the use of correct design-for-manufacturability rules and guidelines. A key point in a network topology is to ensure proper operation even in the case of node malfunctioning, which may create problems with data transmission or compromise the entire network. The envisaged operation of DSN topology should preserve the

data transmission to the outside world even in the presence of single-node failure and change the output path consequently.

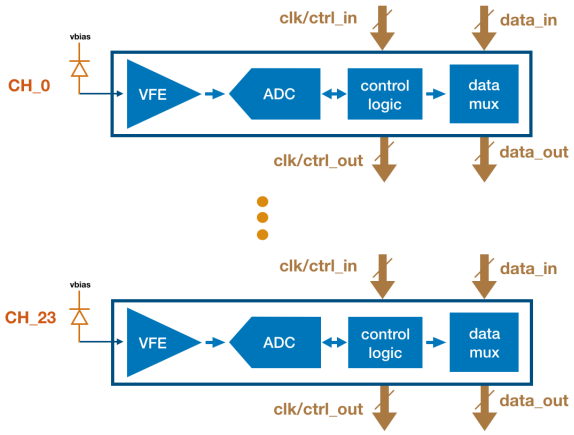


Figure 5.1: Simplified block diagram of the CMOS sensor circuitry and data links.

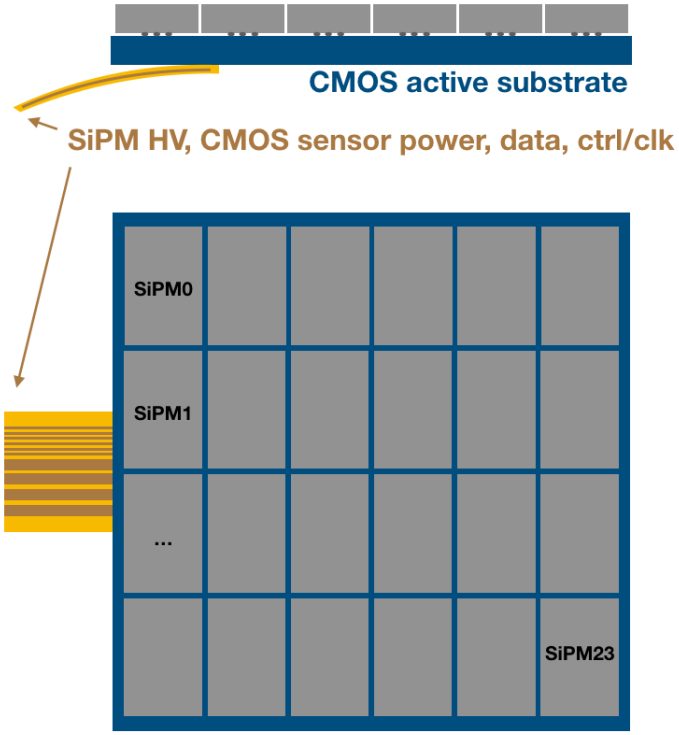


Figure 5.2: Illustration of a possible embodiment of the CMOS distributed-sensor active substrate for SiPM readout and assembly.

5.2 DSN topology

In order to understand correctly the network architecture presented, an overview description of the main structure is essential. The different layers are presented and described below:

- The sensor: is the whole sensor area of the detector which is in the order of m^2 and it is divided in N sub-sensors;
- The sub-sensor: is a small portion of the sensor and it is divided in M small pixels, in this area the DSN take place;
- The pixel: is $\frac{1}{M \cdot N}$ portion of the sensor and it is connected to the readout sensor embedded on the CMOS active substrate;
- The CMOS active substrate: is placed beneath the sensor, it reads signals coming from pixels region and cover a sub-sensor area;

The pixels placed on the same sub-sensor area are connected in the matrix topology as it is shown in Figure 5.3. In this paper, 24-pixel division is considered for a sub-sensor area of 24 cm^2. $Pix0$ and $Pix23$ are the input and output of the network. These two nodes are also a critical point of the network: if one of the two fails, all the network is compromised. Each pixel has a 4 point to point bidirectional connection between neighbouring pixels. In this way, for each node there are four possible paths for data transmission. In the same column, the first pixel is connected to the last pixel (i.e. $Pix0$ is connected to $Pix18$). This type of connection is the most reliable topology, and it has been chosen after the simulation described in Section 5.3. Data generated from each pixel has to reach $Pix23$ in order to be retrieved outside the network. This fully connected topology allows to have multiple output paths in order to reach the output of the network, even in case of single or multiple node failure. If used stand-alone, there is a point-to-point connection from the active substrate to warm electronics outside the detector, and thus the $Pix0$ is the first data transmitting node. The number of pixels in DSN depends on the granularity of the sensor and the total area of the sub-sensor. While several DSN can be plugged to each other through input and output ports in a daisy chain network, creating a big structure. Thanks to this feature, the DSN topology is a flexible, modular and scalable solution to readout large area of sensors.

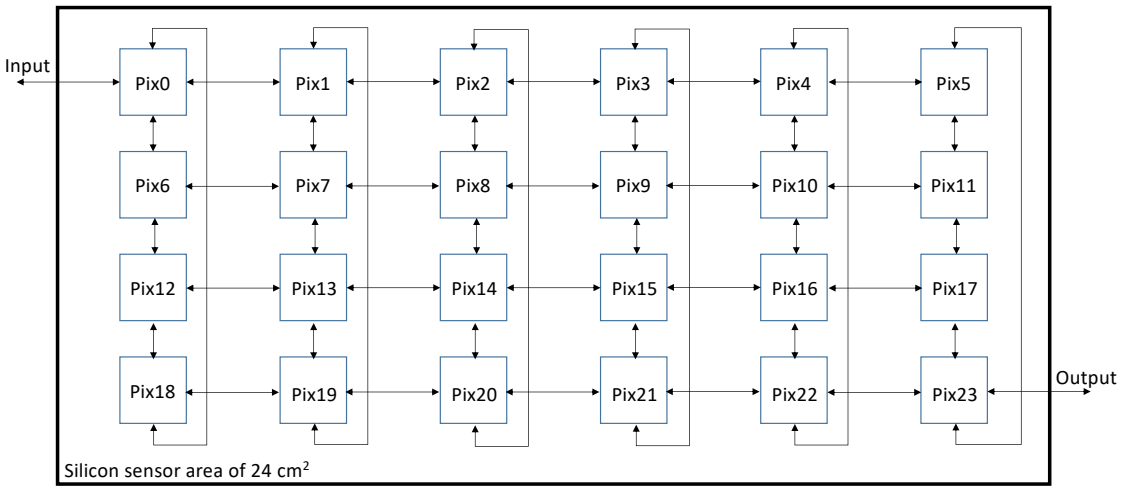


Figure 5.3: Block diagram of distributed-sensor network over a sub-sensor area of 24 cm^2.

5.2.1 Data transmission between pixel nodes

This work addresses the resilience of the network to maintain and recover the data transmission links in case of pixel failure. The Figure 5.4 illustrates the main blocks that are involved in the data transmission. Starting from the *Data Control*, this block is in charge of transmitting/receive data from/to pixels. The advantage to have only a point to point connection allows the pixel to manage independently communications in four directions. In order to do so, a FIFO queue must be implemented in order to store temporarily the incoming data from neighbouring pixels or to store data generated from the pixel itself. The FIFO depth must be set depending on the application and on the data rate. The *Direction Controller* performs an important role on the data transmission because this is the block that decides where in which direction the data will be dispatched according to a well-defined algorithm. The *Direction Controller* block, in order to keep the status of neighbouring pixels, uses a table to store information about reachability. At the reset state, the default value for each direction is set to *reachable*. The record is updated to *unreachable* as soon as the pixel in that direction stops to communicate. The record of reachability table is updated to *unreachable* in two main cases:

- When a pixel starts a data communication and doesn't receive any response from the neighbour pixel after a certain amount of time;

- When a pixel receives data from the right or bottom pixels, which means data is coming back, and therefore those directions are dead paths;

According to the reachability table, the algorithm shown in Figure 5.5 is followed to transmit data. The data generated from one pixel has to reach the output of the DSN network. In order to do so, the natural data flow path inside the topology is the right/bottom direction. In case these directions are marked as *unreachable* in the reachability table, the pixel tries the other two directions. The table is checked periodically using the system clock. A pixel stops to generate data in case all the records in the table are marked as *unreachable*. Conflict cases of two pixels trying to transmit data at the same time is avoided; if the right pixel transmits data, it means all the other paths of this pixel are dead paths. Some case if the bottom pixel wants to transmit to the upper pixel. However if these particular cases take place, the transmission priority is given to the right/bottom node and the *reachability* table is accordingly updated.

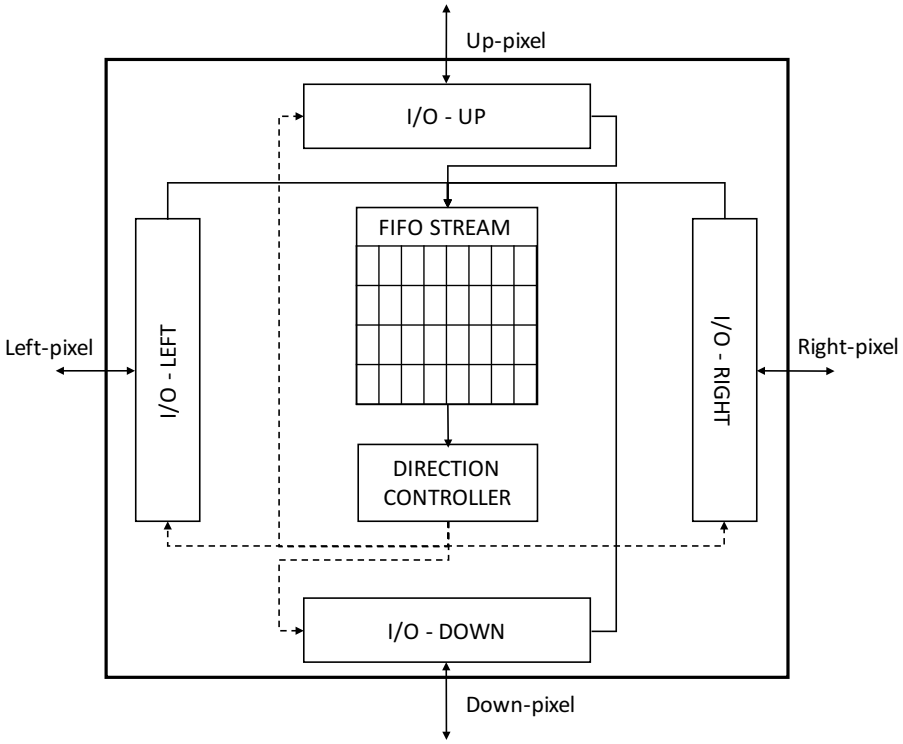


Figure 5.4: Pixel Data Control block diagram.

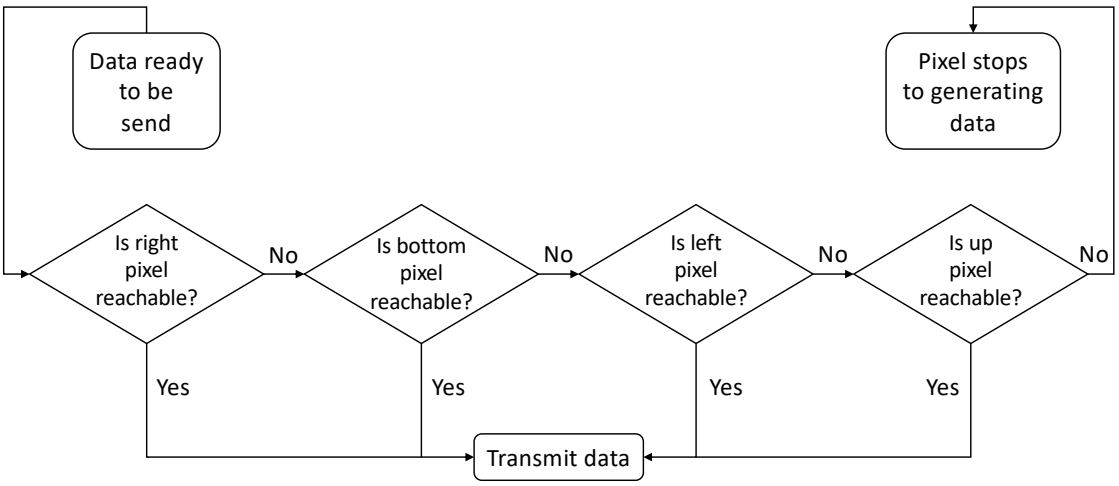


Figure 5.5: Data transmission algorithm, the pixel follows these steps in order to send the data: starting from the right-direction and ends to up-direction. If all the connection are unreachable, the pixel stops to generate data.

Since this topology is meant to be employed in large area sensors, the physical distance between pixels can be in the order of *cm*, the clock can propagate to all pixel with some delay. Therefore, the data transmission is treated as asynchronous communication. The I/O block uses a custom handshake protocol to establish and initiate a connection with the neighbouring pixels. This protocol is described in a state diagram in Figure 5.6. The FSM of the I/O controller manages either the data transmitting or the data receiving. The FSM waits in *IDLE* state till receives a *data_ready* or a *request_in* signal. The right branch is taken when there is data ready to be sent, while the left branch is used to read incoming data. In the first case, the pixel sends a writing request to the neighbour pixel and waits in the *WAIT_READY* state for a *ready_in* response. When both pixels are logically connected, the data transmission can start and lasts for a clock period proportional to the data length. In the second case, the pixel that receives a request signal from a neighbouring pixel sends a *ready_out* signal and waits for the incoming data. The pattern data length is set during configuration or can be preconfigured in the pixel.

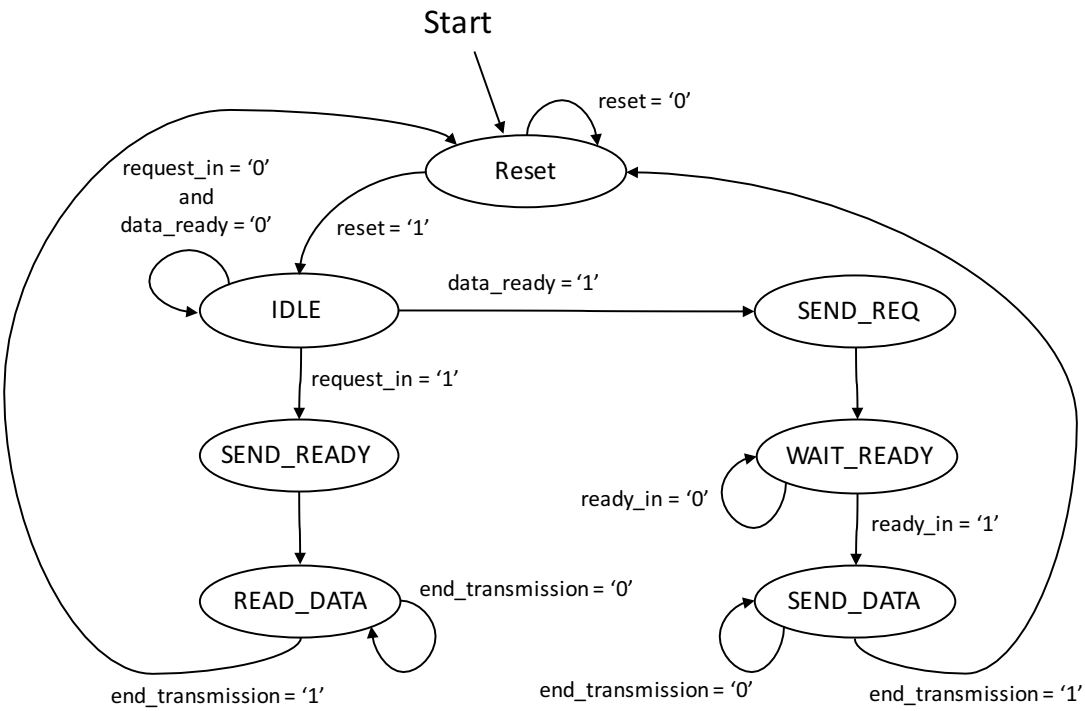


Figure 5.6: Block diagram of data transmission FSM.

The physical connection between pixels must be the minimum necessary. Beside the hand-shaking signal, the clock and data signal must be included in the connections. These two information can be easily combined using a Manchester encoding technique, where the data controls the phase of a square wave carrier whose frequency is the data rate; the clock rate is proportional to the line voltage transitions [78]. Figure 5.7 depicts an example of data transmission using this technique. Depending on the transmitting data, two consecutive bits of the same type force a transition at the beginning of a bit period: the logic-0 state forces a positive transition in the middle of the bit, while the logic-1 state forces a negative transition in the middle of the bit.

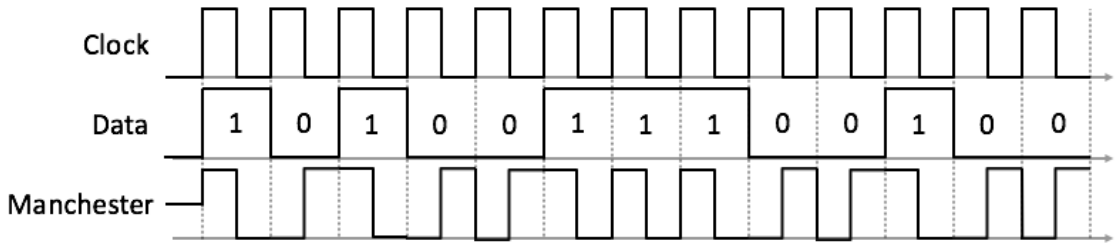


Figure 5.7: Example of Manchester encoded data transmission.

The simulation of data transmission between two pixels is showed in Figure 5.8. Using a digital simulator, this is done at RTL level in VHDL language to demonstrate the operation of handshake protocol and Manchester encoded data transmission. In this example *A-pixel* is the sender and *B-pixel* is the receiver.

A-pixel starts to establish a communication at the simulation time 167.5 *ns* and *B-pixel* acknowledges the communication at the simulation time 175 *ns*. After these initial handshake signals, the data transmission can be started. The data to be transmitted is "$0xAAAAAAAA$", a sequence of logic-0 and logic-1. This is a typical data sequence chosen to stress the data transmission since it has very close sequences of zeros and ones. The data encoded with Manchester technique is sent serially from *A-pixel* through the output port *data_out*, and is connected to the *data_in* port of *B-pixel*. It is possible to see the *pixel_memory_in* signal that changes its value as soon as a new bit of information is added. In this case, the transmission lasts for 3 clock cycles for hand shake protocol and 32 clock cycles for data transmission. The advantage of performing serial data communication is the possibility of increase or decrease the data length without changing the physical connection. In order to ensure the integrity of transmitted data, a parity bit can be easily added at the end of the transmission. This bit is an extra information that tells the receiver how many ones are contained in the data. When this number is even, the parity bit is set to logic-0. Otherwise, if this number is odd, the parity bit is set to logic-1.

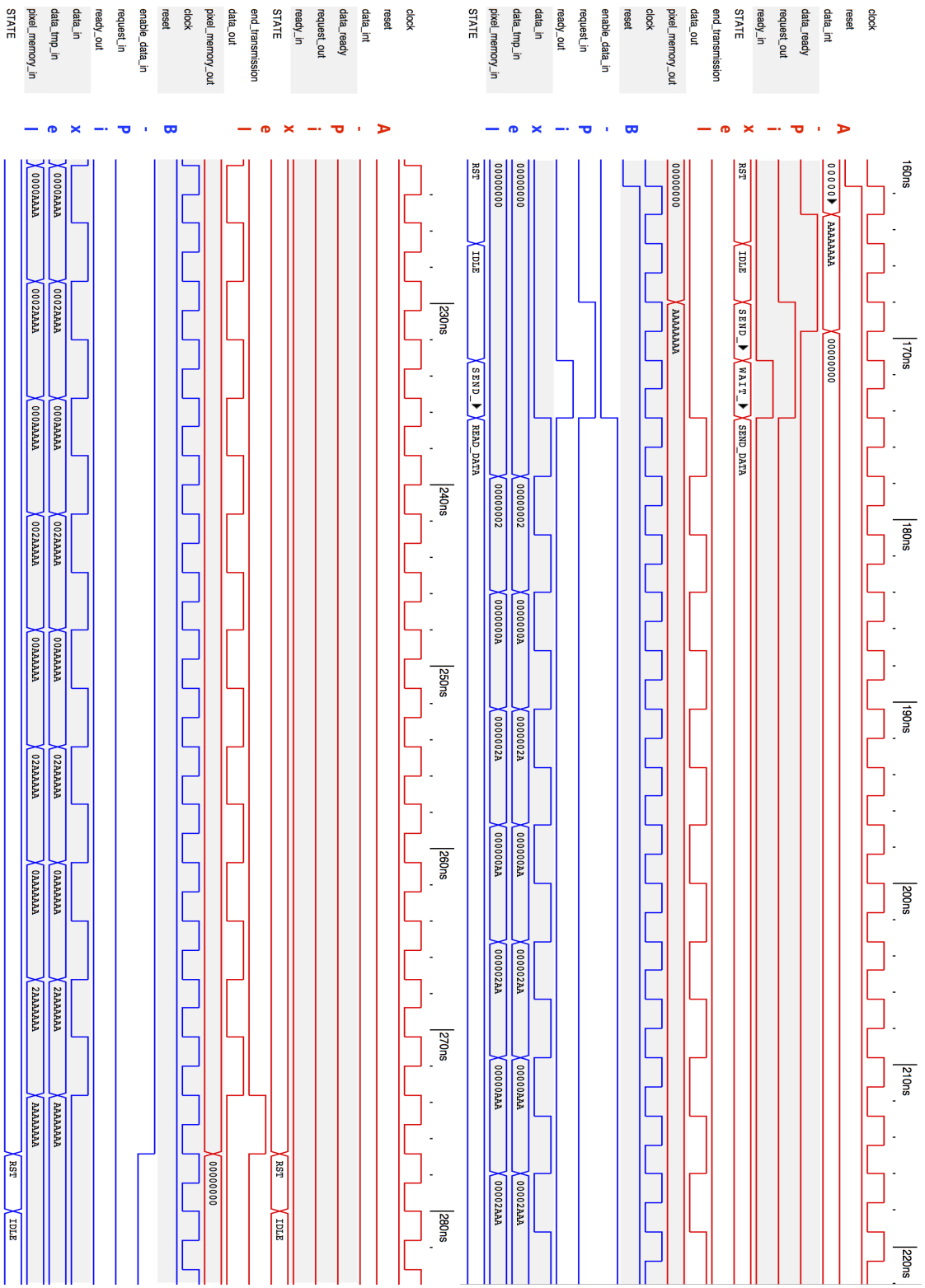


Figure 5.8: Time diagram of VHDL simulation, handshaking and data transmission between two pixels.

5.3 Reliability of the DSN to pixel failure

The DSN is a network designed to be free from node failure. In case of pixel failure, the network must ensure a data path to transmit payloads externally to the network. Therefore, different connection topologies between nodes have been considered and chosen the most reliable. A pixel is considered failed when the data transmission circuit of the node stops to behave properly. This may happen as a result of normal wear or due to shorter-than-expected lifetime of the electronic components at cryogenic temperature. The network of 24-pixel has been simulated to prove the robustness of the distributed sensor in case of failed pixels. The pseudo-code executed in the Python language is shown in Figure 5.9.

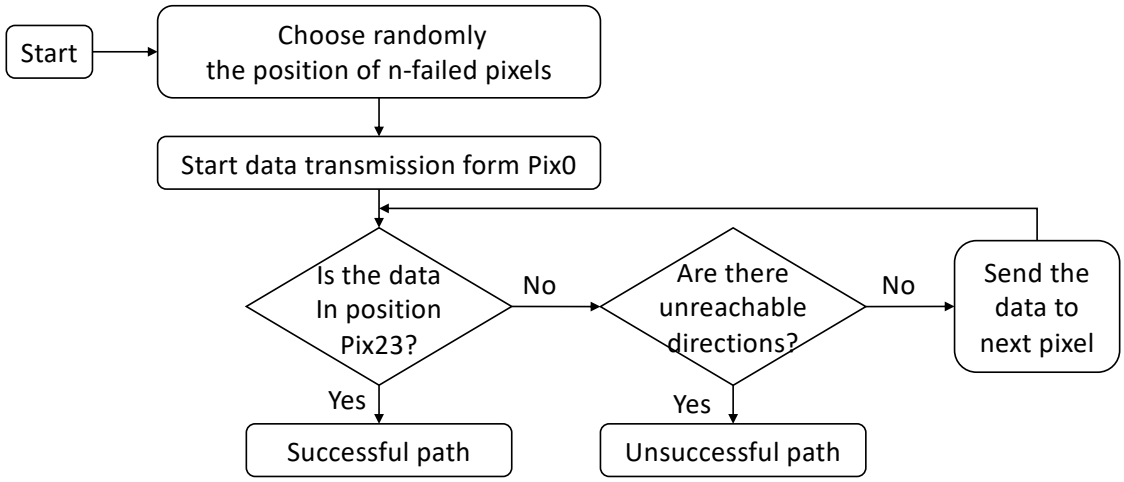


Figure 5.9: Pseudo code of DSN network

The purpose of the simulation is to understand how many pixels have to fail in order to compromise the data transmission in the DSN network. In each simulation the algorithm chooses randomly n-failed pixels in the network, and the data payload generated from $Pix0$ must reach the output of the network in $Pix23$. Using the data transmission algorithm discussed in Section 5.2.1 the data payload tracks a successful data path in case it reaches the output or an unsuccessful data path in case the data remains stuck in the network. An example of a successful data path is depicted in Figure 5.10, where there are 4-failed pixels in red, while the green pixels track the path that the data took to reach the last node. A simulation performed from 1 to 22 pixels failed, excluding $Pix0$

and $Pix23$ inasmuch as they are the starting and ending nodes of the network.

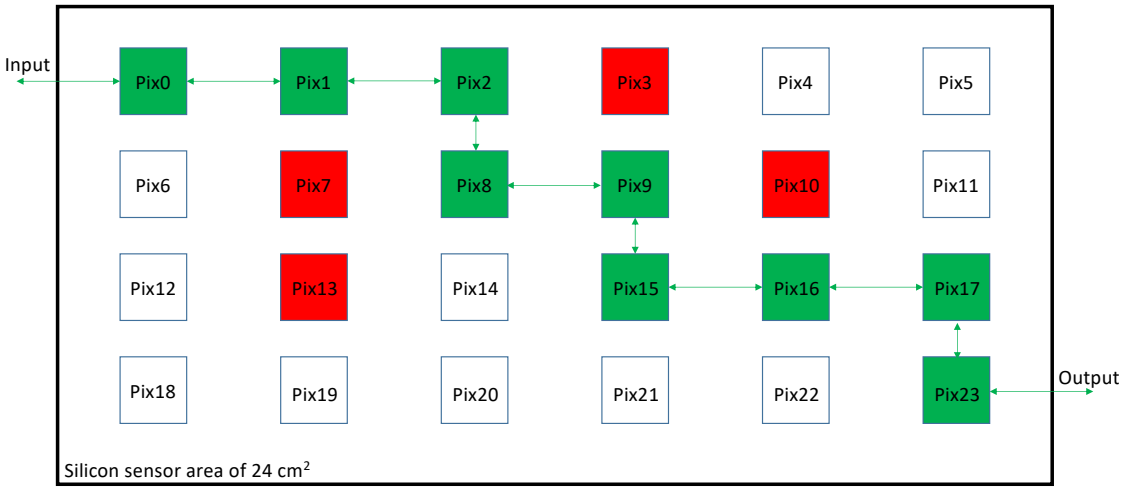


Figure 5.10: Simulation example of a successful data path from Pix0 to Pix23. In red failed pixels (Pix3, Pix7, Pix10, pix13), while in green the path that the data payload took to reach the Pix23 from Pix0.

The pixels matrix layout allows to have different connections between nodes. Increasing the number of links, the probability to find a correct data path increases consequently. Therefore, the simulation is performed considering four different connection topologies depicted in Figure 5.11 and they are defined below:

- **Normal** topology, the network has only inner connections between neighbouring nodes, they are marked in black.
- **Up-Bottom** topology, beside the inner connections, the network has external connection between nodes in the first row and nodes in the last row of same column (e.g. Pix0 connected to Pix18). These links are marked in red.
- **Right-Left** topology, beside the inner connections, the network has connections between rows, nodes in the last column are connected to nodes in the first column (e.g. Pix5 connected to Pix6). These links are marked in blue.
- **Full** topology includes all the other three topologies creating a fully connected network.

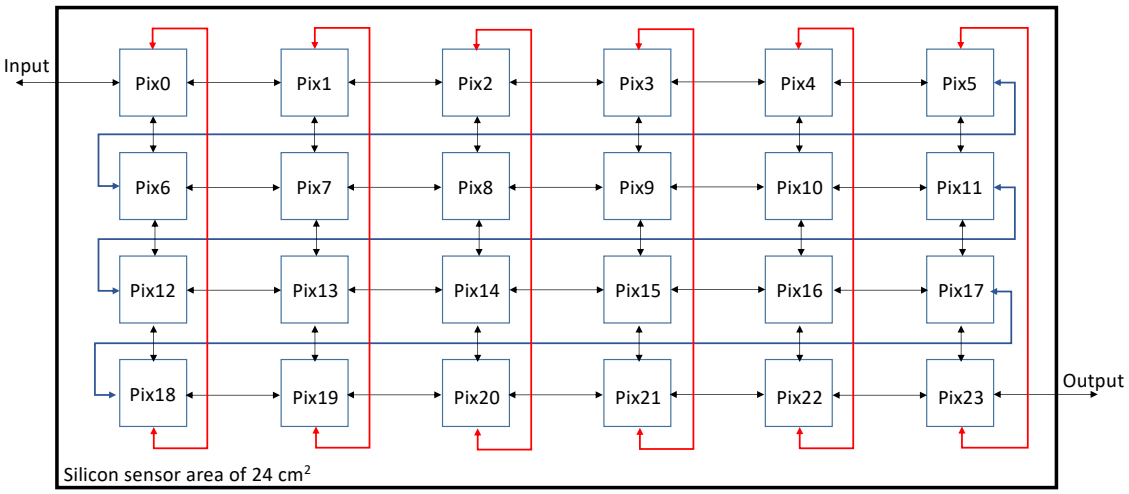


Figure 5.11: DSN network with inner connections (black), up-bottom connections (red) and left-right connections (blue).

The number of output paths is proportional to the number of inner connections. A path counting algorithm has been run to asses the possible paths from $Pix0$ to $Pix23$ and results are reported in Table 5.1. Obviously, the *Full* connected network has a higher number of paths, 478821 compared to the *Normal* connected network which has only 5382 paths.

	Normal	**Up-Bottom**	**Right-Left**	**Full**
Paths	5382	132·070	37·016	478·821

Table 5.1: Number of possible paths from $Pix0$ to $Pix23$ for each network.

The four networks are simulated in order to understand which of those connections between pixels are essential. Results are reported in Figure 5.12 where the trend of curves depicts how networks respond in case of a random failed pixel. The percentage of *Correct paths* goes below 50% between 7 to 9 failed pixels, but *Up-Bottom* connection is turned out as the most robust network, despite it has lower possible paths compared to *Full* network. The *Right-Left* connections do not introduce an advantage with the data transmission algorithm proposed in Section 5.2.1. The trend is very similar among all the networks, therefore a secondary judgement parameter has been introduced: the number of steps needed to reach the output node.

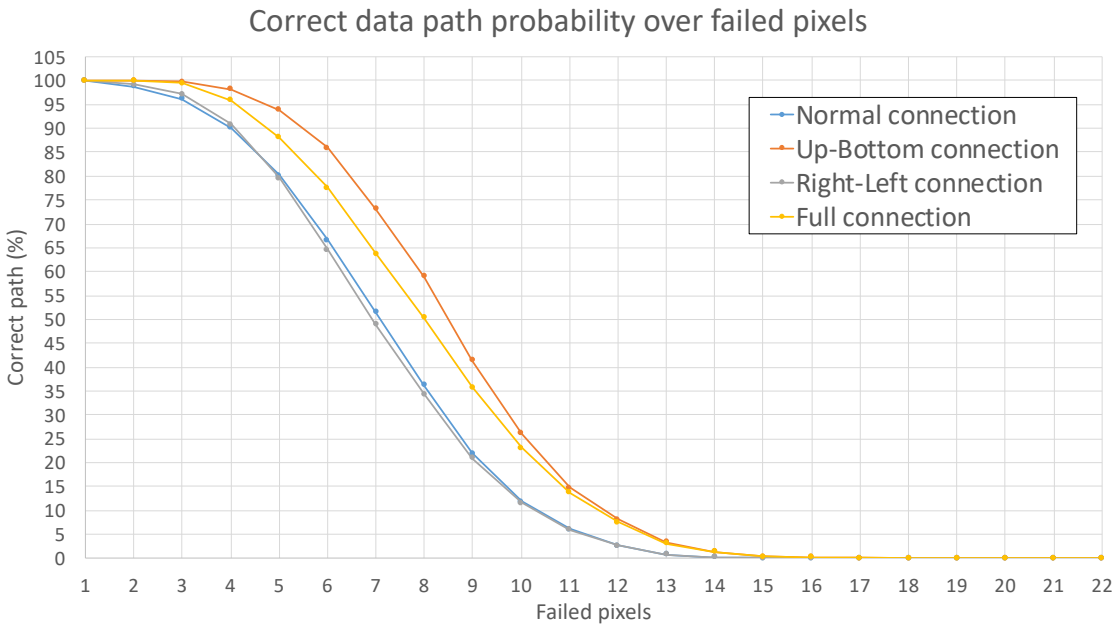


Figure 5.12: Result of the simulation: x-axis shows the number of pixel failed over 24 pixels, y-axis shows the percentage of successful path.

Comparing the *Up-Bottom* and *Full* topologies which had a very similar curve in the previous analysis, the first topology takes a much smaller number of steps to reach the output port. The Figure 5.13 depicts the curves of the four networks, where the *Up-Bottom* required a mean of ~ 9 steps compared to *Full* network that requires at the beginning a mean of ~ 28 steps and then decreases to a mean of ~ 7 steps as soon as pixels start to fail. The zero steps mean that no correct paths have been produced in the simulation with that number of failed pixel.

The constant steps and better reliability to pixel failure make the *Up-Bottom* topology the most robust network. Compared to *Full* topology, the reduction of *Right-Left* links is an advantage for the design of the CMOS active substrate.

The same simulation has been performed with 100 pixels in a matrix of 10×10, in order to test the behaviour of DSN network with bigger matrices. The obtained results are fully comparable with the previous simulation. Also in this case the *Up-Bottom* comes out as the best topology to be implemented in a DSN network. The Figure 5.14 depicts the results obtained with the *Full* and *Up-Bottom* topology, showing both percentages of successful paths and number of steps as function of failed pixels.

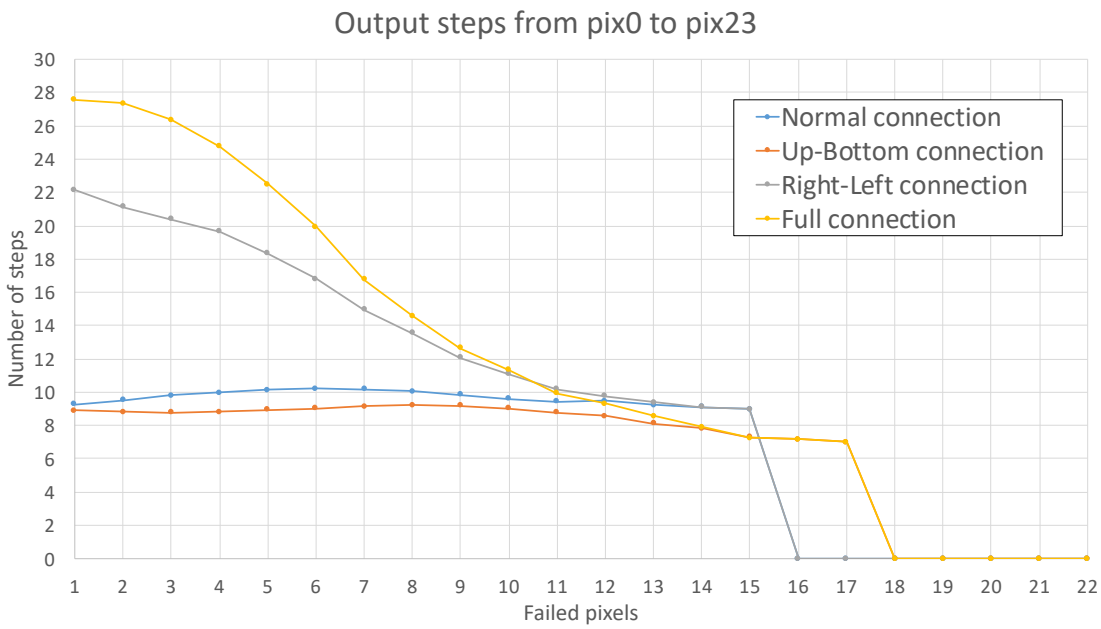


Figure 5.13: Result of the simulation: x-axis shows the number of pixel failed over 24 pixels, y-axis shows the number of steps that the date takes to reach $Pix23$ from $Pix0$.

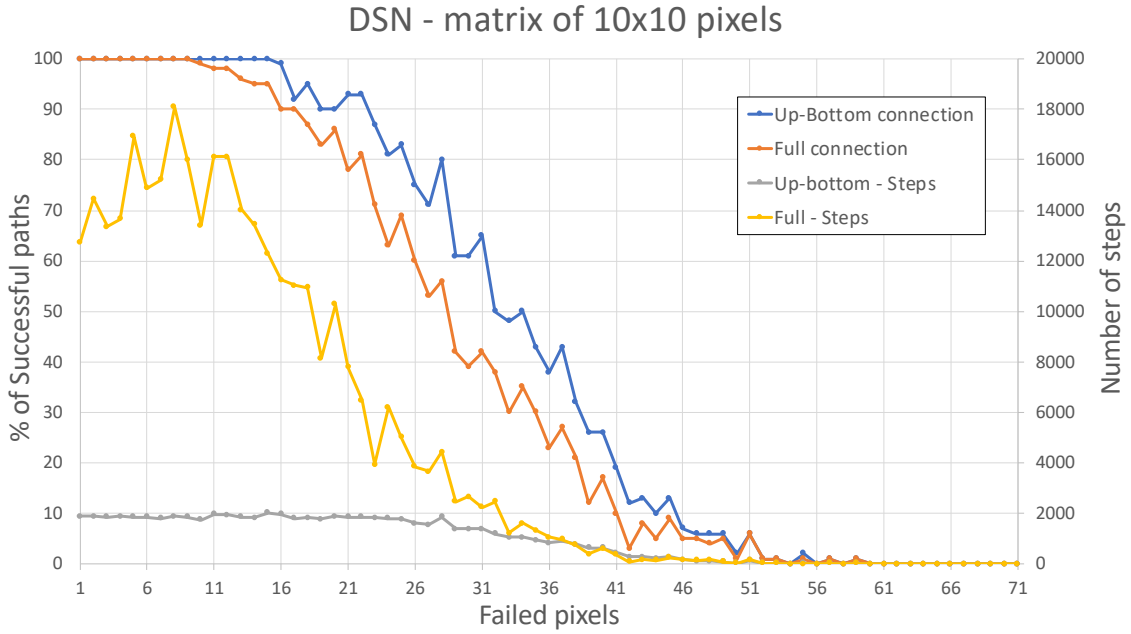


Figure 5.14: Simulation results of a DSN network with 100 pixels. x-axis reports the number of pixel failed, right y-axis reports the number of steps that the date takes to reach $Pix23$ from $Pix0$, right y-axis reports the percentage of successful paths.

5.4 Conclusions

This work describes a Distributed-Sensor Network (DSN) implemented in a pixel-based topology, suitable for the readout of a large area of SiPM sensors in future detectors looking for very rare events. Preliminary studies and simulations have been done on a 24-pixel network using as a case study a 24 cm^2 silicon sensor area. This chapter discussed the data transmission techniques and the robustness of the network to single and multiple node failure. In the DSN, pixels are connected in a matrix structure, which allows to have different output paths in case of single or multiple pixel failure. Simulation results demonstrate that a *Up-Bottom* topology network is less prone to failure due to a single pixel loss. This work is a starting point towards an all-silicon ultra-low radioactive background photoelectronics module for future dark matter and neutrino detectors with unprecedented sensitivity.

Appendix A

Alcor

A.1 Configuration registers

Bias Configuration Register

Position	Signal name	Description
<0:1>	iblatchDAC	Bias for DACs
<2:6>	iTDC	Bias for TDCs
<7:9>	cal	Enables TP as FE input

Table A.1: BCR_0, defines global analogue bias settings.

Position	Signal name	Description
<0:4>	Bit_cg	Common gate current of VFE
<9:5>	Bit_boost	gm boost current of VFE
<10>	S0	VFE input polarisation
<11>	ib_sF	bias of discriminator
<12:13>	ib_3	bias of discriminator
14:15>	ib_2	bias of discriminator

Table A.2: BCR_1, defines global analogue bias settings.

Pixel Configuration Registers - 0

Position	Signal name
<15:12>	cDAC_TDC3
<8:11>	cDAC_TDC2
<7:4>	cDAC_TDC1
<3:0>	cDAC_TDC0

Table A.3: Configuration registers to set coarse TDC's fast current.

Pixel Configuration Registers - 1

Position	Signal name
<15:11>	fDAC_TDC3
<8:11>	fDAC_TDC2
<7:4>	fDAC_TDC1
<3:0>	fDAC_TDC0

Table A.4: Configuration register to set fine TDC's fast current.

Pixel Configuration Registers - 2

Position	Signal Name	Value
<15:10>	LE2DAC	max: 111111 min: 000000 LSB: LEDACrange/64
<9:8>	LEDACVth	Vth_{min} max: 750 mV (11) min: 550 mV (00)
<7:6>	LEDACrange	Vth_{delta} max: 128 mV (11) min: 50 mV (00)
<5:0>	LE1DAC	max: 111111 min: 000000 LSB: LEDACrange/64

Table A.5: Configuration register to set discriminator threshold voltages and ranges.

Pixel Configuration Registers - 3

Position	Signal name	Description
<15:13>	Offset1	offset current of amplifier 2
<12:9>	OpMode	pixel's operational mode
<8:6>	Offset2	offset current of amplifier 2
<5:4>	Gain1	defines gain for amplifier 1
<3:2>	Gain2	defines gain for amplifier 2
<1>	Polarisation	'0' : negative input signal '1' : positive input signal
<0>	Void	Not Used

Table A.6: Configuration register to set amplifiers configuration and pixel operation mode.

End of Column Configuration Register

Position	Description
<15>	Enable Status Word in data (double column)
<14>	Serialiser Align Mode (double column)
<13>	Serialiser Enable (double column)
<12>	8b/10b Encoder Enable (double column)
<11>	Raw Mode Data (double column)
<6:10>	Not used
<5>	Column 1 cfg_I_ratio
<4>	Column 1 cfg_Safety_bit
<3>	Column 1 Enable
<2>	Column 0 cfg_I_ratio
<1>	Column 0 cgf_Safety_bit
<0>	Column 0 Enable

Table A.7: End of Column Configuration Register

Registers default values

Register	Value <15:0>
PCR0	0111 | 0111 | 0111 | 0111
PCR1	1000 | 1000 | 1000 | 1000
PCR2	111111 | 11 | 11 | 111111
PCR3	000 | 0001 | 000 | 11 | 11 | 0 | 0
ECCR	00000 | 00000 | 000000

A.2 FSM with Hamming code implementation

Code Listing A.1: VHDL code with Hamming code implementation

```
signal STATE, NEXT_STATE : STATE_TYPE;
subtype STATE_TYPE is std_logic_vector(5 downto 0);

-- FSM Valid states without Hamming code implementation
constant IDLE:                  STATE_TYPE := "000000"; -- "000"
constant WRITE_STAT:            STATE_TYPE := "010101"; -- "001"
constant RESET_FF_DVAL:         STATE_TYPE := "100110"; -- "010"
constant WRITE_REQ:             STATE_TYPE := "110011"; -- "011"
constant WRITE_OUT:             STATE_TYPE := "111000"; -- "100"
constant READ_FIFO:             STATE_TYPE := "101101"; -- "101"

-- FSM Wrong states
constant w_IDLE_1:              STATE_TYPE := "000001";
constant w_IDLE_2:              STATE_TYPE := "000010";
constant w_IDLE_3:              STATE_TYPE := "000100";
constant w_IDLE_4:              STATE_TYPE := "001000";
constant w_IDLE_5:              STATE_TYPE := "010000";
constant w_IDLE_6:              STATE_TYPE := "100000";

constant w_WRITE_STAT_1:        STATE_TYPE := "010100";
constant w_WRITE_STAT_2:        STATE_TYPE := "010111";
constant w_WRITE_STAT_3:        STATE_TYPE := "010001";
constant w_WRITE_STAT_4:        STATE_TYPE := "011101";
constant w_WRITE_STAT_5:        STATE_TYPE := "000101";
constant w_WRITE_STAT_6:        STATE_TYPE := "110101";

constant w_RESET_FF_DVAL_1:     STATE_TYPE := "100111";
constant w_RESET_FF_DVAL_2:     STATE_TYPE := "100100";
constant w_RESET_FF_DVAL_3:     STATE_TYPE := "100010";
constant w_RESET_FF_DVAL_4:     STATE_TYPE := "101110";
constant w_RESET_FF_DVAL_5:     STATE_TYPE := "110110";
constant w_RESET_FF_DVAL_6:     STATE_TYPE := "000110";

constant w_WRITE_REQ_1:         STATE_TYPE := "110010";
constant w_WRITE_REQ_2:         STATE_TYPE := "110001";
constant w_WRITE_REQ_3:         STATE_TYPE := "110111";
constant w_WRITE_REQ_4:         STATE_TYPE := "111011";
constant w_WRITE_REQ_5:         STATE_TYPE := "100011";
constant w_WRITE_REQ_6:         STATE_TYPE := "010011";

constant w_WRITE_OUT_1:         STATE_TYPE := "111001";
constant w_WRITE_OUT_2:         STATE_TYPE := "111010";
constant w_WRITE_OUT_3:         STATE_TYPE := "111100";
constant w_WRITE_OUT_4:         STATE_TYPE := "110000";
constant w_WRITE_OUT_5:         STATE_TYPE := "101000";
constant w_WRITE_OUT_6:         STATE_TYPE := "011000";

constant w_READ_FIFO_1:         STATE_TYPE := "101100";
constant w_READ_FIFO_2:         STATE_TYPE := "101111";
constant w_READ_FIFO_3:         STATE_TYPE := "101001";
constant w_READ_FIFO_4:         STATE_TYPE := "100101";
constant w_READ_FIFO_5:         STATE_TYPE := "111101";
constant w_READ_FIFO_6:         STATE_TYPE := "001101";

state_encode : process (STATE, empty, read_pixel, end_count, read_status,
    end_count2, count(0))
begin
        case STATE is
                when IDLE =>
                        if read_status = '1' then
```

```
                        NEXT_STATE <= WRITE_STAT;
                else
                        if empty = '0' then
                                NEXT_STATE <= WRITE_REQ;
                        else
                                NEXT_STATE <= IDLE;

                        end if;
                end if;
                rad_error_count <= '0';
        when w_IDLE_1 | w_IDLE_2 | w_IDLE_3 | w_IDLE_4 | w_IDLE_5
            | w_IDLE_6 =>
                if read_status = '1' then
                        NEXT_STATE <= WRITE_STAT;
                else
                        if empty = '0' then
                                NEXT_STATE <= WRITE_REQ;
                        else
                                NEXT_STATE <= IDLE;

                        end if;
                end if;
                rad_error_count <= '1';
        when WRITE_REQ =>
                if read_status = '1' then
                        NEXT_STATE <= WRITE_STAT;
                else
                        if read_pixel = '1' then
                                NEXT_STATE <= READ_FIFO_1;
                        else
                                NEXT_STATE <= WRITE_REQ;
                        end if;
                end if;
                rad_error_count <- '0';
        when w_WRITE_REQ_1 | w_WRITE_REQ_2 | w_WRITE_REQ_3 |
            w_WRITE_REQ_4 | w_WRITE_REQ_5 | w_WRITE_REQ_6 =>
                if read_status = '1' then
                        NEXT_STATE <= WRITE_STAT;
                else
                        if read_pixel = '1' then
                                NEXT_STATE <= READ_FIFO_1;
                        else
                                NEXT_STATE <= WRITE_REQ;
                        end if;
                end if;
                rad_error_count <= '1';
        when READ_FIFO =>
                NEXT_STATE <= WRITE_OUT1;
                rad_error_count <= '0';
        when w_READ_FIFO_1 | w_READ_FIFO_2 | w_READ_FIFO_3 |
            w_READ_FIFO_4 | w_READ_FIFO_5 | w_READ_FIFO_6 =>
                NEXT_STATE <= WRITE_OUT1;
                rad_error_count <= '1';
        when WRITE_STAT =>
                if end_count = '1' then
                        NEXT_STATE <= RESET_FF_DVAL;
                else
                        NEXT_STATE <= WRITE_STAT;
                end if;
                rad_error_count <= '0';
        when w_WRITE_STAT_1 | w_WRITE_STAT_2 | w_WRITE_STAT_3 |
            w_WRITE_STAT_4 | w_WRITE_STAT_5 | w_WRITE_STAT_6 =>
                if end_count = '1' then
                        NEXT_STATE <= RESET_FF_DVAL;
                else
                        NEXT_STATE <= WRITE_STAT;
                end if;
                rad_error_count <= '1';
```

```
                when WRITE_OUT =>
                        if end_count = '1' then
                                NEXT_STATE <= RESET_FF_DVAL;
                        else
                                NEXT_STATE <= WRITE_OUT1;
                        end if;
                        rad_error_count <= '0';
                when w_WRITE_OUT_1 |  w_WRITE_OUT_2 |  w_WRITE_OUT_3 |
                    w_WRITE_OUT_4 |  w_WRITE_OUT_5 |  w_WRITE_OUT_6 =>

                        if end_count = '1' then
                                NEXT_STATE <= RESET_FF_DVAL;
                        else
                                NEXT_STATE <= WRITE_OUT1;
                        end if;
                        rad_error_count <= '1';
                when RESET_FF_DVAL =>
                        NEXT_STATE <= IDLE;
                        rad_error_count <= '0';
                when w_RESET_FF_DVAL_1 | w_RESET_FF_DVAL_2 |
                    w_RESET_FF_DVAL_3 | w_RESET_FF_DVAL_4 |
                    w_RESET_FF_DVAL_5 | w_RESET_FF_DVAL_6 =>
                        NEXT_STATE <= IDLE;
                        rad_error_count <= '1';
                when others =>
                        NEXT_STATE <= IDLE;
                end case;
end process;
```

A.3 Python scripts

Python scripts used to elaborate data payloads.

A.3.1 LET script

The event time extrapolated in simulation is compared with timestamp obtained from pixel in LET mode. An histogram is generated for every TDC.

```
import os
import numpy as np
import matplotlib.mlab as mlab
import matplotlib.pyplot as plt
%matplotlib notebook

file_content = np.loadtxt('./TP_LE_100ps_64_stdCurr.results', skiprows=1, dtype=
                                        str, delimiter=' ')
tdc_range = {'0' : [],'1' : [], '2': [], '3': []}
i_ratio_tdc = [0,0,0,0]
center_tdc = [0,0,0,0]
```

```
for element in file_content:
  tdc_range[str(element[2])].append(int(element[4],16))
for i in range(0,4):
  # i_ratio for each TDC is different
  i_ratio_tdc[i] = max(tdc_range[str(i)]) - min(tdc_range[str(i)])
  # compute the center where will be applied the cut
  center_tdc[i] = (max(tdc_range[str(i)]) + min(tdc_range[str(i)])) / 2
# TDC2 center value has to be corrected to avoid unwanted cut
center_tdc[2] = center_tdc[2] + 6
# ps first test-pulse, 1.92248 are in us
tp = 1.92248 * 1000000
# ps period, 3.2001 are in us
tp_period = 3.2001 * 1000000
# ps
clock_period = 3.2 *1000
# 104857.6 ns
coarse_time_window = (2**15 * clock_period)
diff_tp_LET = {0 : [], 1 : [], 2 : [], 3 : []}
# ps time when reset ends (goes to '1')
rst = 50 * clock_period + 10
# counts of negative difference
cnt_wrong = 0
for element in file_content:
  tdc_id = int(element[2])
  t_coarse = int(element[3],16) * clock_period + rst
  if tp > coarse_time_window:
    t_coarse = t_coarse + (coarse_time_window * int(tp/coarse_time_window))
  t_fine = int(element[4],16)
  if t_fine > center_tdc[tdc_id]: #remove Counter_fine > Counter_Cuts
    t_fine = ((clock_period/i_ratio_tdc[tdc_id]) * t_fine) - clock_period
  else:
    t_fine = ((clock_period/i_ratio_tdc[tdc_id]) * t_fine)
diff_tmp = ((t_coarse-t_fine) - tp)
#Creating a dictionary for each TDC
  if diff_tmp < coarse_time_window:
    diff_tp_LET[tdc_id].append(diff_tmp)
  else:
    cnt_wrong = cnt_wrong + 1
  tp = tp + tp_period
```

```
for i in range(0,4):
  num_bins = 8
  ax = plt.figure().gca()
  n, bins, patches = plt.hist(diff_tp_LET[i], num_bins, facecolor='blue')
  plt.title("TDC-" + str(i) + " TP_time - LET_timestamp")
  plt.xlabel("ps")
  plt.ylabel("Counts")
  ax.plot()
```

A.3.2 ToT and SR script

This script compute the ToT or SR time measurement and generates a histogram for every coupled TDC.

```
import os
import numpy as np
import matplotlib.mlab as mlab
import matplotlib.pyplot as plt
%matplotlib notebook

TB = 3.2/128.0  % TDC time binning, depends on the clock frequency and
                                        Interpolation Factor of TDCs
Fine_dict = {'0':[], '1':[], '2':[], '3':[]}
Center_dict = {'0':[], '1':[], '2':[], '3':[]}
New_Center_dict = {'0':[], '1':[], '2':[], '3':[]}
Pixel = 0
file_context = np.loadtxt('../ToT_scan_clk.txt', skiprows=1, dtype=str, delimiter
                                        =' ')
Pixel_ID = file_context[:,1]
Pixel_ID = Pixel_ID.astype(int)
TDC_ID = file_context[:,2]
TDC_ID = TDC_ID.astype(int)
Coarse_counter = file_context[:,3]
Coarse_counter = Coarse_counter.astype(int)
Fine_counter = file_context[:,4]
Fine_counter = Fine_counter.astype(int)
for i in range(0, len(Pixel_ID)):
  if Pixel_ID[i] == Pixel:
    Fine_dict[str(TDC_ID[i])].append(Fine_counter[i])
```

```
for element in Fine_dict:
  Center_dict[element] = (max(Fine_dict[element]) + min(Fine_dict[element])) / 2
cnt = 0
clock = 3.2
Time_histo = []
i_TDC = [(0,1),(2,3)]
i_f = 0
i_s = 0
#calibrate TDCs center
New_Center_dict['0'] = Center_dict['0'] - 0
New_Center_dict['1'] = Center_dict['1'] - 0
New_Center_dict['2'] = Center_dict['2'] + 19
New_Center_dict['3'] = Center_dict['3'] - 1
for element in i_TDC:
  for i in range(0,len(Pixel_ID)):
    if Pixel_ID[i] == Pixel:
      if TDC_ID[i] == element[0]:
        i_f = i
        cnt = cnt + 1
    if TDC_ID[i] == element[1]:
        i_s = i
        cnt = cnt + 1
    if cnt == 2:
      t0 = CalculateTime(TDC_ID[i_f], Coarse_counter[i_f], Fine_counter[i_f],
                                        New_Center_dict[str(TDC_ID[i_f])], min(
                                        Fine_dict[str(TDC_ID[i_f])]), TB, clock)
      t1 = CalculateTime(TDC_ID[i_s], Coarse_counter[i_s], Fine_counter[i_s],
                                        New_Center_dict[str(TDC_ID[i_s])], min(
                                        Fine_dict[str(TDC_ID[i_s])]), TB, clock)
      t0 = CalculateTime(TDC_ID[i_f], Coarse_counter[i_f], Fine_counter[i_f],
                                        New_Center_dict[str(TDC_ID[i_f])], min(
                                        Fine_dict[str(TDC_ID[i_f])]), TB, clock,
                                         p_rint = False)
      t1 = CalculateTime(TDC_ID[i_s], Coarse_counter[i_s], Fine_counter[i_s],
                                        New_Center_dict[str(TDC_ID[i_s])], min(
                                        Fine_dict[str(TDC_ID[i_s])]), TB, clock,
                                         p_rint = False)
      Time_histo.append(t1-t0)
    cnt = 0
```

```
# Histogram
num_bins = int((max(Time_histo) - min(Time_histo)) * 1000 / 25) #binning equal to
                                                    TDC's binning
ax = plt.figure().gca()
n, bins, patches = plt.hist(Time_histo, num_bins, facecolor='blue')
plt.title("ToT time measuremnt TDC0/TDC1")
plt.xlabel("ns")
plt.ylabel("Counts")
ax.plot()
```

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Acronyms

ADC Analog to Digital Converter. 8, 9, 23, 25, 28, 51, 52

ALCOR A Low-power Circuit for Optical Readout. 37, 43, 44, 47, 48, 51, 68, 72, 74, 79, 82, 89, 92

AP After-Pulsing. 15–17

ASIC Application specific integrated circuit. 9, 18, 20–22, 26, 28, 34, 35, 62–64, 74, 79, 80, 82, 92

BCR Bias Configuration Register. 45, 46, 50, 64

BSCS Briged-Switches Current Sources. 88

CFD Constant Fraction Discrimination. 24, 25

CIS CMOS Image Sensor. 32

CMFB Common Mode FeedBack. 88

CMOS Complementary Metal Oxide Semiconductor. 18, 28, 30, 33, 34, 76, 94, 106

CPHA Clock Phase. 62

CPO Clock Polarity. 62

CRC Cyclic Redundancy Check. 39, 65–67

CSA Charge Sensitive Amplifier. 18, 19, 23

CT Cross-Talk. 16, 17

DAC Digital-to-Analogue. 26, 44

DAQ Data Aquistition. 8, 9, 26, 28

DCR Dark Count Rate. 6, 15, 17, 30, 32, 35

DDR Double Data Rate. 67

DLED Differential Leading Edge Discriminator. 25

DS-20k DarkSide-20k. xii, 2, 3, 6–9, 94

DSN Distributed-Sensor Network. 94, 96, 98, 103, 106, 108

ECCR End of Column Configuration Register. 52, 64, 65

EoC End-of-Column. 39, 43, 45, 56, 58, 59, 61, 63, 65–67, 80, 82

FBK Fondazione Bruno Kessler. 3, 17

FE Front-End. 18–20, 23, 24, 39, 41, 46–48, 57, 75, 94

FF Flip-Flops. 31, 32, 34, 82

FIFO First-In-First-Out. 56, 58, 62, 65, 67, 97

FPGA Field-Programmable Gate Array. 8, 9, 28, 35, 39, 62, 67

FSM Finite-State Machine. 47, 61, 62, 67, 68, 72, 73, 99

FWHM Full Width at Half Maximum. 33

HD Hamming Distance. 66

IAB Inner Active atmospheric argon Buffer. 6

IF Interpolation Factor. 49, 50, 52

ILC International Linear Collider. 26

LAr Liquid Argon. 2, 4–7

LDO Low-dropout. 80

LED Leading Edge Discriminator. 19, 24

LET Leading Edge Trigger. 46, 54

LNGS Laboratori Nazionali del Gran Sasso. 2

LSB Least Significant Bit. 45, 49, 50

LVDS Low Voltage Differential Signaling. 28, 39, 62, 74, 79, 80, 87, 89, 92

MSB Most Significant Bit. 62, 65

NRZ Non-Return-to-Zero. 89

OAB Outer Active atmospheric argon Buffer. 6

PCB Printed Circuit Board. 80

PCR Pixel Configuration Register. x, 44–49, 57, 64, 68, 69

PDE Photon Detection Efficiency. 14, 30, 32, 93

PDM Photodetector Module. 3–8, 94

PDPC Philips Digital Photon Counter. 31

PE Photon Electron. 5, 12, 13, 16, 17

PRBS PseudorRandom Binary Sequence. 89

QC Quenching Circuit. 33, 35

QDC Charge to Digital Converter. 28, 35

RGC Regulated Cascode. 41

RTL Register Transfer Level. 72, 101

SCA Switched Capacitor Array. 25, 26

SEU Single Event Upset. 56, 59, 68–72

SiPM Silicon Photomultiplier. 3, 5–7, 9, 11, 12, 14–21, 23–25, 30, 32–34, 37, 38, 41, 46–48, 55, 57, 74, 93, 94

SMA SubMiniature version A. 80

SNR Signal to Noise Ratio. 8

SPAD Single-Photon Avalanche Diode. xii, 12–16, 18, 30–35

SPI Serial Peripheral Interface. 28, 39, 44, 62–65

SPIROC SiPM Integrated Read-Out Chip. 26

SPTR Single Photon Time Resolution. 15, 33

SQB Square Board. 3

SR Slew Rate. 43, 47, 55, 57

TC Test Chip. 58, 79, 87, 92

TDC Time to Digital Converter. 9, 23, 24, 28, 30–33, 35, 41, 43–57, 74

TIA Transimpedance Amplifier. 7, 19

TMR Triple Modular Redundancy. 68–70

ToA Time-of-Arrival. 28, 74

ToF Time-of-Flight. 15, 28

ToT Time-over-Threshold. 23, 41, 43, 46, 55, 57, 74

TP Test Pulse. 47, 48, 51, 54, 55

TPC Time Projection Chamber. 2–6

TRB Triangular Board. 3

TSV Through Silicon Via. 33

UV Ultra-violet. 93

VHDL Very-high-speed-integrated-circuits Hardware Description Language. 72, 93, 101

WIMP Weakly Interacting Massive Particles. 1, 2

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