Low-Power Mixed-Signal ASIC for Cryogenic SiPM Readout

Summary

There is a growing interest in the use of Silicon photomultipliers (SiPMs) operating at cryogenic temperatures. The largely suppressed dark count rate observed at liquid Xenon and liquid Argon temperature makes such sensors ideally suited to equip large area detectors like those needed in dark matter and neutrino experiments. Research programs to explore the possibility of building total body PET scanners based on noble liquids readout by SiPM are also ongoing. Highly integrated front-end electronics embedded in the cold volume close to the sensor allows for a significant reduction of the interconnections and feed-through as data can be easily multiplexed and serialised in the digital domain. Depending on the application, the SiPM pixel size may range from a few mm^2 to a few cm^2.

The INFN-Torino group developed a low-power mixed-signal ASIC to readout SiPM at low temperature. The chip, called ALCOR, is designed in 110 nm CMOS technology, is a first prototype suitable for future 3D integration with the photon sensor. The architecture comprises of 32 independent pixels, each of them features an analogue front-end, discriminators, digital logic and low-power TDCs based on analogue interpolation. The total area of the IC is $4.95 \times 3.78\ mm^2$, where each pixel occupies $500 \times 500\ \mu m^2$ for a power consumption less than $10\ mW$. The pixel generates the timestamp of the arrival time of the event when it operates in a single photon detection mode, but it can be programmed to operate also in Time-over-Threshold where two timestamps are generated for each event. This modality is useful when many photons pile-up to yield a continuous signal. In single photon counting mode, an event rate of up to $5\ MHz$ per pixel can be accommodated. The time binning of TDCs is $50\ ps$ at the maximum system clock frequency of $320\ MHz$. The 32-bit data payloads are transmitted externally to a FPGA through four LVDS drivers with maximum throughput of $640\ Mb/s$.

Normally, digital standard cell models below $-40\ ^{\circ}C$ are not provided by the technology vendor. Therefore, a preliminary Test Chip ASIC has been produced and tested in order to get insight into cryogenic behaviour. This ASIC embeds some of critical building blocks that are employed in the mixed-signal ASIC. In particular, a digital synchronisation circuit designed with 110 *nm* standard cells has been included. This thesis reports the dedicated test results at cryogenic temperature and a comparison with SPICE simulation of extrapolated models at 77 K of the same circuits.

My personal contribution to the development of this work has been divided into three parts. The first part concerns the definition of specifications, simulation and implementation of digital circuits for ALCOR. Subsequently, I dealt with the development and cryogenic characterization of some critical digital blocks. Finally, I carried out a preliminary study of a distributed sensor network that allows to minimize the number of interconnections with the outside world while maintaining a high fault tolerance.

The Chapter 1 introduces the DarkSide-20k experiment, an underground detector for direct dark matter detection which is the future upgrade of the DarkSide-50 detector built in Laboratori Nazionali del Gran Sasso (LNGS). The detector is based on a two-phase Liquid Argon Time Project Chamber and cryogenic SiPM photo sensors to detect scintillation events.

The Chapter 2 describes briefly the structure and behaviour of SiPM photosensor and reports the state-of-art of ASICs for both analogue and digital SiPM readout.

The Chapter 3 discussed the design of the mixed-signal ASIC suitable for cryogenic SiPM readout. The chapter describes the architecture employed and the chip simulation results that describe the behaviour of the circuit.

The Chapter 4 reports the issue related to designing a digital circuit for the cryogenic environment, showing the characterisation and results of a test chip fabricated embedding important building blocks.

The Chapter 5 describes a preliminary study of a distributed readout network suitable for a large area of sensor. It describes the implementation of the network in a 3D digital SiPM where data are digitised and multiplexed reducing the cable connection at the minimum necessary.

Keywords: Noble liquid detectors, Mixed analogue digital integrated circuits, Timing, Cryogenic electronics.