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Software Solutions to Mitigate the Electromagnetic Emissions of Power Inverters

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* * * * * *

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Michele Perotti

Turin, May 2020

Mi l'hai guardà le nivule ch'a curiu 'n tel ciel

Gianni Comino

Gli scienziati sono tante formiche, tante api: ciascuno porta all'alveare tutto quello che può raccogliere.

Quintino Sella

Summary

Nowadays, the switching circuits have become the most used system to convert voltages and currents, in order to supply electrical devices or to drive electrical loads, such as motors. The design of such switching circuits, should take into account not only the power electronics issues, but also the Electromagnetic Compatibility (EMC) ones. Indeed, each electronic system, in order to be sold, should be able to withstand to electromagnetic (EM) disturbances (immunity) as well as to not generate electromagnetic interferences (EMI) over a standard defined limit (emission). The electromagnetic emission, in particular the conducted ones, i.e. the one that propagates in the power supply cables, are usually reduced using power line filters. Such filters are composed by a large inductor, the common mode choke, and some capacitors, in order to confine the generated disturbances at the board power supply input. Such a choke is usually bulky, expensive and heavy. For these reasons, in recent years, the research activity in EMC field has been oriented in developing new techniques to reduce the filter's dimensions or even to remove it. These techniques are mainly software based, such as Spread Spectrum Modulation (SSM) or waveform shaping. However, these approaches present some disadvantages: the first spreads the disturbance signal over a wider frequency band, without reducing its total energy; the latter could reduce the efficiency of the switching circuit, and it requires *ad hoc* gate drivers in order to be implemented.

This work aims to develop and propose a new conducted emission mitigation technique based on software, in order to reduce the power line filter size. Such a technique is applicable whenever a bipolar PWM is used, i.e. the switching circuit should present couples of output nodes switched oppositely. Every time the outputs are switched, during the transition some high frequency current is injected in the parasitic capacitances present between the output switching node and the chassis. This current is defined as common mode conducted emission. If a bipolar PWM is used, such transitions are opposite and synchronized; if the rising and falling times are equal and the parasitic capacitance related to the output nodes have the same value, the disturbance current is internally recovered and it is not measured by the EMI receiver. However, this usually does not occur, since the propagation of the output control signals is affected by a delay, which cannot be determined *a priori*. Due to this delay, the output transitions are not complementary, and some CM

current flows in the parasitic capacitances and it is measured by the EMI receiver instrument. From the analytical evaluation of the disturbances, the larger is the delay, the higher are the CM emissions at low frequencies, and therefore the filter needed for the EMI attenuation is larger.

For these reasons, in this work, a closed-loop technique able to compensate the delay, i.e. to align the output waveform transitions, has been developed. The proposed technique exploits a software algorithm, combined with a simple and low-cost sensing circuitry to compensate the delay between the switching circuit outputs. The proposed technique works for bipolar switched circuits. In order to prove its effectiveness, a BLDC motor driver has been designed and prototyped. Using the test bench proposed in the standard CISPR25, the CM emissions have been measured. Two cases have been considered: the first in which a delay is present between the output transitions, approximately equal to 100 ns; the second in which the closed loop delay compensation is active. In the second case the CM EMI spectrum is reduced by 17 dB (best value) with respect to the first case. As found in the analytical evaluation of the delay compensation, the technique is efficient in the lower part of the spectrum; however, in the higher part the emissions are not worsened. The closed-loop delay compensation technique, unlike the SSM technique, reduces the disturbance energy. Since the two EMI reduction techniques work independently, they can be used together in order to obtain a further reduction of the conducted emissions.

If the EMC requirements are still not met, a filter is needed anyway. Unlike the case in which the proposed technique is not implemented, where a classical commercial filter is used, the employment of the delay compensation technique allows the designer to reduce the conducted EMI filter size, gaining a reduction in weight, volume and cost.

Acknowledgements

I would like to express my deep gratitude to my supervisor Prof. Franco Fiori, especially for his useful critiques along the development of this research work. I would also acknowledge all the people who have supported me during these years: my family, my PhD colleagues Erica, Marco, Mark, Vincenzo, and all my friends.

Lastly, I would like to thank the Power Electronics Innovation Center (PEIC), whose support allowed me to use innovative instrumentation to perform this research work.

Contents

Chapter 1

Introduction

The electromagnetic compatibility (EMC) issues in designing power electronic circuits represent a challenging task for designers. The EMC can be defined as "the ability of an electronic system to work properly in its intended electromagnetic environment, and to not contribute interference to other systems in the environment" [1]. Therefore, each electronic system should be able to work in electromagnetic polluted environments (immunity) as well as to not generate high level of electromagnetic interference (EMI).

In this work, only the electromagnetic (EM) emission issues are addressed. The maximum EMI level that an electronic system can generate, is defined in international standards, like CISPR 14 [2] for household appliances and CISPR 25 [3] for automotive applications. These standards, besides indicating the maximum emission levels, define also the test setup which should be used performing the EMI measurements. If the requirements are not met, the designers should employ EMI reduction techniques to reduce the EMI. In the following Section the generation of the electromagnetic emissions is explained in details.

1.1 Generation and propagation of EM emissions

In electrical and electronic system, the electromagnetic compatibility issues arise when three elements are present: a source of the EM emission, a victim and a coupling path connecting the two. In general, the EM noise can be generated by all the signals which are characterized by a non negligible dv/dt and di/dt magnitude. This noise can affect the operation of other electronic equipment, susceptible to that interference, i.e. the victim circuits. In order to be effective in interfere with the victim circuit operation, the EMI should be characterized by enough amplitude (or power) at the frequencies at which the victim is susceptible. In addition, the time duration of the noise generation is important for the characterization of the victim immunity [4].

Focusing on the coupling channel, there are two possibilities for the noise propagation. The EMI can propagate in free space as electromagnetic waves, i.e. the radiated emission, or it can propagate as disturbance current in power supply cables and interconnections, i.e. the conducted emissions [5].

Often, exploiting the reciprocity effect, if the emission issues are solved for a given circuit, also its immunity to EMI is improved.

In the following paragraphs, the two coupling methods are detailed.

1.2 Conductive Coupling

The most evident channel for the propagation of the EMI is the direct conductive contact between the noise source and the receiver circuit. This connection can be represented by the printed circuit board (PCB) traces, the interconnecting cables, the data communication lines, etc. In particular, the power line cables represent the classical path for EM noise transmission. The power line can be represented by the mains, in household and industrial appliances, or by the battery distribution system in automotive applications.

The conducted emission can be a direct form of interference for the circuits connected to the same power line, or the power line itself can behave like an antenna and radiate the interference in the surrounding environment.

This conducted interference propagates as common mode, i.e. between the power line and a reference conductor, usually represented by the chassis of the device, or differential mode, i.e entering in the positive supply cable and coming back from the return one. This distinction is analyzed in details in Section 1.5.

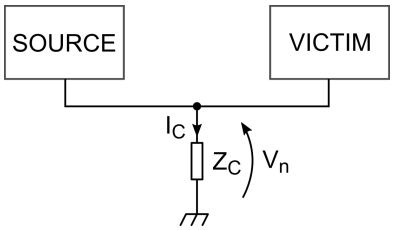

Figure 1.1: Common Impedance EMI propagation path.

Another path for the conductive EMI transmission is the common earth impedance [6], shown in Fig. 1.1. When the EMI source inject high frequency current in the common impedance, usually modeled with an inductance, the victim circuit experiences a variation on the voltage at the common terminal, which propagates internally. Indeed, when high di/dt current is injected in the common impedance $Z_C \approx L$, the resulting voltage at the ground connection of the victim circuit is:

$$V_n(t) = L\frac{dI_C(t)}{dt}. \tag{1.1}$$

The current I_C, in particular in switched circuits, can be represented by a waveform with high di/dt transients, which generate voltage spikes on the common impedance. These spikes can be responsible of failures in the victim circuit.

1.3 Radiated Coupling

The other coupling channel for EM noise is the radiated one. This coupling mechanism can be represented in three different ways: magnetic coupling, electric coupling and far field coupling. The former two are in general low frequency, near field coupling mechanisms and they are shown in Fig. 1.2.

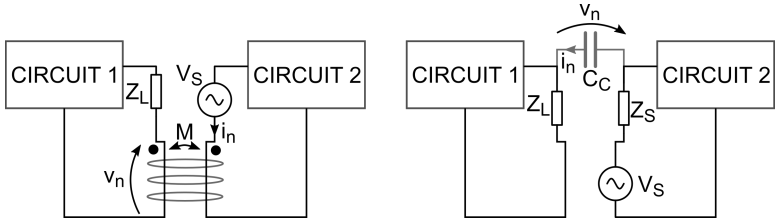

Figure 1.2: Radiated emission coupling mechanisms: the magnetic coupling (on the left) and the electric coupling (on the right).

The magnetic, or inductive, coupling is caused by the high frequency current flowing in a conductor. This current flow, according to the Lenz's law, generates a magnetic field which couples with the surrounding conductors. Such coupling mechanism can be modeled with the mutual inductance present between the two conductors. The voltage generated in the victim conductor by the disturbance current i_n can be evaluated as:

$$v_n(t) = M\frac{di_n(t)}{dt}, \tag{1.2}$$

where M is the mutual inductance between the two conductors. This parameter depends on the areas of the conductor loops and on the distance between them.

The electrical coupling, instead, is due to the capacitive coupling between the conductors. High dv/dt transients generate high frequency current flow in the mutual capacitances present between two conductors. The current flowing to the victim conductor can be expressed as:

$$i_n(t) = C_C\frac{dv_n(t)}{dt}, \tag{1.3}$$

where C_C is the coupling capacitance.

The third coupling mechanism is due to the electromagnetic wave propagation between the source and the victim. The electromagnetic field is generated in a conductor, which acts as an antenna. This field propagates in the surrounding space,

with a speed dependent on the relative permittivity of the propagation medium. In near field, the nature of the wave depends on the characteristics of the source: if the source is a current the generated field is mainly magnetic, while if it is generated by a voltage variation it is mainly electric. In far field condition, instead, the only components which propagate, according to the Maxwell's laws, are the one orthogonal to the direction of propagation, and the field can be represented as a plane wave. In far field condition, the ratio between the E field and the H field is constant and, in vacuum, is equal to:

$$Z_0 = E/H = \sqrt{\mu_0/\varepsilon_0} = 377\Omega. \tag{1.4}$$

In this third case of coupling the victim circuit acts as a receiving antenna. The interferences are generated from the high dv/dt and di/dt signals which flow in conductors which have dimensions of $\lambda/4$ with respect to the frequency band of interest. For example, for an emission frequency of 100 MHz, $\lambda/4 = 0.75$ m. From this consideration, it can be concluded that the radiated emissions are effective at high frequency, i.e. over a few hundred of MHz [6].

In the present work, only the conducted emissions are considered. In order to evaluate the magnitude of such emissions, several standard have been developed in the past. In the following Section, in particular, the CISPR25 standard is analyzed.

1.4 Measurement of Conducted Emissions

The conducted emission are regulated by international standards. In this work, the CISPR25 standard [3], employed in the automotive field, has been used as reference. This standard defines the test setup for the various equipment under test (EUTs) according to their functionality and to their placement with respect to the chassis of the vehicles.

The conducted emission measurements aim to evaluate the spectrum of the disturbance current flowing in the power supply cables. This current depends on the impedance seen from the EUT towards the power supply source, which has a strong variability according to the measured system. For this reason, in order to obtain repeatable results and to standardize the measurement process, one or two Line Impedance Stabilization Networks (LISNs) should be used. These circuits are needed to fix the impedance that the EUT sees from its power supply terminals towards the power source. The LISN circuit, according to CISPR25 is shown in Fig. 1.3.

The conducted emissions, according to CISPR25, should be measured from 150 kHz to 30 MHz, and from 30 MHz to 108 MHz to evaluate the disturbances in the radio communication band. Therefore, the LISN circuit has been designed in order to show, for low frequencies, a negligible impedance toward the EUT and an high impedance toward the RF measurement port, in order to allow the supply of

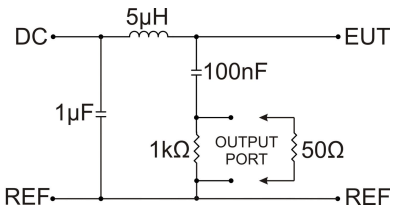

Figure 1.3: LISN circuit.

the EUT. Indeed, at DC, the inductor can be approximated as a short circuit, and the 100 nF capacitor as a open circuit. For the conducted emissions frequency range, instead, such a network shows an impedance of around 50 Ω, since the inductor and the capacitor can be considered as an open and a closed circuit, respectively. The 1 kΩ resistor is used to discharge the LISN capacitors when both the load and the EUT are disconnected, preventing the user from electrical shock.

The impedance seen from the EUT power supply terminals towards the power line, evaluated using the test bench reported in Fig. 1.4, is shown in Fig. 1.5.

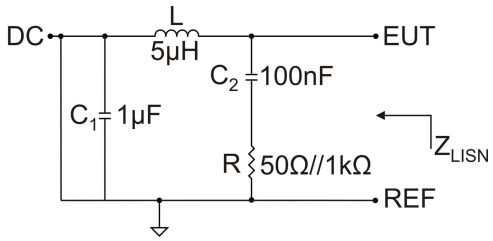

Figure 1.4: Test setup for the evaluation of LISN impedance.

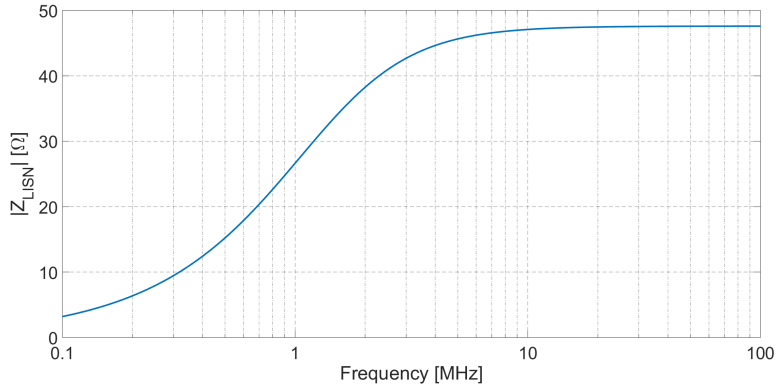

Figure 1.5: LISN impedance according to CISPR25.

Since in the conducted frequency range the LISN shows an impedance of around 50 Ω, the whole circuit can be approximated as a 50 Ω resistance.

The following Section provides an overview of the needed equipment for the conducted emission measurement.

1.4.1 Test equipment and setups for conducted emission measurement

In order to perform the conducted emission measurements, the system is placed on a conductive ground plane, usually made of copper. This reference plane has to be placed 0.9 m above the floor, with a non conductive support. Both the LISN and the EUT should be placed on the reference plane: the LISN chassis has to be connected to the plane, and the EUT is generally isolated from the plane. According to the EUT ground connection in the actual application, it is possible to distinguish between two cases:

- EUT locally grounded (ground line equal or shorter than 200 mm): one LISN is required, connected to the positive power supply line.
- EUT remotely grounded (ground line longer than 200 mm): two LISNs are needed, one for the positive supply line and one for the negative one;

The EUT is connected to the LISN(s) and it is placed on a non conducting, low permittivity ($\varepsilon_r < 1.4$), 50 mm thick platform. The distance between the EUT and the reference plane edges should be greater than 200 mm, and the cables connecting the LISN and the EUT have a standard length of 200 mm.

The power supply to the system shall be provided by a battery, which is placed out of the reference plane and its return cable is connected to the reference plane between the LISN and the plane edge.

The RF output of the LISN is connected to the EMI receiver with a coaxial cable. The EMI receiver, according to the standard, could be substituted with a spectrum analyzer. The RF output of the LISN not connected to the receiver should be terminated on a 50 Ω load.

The test procedure is different according to the two cases presented before. For the remotely grounded EUTs the conducted EMI measurements should be performed on both positive and negative LISN outputs, while for locally grounded EUTs the measurement is performed only on the positive terminal, since only one LISN is present.

The two possible test setups, according to CISPR25, are shown in Figs. 1.6 and 1.7.

1.4.2 Limits for conducted emissions

The measurements can be performed with three types of detectors: peak, quasi-peak and average detector. The peak detector is the most used in measurement

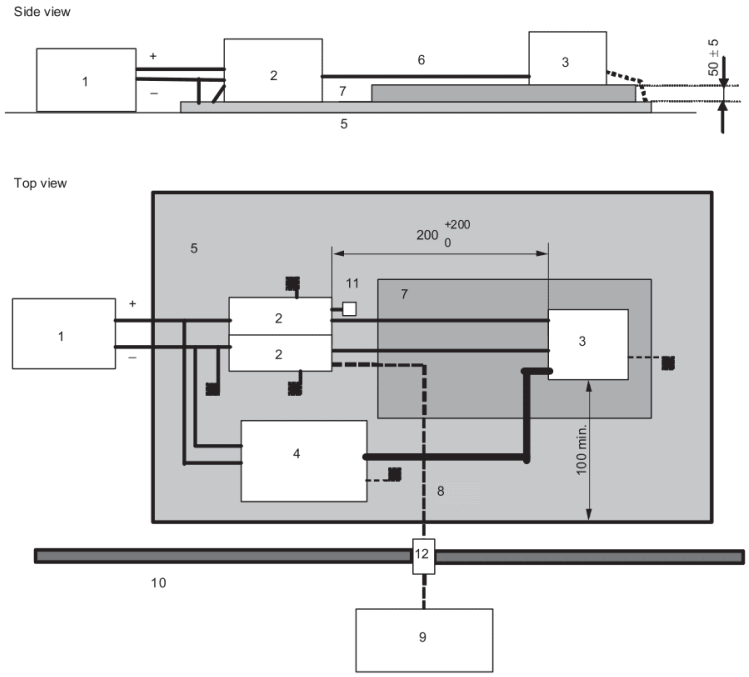

Figure 1.6: Test setup for remotely grounded EUTs according to CISPR25. Legend: 1 - Power supply; 2 - LISN; 3 - EUT; 4- Load simulator (if required); 5 - Ground plane; 6 - Power supply line; 7 - Low relative permittivity support; 8 - Coaxial cable; 9 - Measuring instrument; 10 - Shielded enclosure; 12 - Bulkhead connector

instruments. The signal is filtered with an intermediate frequency (IF) filter and it is given as input to an envelope detector. The measured signal is the one at the output of the envelope detector.

The quasi-peak detector is a particular envelope detector designed to have a charge time shorter than the discharge one. In this way, if the signal repetition rate is high, the filter capacitor will be charged more. The signal power read with the quasi-peak detector is always less or equal to the one read with the peak detector.

The average detector is used only in conducted emission measurements and provides an average value of the detected envelope.

The CISPR25 standard defines some limits for the emission generated by the EUTs. Those limits, shown in Tab. 1.1, are not mandatory, since each manufacturer can define more strict requirements.

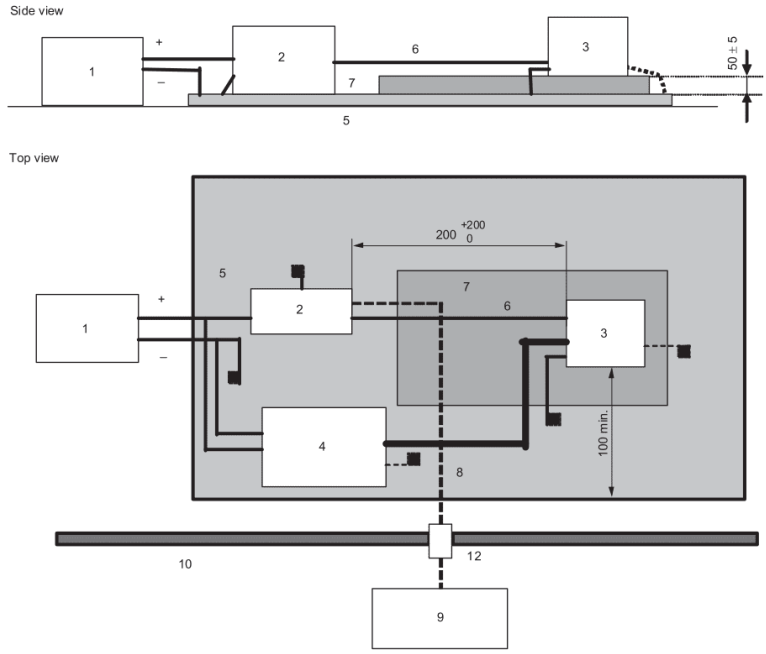

Figure 1.7: Test setup for locally grounded EUTs according to CISPR25. Legend: 1 - Power supply; 2 - LISN; 3 - EUT; 4- Load simulator (if required); 5 - Ground plane; 6 - Power supply line; 7 - Low relative permittivity support; 8 - Coaxial cable; 9 - Measuring instrument; 10 - Shielded enclosure; 12 - Bulkhead connector

Table 1.1: CISPR25 conducted emission limits

Band	Freq. [MHz]	Levels [dBμV]									
		Class 1		Class 2		Class 3		Class 4		Class 5	
		P	QP	P	QP	P	QP	P	QP	P	QP
Broadcast											
LW	0.15-0.30	110	97	100	87	90	77	80	67	70	57
MW	0.53-1.8	86	73	78	65	70	57	62	49	54	41
SW	5.9-6.2	77	64	71	58	65	52	59	46	53	40
FM	76-108	62	49	56	53	50	37	44	31	38	25
TV Band I	41-88	58	-	52	-	46	-	40	-	34	-
Mobile Services											
CB	26-28	68	55	62	49	56	43	50	37	44	31
VHF	30-54	68	55	62	49	56	43	50	37	44	31
VHF	68-87	62	49	56	43	50	37	44	31	38	25

1.5 Conducted Emissions: Common Mode and Differential Mode

When the remotely grounded equipment test setup is used, it is possible to distinguish between two modes of emissions: common mode (CM) and differential mode (DM) emissions. The distinction between the two modes is useful when the imposed limits are exceeded, in order to design an EMI mitigation system. Indeed, as will be explained in the following sections, according to the emission mode there are different design approaches. The conducted emission test setup is shown in Fig. 1.8. In the following paragraphs the DM and CM are analyzed.

1.5.1 Differential Mode Conducted Emissions

In order to perform the following analyses, switching circuits, such as inverters, switched mode power suppliers, etc., are considered as example. In switching circuits, the power supply voltage is chopped by the commutation of power transistors. Therefore, the current absorbed by the EUT is not constant, but it is given by the superposition of the actual DC current consumption and a current ripple, generated by the modulation. In order to confine this ripple current into the EUT and to maintain the supply voltage stable, an input capacitor is inserted.

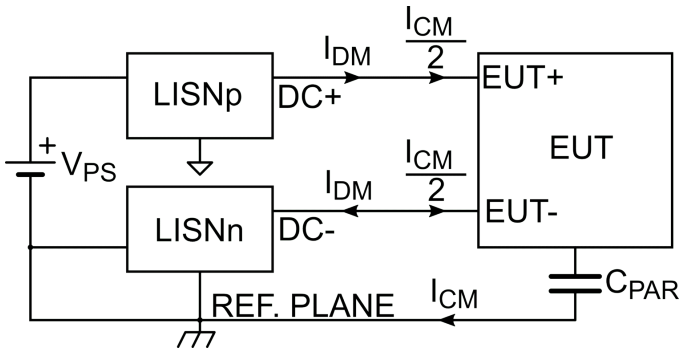

Figure 1.8: Block scheme for conducted emission measurement.

Such an input capacitor, most of the times is electrolytic, so it presents a non negligible equivalent series resistance (ESR) and an equivalent series inductance (ESL). The capacitor impedance is shown in Fig. 1.9. Therefore, for the conducted emission frequency range, such a capacitor behaves like a resistance or an inductor, so, actually, its filtering behavior is not as efficient as in the ideal case.

On these bases, an equivalent circuit can be derived for the propagation of the ripple current, which is shown in Fig. 1.10. The ripple current I_{EUT} is partitioned between the input capacitor impedance and the LISNs impedance. So, it is possible to define the differential mode emission current as the current which flows into the

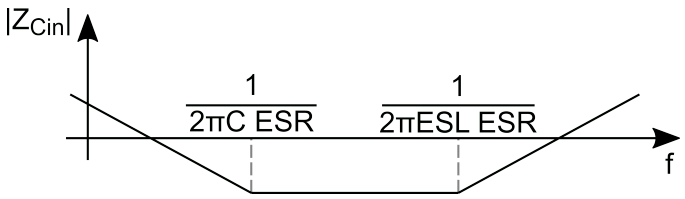

Figure 1.9: Input capacitor impedance.

positive power supply terminal of the EUT and exits from the negative one. This current circulates in the LISN impedance, and it is sensed by the EMI measurement instrument. The LISN impedances, in this case, are in series; so the equivalent LISN impedance can be approximated to $Z_{\mathrm{LISN,DM}} = 100\,\Omega$ [4].

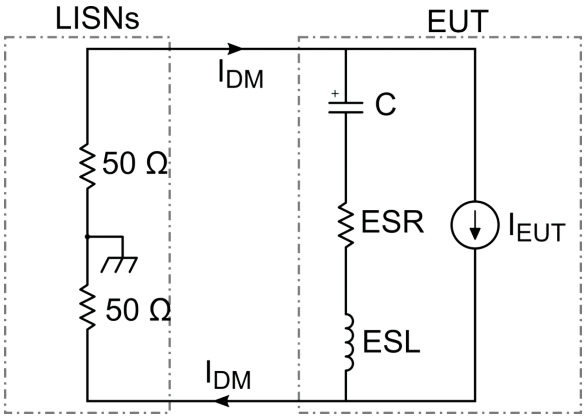

Figure 1.10: Differential Mode equivalent circuit for conducted emission test setup.

According to the circuit shown in Fig. 1.10, the spectrum envelope of the differential mode current can be evaluated:

$$I_{\mathrm{DM}} = I_{\mathrm{EUT}}(s) \cdot \frac{ESR + s\,ESL + 1/sC}{Z_{\mathrm{LISN,DM}} + ESR + s\,ESL + 1/sC}. \tag{1.5}$$

1.5.2 Common Mode Conducted Emissions

When the conducted emissions are measured, as stated in the previous Section, the EUT is isolated from the reference plane. This isolation introduces some parasitic capacitances, in which high frequency current can be injected. This current can be defined as common mode (CM) current, since flows from the power supply terminals into the EUT, it is injected in the parasitic capacitance, it flows back into the LISN impedance and then it is measured by EMI receiver. The equivalent circuit for the common mode emission path is shown in Fig. 1.11. Since the CM current flows with the same direction in both positive and negative supply lines, the

two LISNs can be considered in parallel. Therefore, the equivalent LISN impedance is $Z_{\mathrm{LISN,CM}} \approx 25\,\Omega$.

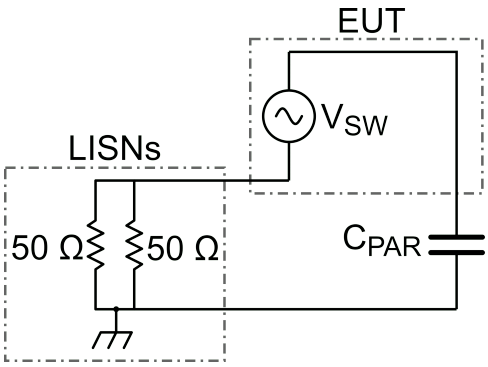

Figure 1.11: Common Mode equivalent circuit for conducted emission test setup.

In particular, in switching circuits, the CM EMI is generated by the nodes which commutate with high dv/dt. Indeed, the current in the parasitic capacitances can be expressed as:

$$I_{\mathrm{C}}(t) = C_{\mathrm{PAR}} \frac{dv_{\mathrm{C}}(t)}{dt}, \tag{1.6}$$

so, the higher the slew rate, the higher the magnitude of the injected current. Finally, the CM voltage at the LISNs output can be computed as:

$$V_{\mathrm{CM}} = V_{\mathrm{SW}}(s) \cdot \frac{Z_{\mathrm{LISN,CM}}}{Z_{\mathrm{LISN,CM}} + 1/(sC_{\mathrm{PAR}})} = V_{\mathrm{SW}} \cdot \frac{sC_{\mathrm{PAR}} Z_{\mathrm{LISN,CM}}}{1 + sC_{\mathrm{PAR}} Z_{\mathrm{LISN,CM}}} \tag{1.7}$$

1.5.3 Measurement of CM and DM conducted emissions

The CISPR standard defines the limits for the total emission measured at the LISNs outputs, i.e. the standard does not provide separated limits for CM and DM EMI. By the way, the separation of the two emissions modes is useful for the designer, since the two mode EMIs can be reduced using different approaches. In order to separate the CM EMI from the DM it is not possible to use directly the EMI receiver or the spectrum analyzer. The reason is that the two measurements, referred to the two LISNs outputs respectively, are performed in different time instants and the phase information is not recorded by the instrument. Aiming to address this issue, different techniques have been developed. One of them, which allows the user to measure only the CM EMI, consists in using a differential mode rejection network (DMRN). This network was proposed by Nave [7] and it is made of three star-connected resistors, where two terminals of the star are connected to the LISNs output ports and the remaining terminal is connected to the EMI

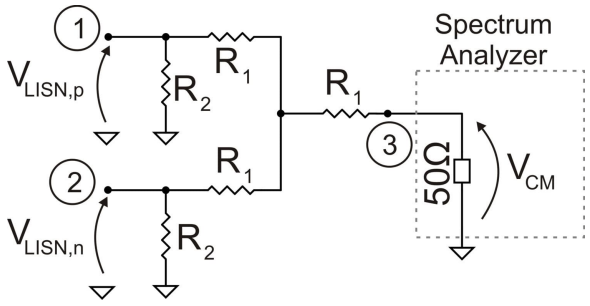

Figure 1.12: Differential mode rejection network.

measurement instrument. Each LISN output is loaded with a 50 Ω resistor. The network is shown in Fig. 1.12.

Another technique used to separate the CM and DM emissions was proposed by Paul and Hardin in [8] and it employs two transformers, to add or to subtract the two LISNs output signals. The transformers should have high bandwidth, wider than the conducted emissions frequency range. Moreover, the transformer should have flat response. The circuit is shown in Fig. 1.13.

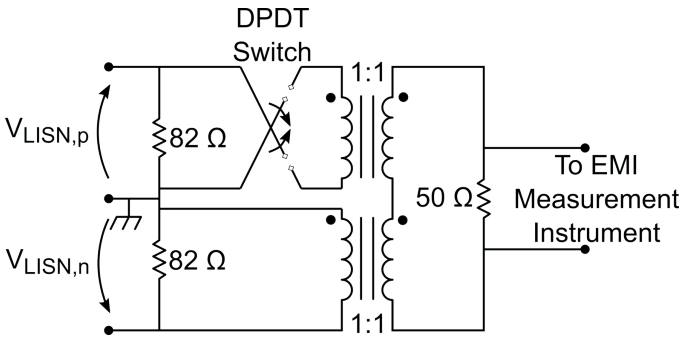

Figure 1.13: Switchable CM-DM separation network.

Since in this work only the CM conducted emissions are considered, the DMRN has been chosen to separate the two emission modes. It is worth underlining that the resistors absolute value is not as important as their matching, because if the resistance of the three star resistors R_1 is not equal, a portion of the DM emissions reaches the spectrum analyzer. However, the absolute value of the resistors is fundamental in order to know the relationship between the CM voltage at the LISNs outputs and the one measured at the DMRN end. The resistors selected values are $R_1 = 28.7\,\Omega$, 1% and $R_2 = 49.9\,\Omega$, 1%. The CM voltage sensed by the spectrum analyzer is:

$$V_{\mathrm{CM}} = \frac{V_{\mathrm{LISN,p}} + V_{\mathrm{LISN,n}}}{2} \cdot 2 \cdot \left(\frac{(R_1 + 50\,\Omega) \parallel R_1}{(R_1 + 50\,\Omega) \parallel R_1 + R_1} \cdot \frac{50\,\Omega}{R_1 + 50\,\Omega} \right). \tag{1.8}$$

The impedance seen by the CM output is lower than 25 Ω, since it is given by the parallel of the 50 Ω resistor and the impedance connecting the LISNs to the spectrum analyzer. The impedance Z_{CM} can be expressed as:

$$Z_{\mathrm{CM}} = \frac{R_2}{2} // \left(\frac{3}{2}R_1 + 50\,\Omega\right). \tag{1.9}$$

The DMRN should be connected to the two LISNs shown in Fig. 1.8 at their measurement ports, in lief of the 50 Ω resistors.

In order to verify the symmetry of the DMRN network, the device has been characterized using an HP8753ES vector network analyzer (VNA). The measurement ports for the scattering matrix are defined in Fig. 1.12. In order to verify the symmetry of the prototyped network, it is possible to compare the transmission coefficients S_{31} and S_{32}: if they are identical in magnitude and phase, the network is symmetrical. The measurement results are shown in Fig. 1.14. In this figure it can be seen that the network shows a resistive behavior up to 100 MHz. Moreover, the two lines are overlapped. This means, respectively, that the network parasitics and the mismatch between the two branches can be neglected.

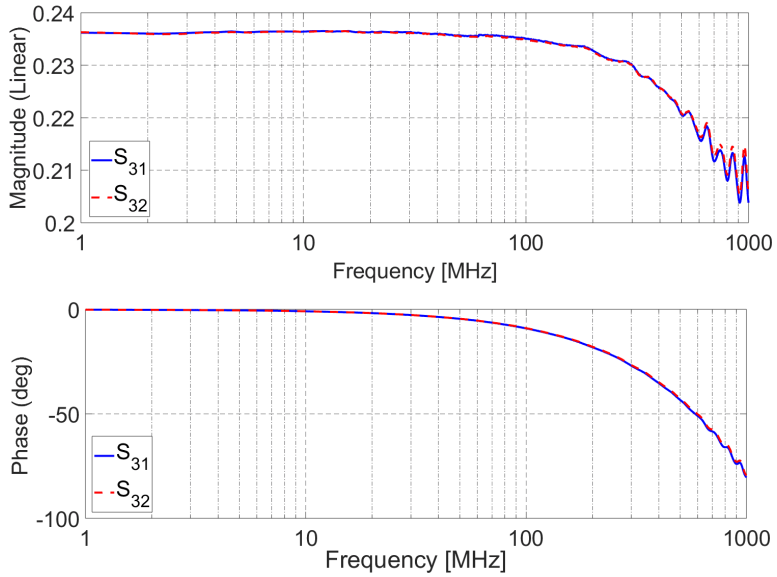

Figure 1.14: DMRN transmission scattering parameters comparison.

1.6 Conducted emissions generation in switching circuits

Electric loads, like motors and actuators, are usually driven by switching circuits, such as power inverters. Such circuits convert a DC voltage into an AC one.

The basic schematic for a full-bridge inverter is shown in Fig. 1.15.

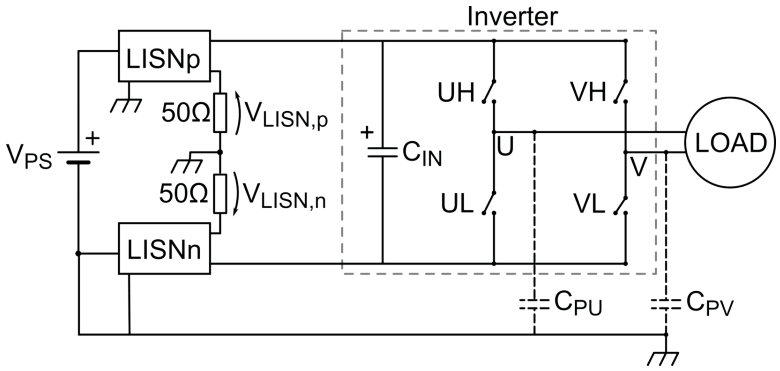

Figure 1.15: Single-phase inverter general schematic.

The two output waveforms, at the nodes U, V, are obtained using pulse width modulation (PWM). The switches are switched on and off at a frequency $f_{\text{sw}} = 1/T_{\text{sw}}$, which should be much greater than the output waveform frequency. The output nodes U and V are therefore connected either to the power supply or to ground for a time interval equal to $D \cdot T_{\text{sw}}$ and $(1 - D) \cdot T_{\text{sw}}$, respectively, where $0 < D < 1$ is defined as duty cycle. For the single-phase, full-bridge inverter, two PWM modulation strategies are usually employed: the Unipolar PWM and the Bipolar PWM [9].

With Unipolar PWM the outputs are controlled as in Fig. 1.16, where V_{L} is the voltage on the load:

$$V_{\text{L}} = V_{\text{U}} - V_{\text{V}} \tag{1.10}$$

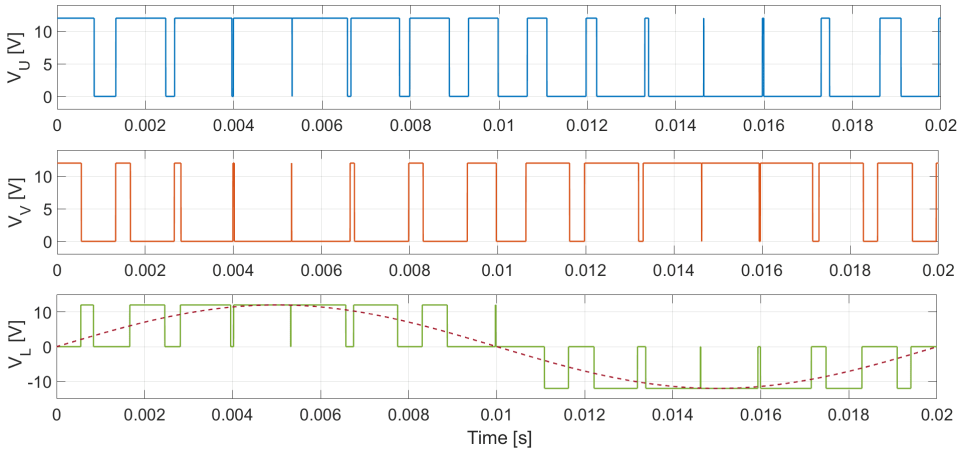

Figure 1.16: Unipolar PWM.

The Bipolar PWM strategy, instead, consists in switching the outputs of the inverter complementary, i.e. when the U output is high, the V output is low, and *viceversa*. The output voltages are shown in Fig. 1.17.

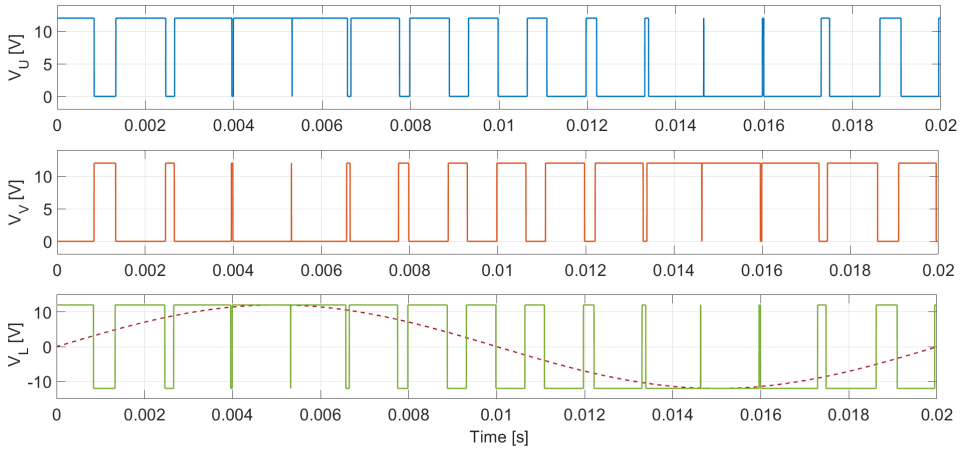

Figure 1.17: Bipolar PWM.

From the inverter output waveforms it is possible to estimate the conducted emissions. Focusing on the DM emissions, the differential mode current is given by the current ripple present on the load, partitioned between the input capacitor C_{IN} and the LISNs impedance. For what concerns the DM emissions, the unipolar PWM produces a lower voltage ripple on the output with respect to the bipolar PWM, and therefore, a lower current ripple.

The common mode disturbance instead, is given by the summation of two contributions: the current generated in the parasitic capacitances present between the output nodes and the reference plane, and the current generated in the parasitic capacitance between the power supply and the reference plane. This second contribution is given by the voltage ripple present on the power supply nodes with respect to the reference plane; in general, since this voltage ripple is much smaller with respect to the output voltage transitions, and it has lower dv/dt, it can be neglected.

Focusing on the first contribution, the current injection in the parasitic capacitance referred to the output nodes is due to the output commutation. Every time one output commutates high to low or low to high a current pulse is sunk or injected into the respective parasitic capacitance, it flows into the LISNs impedance and it is measured by the EMI measurement instrument. Looking at the waveforms of Fig. 1.16 and 1.17, it is possible to see that the bipolar approach allows to reduce the CM current, since, if the outputs are complementary and $C_{\mathrm{PU}} = C_{\mathrm{PV}}$, the CM current toward the LISNs is nulled. This happens because the pulsed current injected in one capacitance, is recovered by the other parasitic capacitance. Using

the unipolar approach, instead, the CM current is never recovered, so it flows for every output commutation into the LISNs impedance and it is measured by the spectrum analyzer.

Finally, since between the CM and the DM, the CM is harder to mitigate [10], the use of bipolar PWM is preferable since it allows to partially reduce the generation of the disturbance.

In the following Chapter, the main approaches in reducing the conducted EMI are presented.

Chapter 2

Conducted Emission Mitigation

In order to mitigate the conducted emissions, the approaches developed in the past years can be classified two categories: the hardware techniques and the software ones. The hardware approaches in reducing the EMI are based on the addition of specific circuits to the EUT, addressed to the reduction of the EM interference. The software ones, instead, are mostly based on an accurate control of the critical signals responsible of the EMI generation. In this Chapter, the most used techniques belonging to each of the two categories are presented. In particular, for the hardware techniques the passive and the active filters are analyzed. Focusing on the software ones, instead, the Spread Spectrum Modulation (SSM) and the waveform shaping are depicted.

2.1 Passive power line filters

The most used approach in reducing the conducted EMI consists in inserting a passive filter at the power supply input. Such a circuit is a LC low-pass filter, composed of two sections: one for the reduction of the common mode and the other for the mitigation of the differential mode emission [10]. Consequently, it is evident that it is important to distinguish the two emission modes. In order to design the power line filter is therefore possible to separate the CM and DM emission sources, and to use the simplified circuit presented in 1.5.3 to estimate the EMI level. The power line filter is shown in Fig. 2.1.

The common mode filtering section is composed of two coupled inductors L_{CM}, wounded on the same magnetic core, and of two capacitors, C_{Y} connected between the power lines and the chassis, respectively. The CM inductance does not influence the differential mode current, since the magnetic flux generated by the current flowing in one inductor is canceled by the one of the other inductor. Looking at the equivalent circuit of Fig. 2.2, the emission source voltage is partitioned between the parasitic capacitor C_{PAR} and the capacitors C_{Y}, which for the CM are

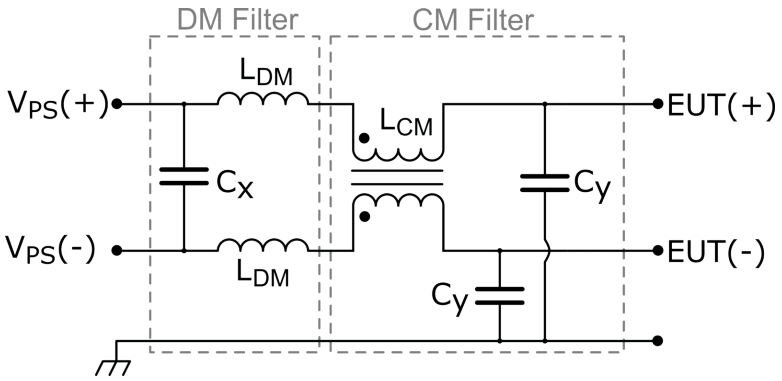

Figure 2.1: Power supply conducted emission filter.

in parallel. The output of the CM filter is loaded with the LISNs CM impedance, i.e. $Z_{\mathrm{LISN,CM}} = 25\,\Omega$.

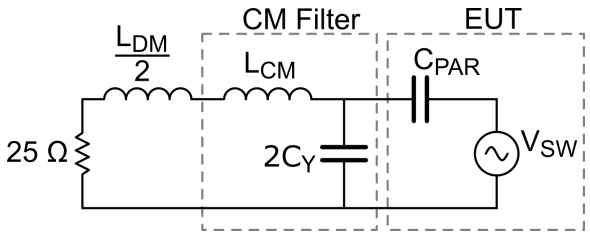

Figure 2.2: Equivalent circuit for CM EMI filtering.

Considering now the differential mode filtering elements, the filter behaves like a second order low-pass filter, loaded with the LISN impedance, which for the differential mode path is equal to $Z_{\mathrm{LISN,DM}} = 100\,\Omega$. The equivalent circuit is shown in Fig. 2.3. The DM filter inductance, L_{DM} is obtained from the leakage inductance of the CM choke. If needed, this inductance can be increased adding additional inductors. The capacitors C_{Y}, for DM, are connected in series, and generally their capacitance is not sufficient to filter the DM current. Consequently, an additional C_{X} capacitance is connected between the two power lines.

In the following paragraph, the design approach for power line filter is presented. The reference circuit for these analyses is an half bridge, reported in Fig. 2.4.

2.1.1 Filter design

In this paragraph, the design of a power supply filter is presented [11]. The design of such filters starts from two elements: the limits imposed from the used standard and the emission spectra generated from the common mode and differential mode sources.

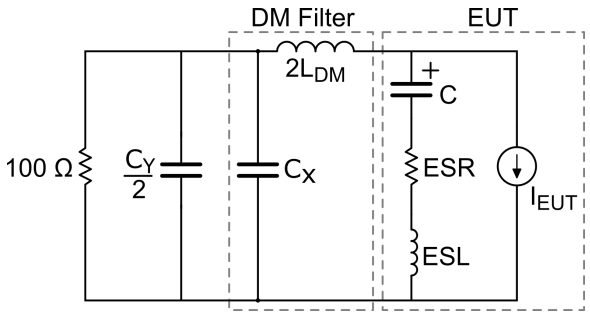

Figure 2.3: Equivalent circuit for DM EMI filtering.

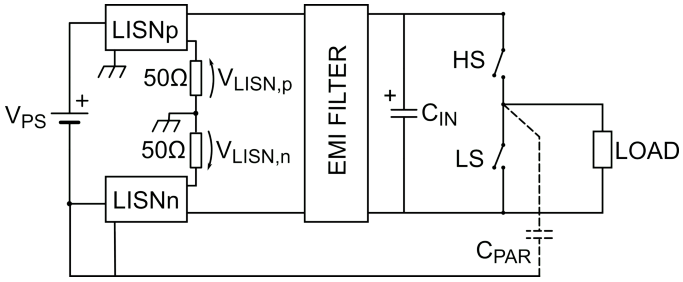

Figure 2.4: Half bridge circuit.

Starting from the CM emission, the equivalent circuit is shown in Fig. 2.2. The CM source is the trapezoidal voltage present at the output node of the circuit. This source is connected to the parasitic capacitance existing between the output node and the reference plane. The circuit is closed on the LISNs impedance. In order to verify if the filter is needed for the CM, the CM spectrum on the LISNs should be computed, using Eq. 1.7. Then, the spectrum is compared with the imposed limits, and if those limits are exceeded, a filter should be placed. In order to filter the CM, a possible approach consist in designing a voltage divider between C_{PAR} and the filter capacitance, adding a inductance to obtain a low-pass second order filter.

First the cutoff frequency of the second-order filter should be designed. If an attenuation A_{CM}, expressed in linear units, is required at a frequency $f_{\mathrm{A,CM}}$, the cutoff frequency $f_{\mathrm{c,CM}}$ can be computed as:

$$f_{\mathrm{c,CM}} = f_{\mathrm{A,CM}}\sqrt{A_{\mathrm{CM}}}. \tag{2.1}$$

Using this cutoff frequency value, the filter can be designed with the following equation:

$$f_{\mathrm{c,CM}} = \frac{1}{2\pi\sqrt{L_{\mathrm{CM}}2C_{\mathrm{y}}}}. \tag{2.2}$$

The degree of freedom in the choice of L_{CM} and C_{y} can be exploited imposing

the quality factor Q of the filter equal to 1, avoiding an amplification of the spectral component near to the cutoff frequency:

$$Q = \frac{\sqrt{\frac{L_{\mathrm{CM}}}{2C_{\mathrm{y}}}}}{Z_{\mathrm{LISN,CM}}} = 1 \quad \rightarrow \quad \sqrt{\frac{L_{\mathrm{CM}}}{2C_{\mathrm{y}}}} = 25\Omega. \tag{2.3}$$

In mains connected EUTs the C_{y} capacitors present a maximum capacitance value, for safety reasons [12]. This maximum capacitance turns out to be in the order of nF, to limit the flow of the common mode leakage current in the protective earth (PE) conductor. For this reason, (2.3) cannot be exploited in every filter design. Indeed, if the C_{y} limit value is reached, the only way to reduce the CM disturbance is to increase the L_{CM} value. This increases the quality factor of the system, thus the damping of the system should be addressed.

Once the CM filter is designed, it is possible to proceed with the design of the differential one. As for CM, the DM disturbance current is evaluated according to the power supply current shape. The DM current source is partitioned between the input capacitance impedance and the LISNs impedance, as shown in Fig. 2.3, and its spectrum can be evaluated according to Eq. 1.5.

The DM current source can be modeled as a current generator, whose waveform depends on the adopted modulation law. Its spectrum is denoted as $I_{\mathrm{EUT}}(s)$. The input capacitance impedance can be written as:

$$Z_{\mathrm{C_{in}}} = \frac{s^2 ESL \cdot C_{\mathrm{in}} + sESR \cdot C_{\mathrm{in}} + 1}{sC_{\mathrm{in}}}. \tag{2.4}$$

Since in general, for low frequencies, $Z_{\mathrm{C_{in}}} << Z_{\mathrm{LISN,DM}} = 100\,\Omega$ it is possible to derive a Thevenin equivalent circuit of the DM source, with a negligible series impedance. The Thevenin equivalent voltage is:

$$V_{\mathrm{DM,EUT}} = I_{\mathrm{EUT}} \cdot Z_{\mathrm{C_{in}}}, \tag{2.5}$$

which, therefore, can be approximated to the DM voltage drop on the LISNs equivalent DM impedance, i.e. $Z_{\mathrm{LISN,DM}} = 100\,\Omega$. If the DM spectrum exceeds the imposed limits, from the attenuation A_{DM} required at a certain frequency $f_{\mathrm{A,DM}}$ it is possible to evaluate the cutoff frequency of the DM second order LC filter:

$$f_{\mathrm{c,DM}} = f_{\mathrm{A,DM}}\sqrt{A_{\mathrm{DM}}}, \tag{2.6}$$

which can be expressed as:

$$f_{\mathrm{c,DM}} = \frac{1}{2\pi\sqrt{2L_{\mathrm{DM}}C_{\mathrm{x}}}}. \tag{2.7}$$

The filter quality factor Q, in order to avoid spectral amplification near the cutoff frequency is set equal to 1:

$$Q = \frac{Z_{\mathrm{LISN,DM}}}{Z_0} = 1, \tag{2.8}$$

where $Z_{\text{LISN,DM}}$ is equal to the LISN differential impedance, i.e. 100Ω, and

$$Z_0 = \sqrt{\frac{2L_{\text{DM}}}{C_{\text{x}}}}. \tag{2.9}$$

From these equations it can be drawn that:

$$\sqrt{\frac{2L_{\text{DM}}}{C_{\text{x}}}} = 100\Omega. \tag{2.10}$$

Also in this case, the DM filter component should be dimensioned according to the imposed standards. Indeed, the capacitor C_{x}, especially for mains connected devices, should respect additional requirement. C_{x} capacitors should be self-healing in order to avoid short circuit hazards [12]. The values of both inductor and capacitors can differ from what initially designed, increasing the quality factor of the filter.

For both CM and DM filtering, a possible solution to address the damping issue is to insert some additional passive elements to reduce the quality factor [13, 14]. Such additional elements are usually RL or RC networks placed in parallel to the elements of the LC filter, in order to avoid its resonance.

2.2 Active EMI filters

The passive filters have some disadvantages, since they are often bulky and heavy. In order to address this issue, in recent years some active filtering techniques have been investigated. Those filtering techniques are mainly based on the disruptive interference between the conducted EMI generated and a signal generated by the active filter, as can be seen in Fig. 2.5. Different approaches have been developed in literature, for both CM and DM emissions [15] or one single mode reduction [16, 17], especially for CM. The CM disturbance is sensed on the CM choke, reversed in polarity and summed at the power line terminals. This reduction technique requires high gain-bandwidth product amplifier, with high slew rate, since the EMI are often high dv/dt (or di/dt) waveforms.

Another approach to reduce the CM choke dimensions maintaining the filter effectiveness was proposed by Xu [18]. Such a technique consist in reducing the size of the CM choke using a negative impedance connected to a third winding, wounded on the choke iron core. This negative impedance is used to increase the CM and DM impedances. in order to increase the insertion loss. This technique allows the reduction of the magnetic component of the filter, but it gives good results only in the lower part of the spectrum, worsening the emissions in the higher frequency range.

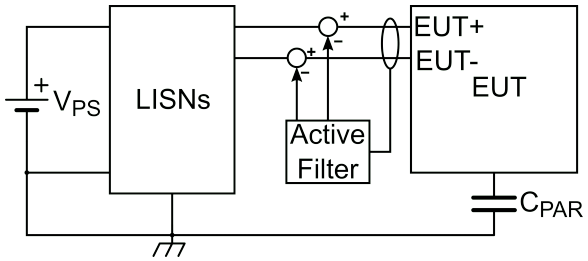

Figure 2.5: Active filter technique operating principle. The conducted EMI is sensed, negative amplified and summed at the power supply nodes.

2.3 Spread Spectrum Modulation

The use of hardware techniques to reduce the EMI has several disadvantages: the filter occupies a non negligible board area and EUT volume, it is heavy, expensive and it is not easily tunable. For this reason, the use of software techniques is preferable: they do not require additional components, they are more flexible than the hardware ones and they allow the designer to further reduce the EMI, if a filter has already been added and the EMC tests are not passed. Among these techniques, the Spread Spectrum Modulation (SSM) [19] is one of the most used by EMC designers.

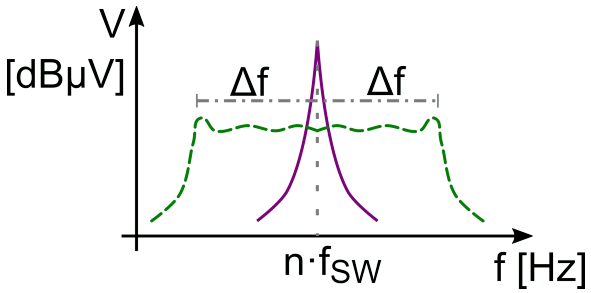

Figure 2.6: Spread Spectrum Modulation operating principle. In continuous line the n-th harmonic, before applying the SSM. In dashed line the same n-th harmonic after applying the SSM.

The spectrum generated by PWM in switching circuits is composed by narrow-band harmonics. The integral of such narrow band harmonics over their frequency band represents the energy of the disturbance at that frequency. If the switching frequency is varied over time, in a frequency range [f_{sw}- Δf, f_{sw}+ Δf], i.e. the Carson's band, the energy remains the same, but it is spread over a wider frequency range: it means that, for every harmonic, the peak level is reduced. In Fig. 2.6 this mechanism is shown. The modulation of the switching frequency can be expressed as [20]:

$$s(t) = A_0 \cos(2\pi(f_{\text{sw}}t + \Delta f \int_{-\infty}^{t} m(t)dt)), \tag{2.11}$$

where A_0 is the signal amplitude and $m(t)$ is the modulation waveform. Such waveform usually is chosen to spread the narrow band harmonic over a wide frequency range, with a flat response. The SSM modulation can be therefore classified according to the used modulation waveform. The SSM techniques can be classified in four groups [21]:

- Programmed PWM: the switching frequency is programmed *a priori* in order to obtain harmonic suppression;
- Periodic modulation: the switching frequency is varied periodically. Several modulation waveforms can be used, like triangular, sinusoidal, exponential, etc..
- Random modulation: the switching frequency is varied randomly, in a specific band, to spread the harmonic energy.
- Chaotic modulation: the PWM switching frequency is generated using a chaotic map, or a circuit [22].

Among these modulation approaches, the most simple to implement is the periodic modulation. Some disadvantages can be present, like the harmonic energy accumulation at the border of the Carson's band. This happens in particular for the modulation waveforms which present a non uniform derivative along their period, like the sine wave. In order to address this issue, generally the triangular waveform modulation is used [23], since it presents a uniform derivative, in module, over its period. The result of using SSM, with triangular modulation waveform is shown in Fig. 2.7. The random modulation [24, 25], instead, is the beast approach in spreading the EMI spectrum, since the imposed PWM frequencies are not time-correlated one another. However, this approach is more difficult to implement than the periodic modulation, since it requires an increased computational effort for the PWM controller.

The modulation depth Δf is designed in order to avoid the overlap of the spreading bands of two adjacent harmonics and both the modulation depth and the modulation frequency f_{m} are tuned looking at the EMI receiver filtering characteristics, in order to obtain the maximum allowable reduction. For this reason and since the interference energy remains unchanged, for many years this technique has been considered a way of cheating.

The SSM, however, presents some disadvantages. One of them is the voltage ripple generation on the output [20]. This ripple is generated at the modulation frequency f_{m}. Since it is a low frequency ripple, it is difficult to suppress, unless a large, low impedance filter capacitor is added to the output, or a feedback network able to compensate this ripple is designed.

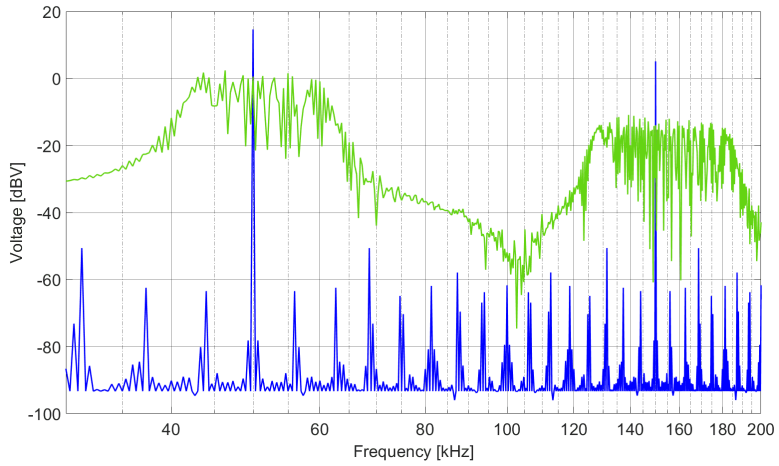

Figure 2.7: Spread Spectrum Modulation effect. In blue the original spectrum (narrow-band) and in green the spectrum after applying SSM.

2.4 Waveform shaping

As said in the previous section, the SSM technique does not reduce the energy of the emission, it only spreads the energy of each harmonic over a wider band. In order to reduce the EMI energy, other approaches have been developed in recent years. One of them, dealing mainly with CM emission reduction, is the output waveform shaping. Different approaches can be used: from the simpler ones, i.e. the reduction of the edges slew rate, to more complex techniques.

The approach proposed in [26] is based on the shaping of the output waveforms modulating the gate command signal. With this approach, the slew rate of the output waveform is limited and the output waveform shape is controlled limiting the second derivative of that voltage. In order to perform these operations, an *ad hoc* gate driver should be designed and implemented. The controller acquires the output voltage and current, and the gate current as feedback, and modulates the gate current in order to obtain the desired output voltage shape.

This technique, however, is difficult to implement and costly, since it requires a specific gate driver and a controller with at least three high speed ADC channels and three DAC channels.

For the reasons above, the research activity of this thesis is focused on the design of a new technique which allows the reduction of the EMI in a software way, with the addition of a simple and cheap sensing circuit.

Chapter 3

Analysis of the CM EMI in Switching Circuits

In this chapter, the generation of the conducted EMI in power switching circuits is presented. In particular, the common mode component of the conducted emission is analyzed in details. The reference circuit for these analyses is a power inverter, like the one shown in Fig. 3.1. The full-bridge inverter is connected to a generic load, and the DC voltage of the power supply, V_{PS}, is provided through two LISNs [3]. For these analyses, the inverter is supplied directly by a DC voltage source, i.e. a battery, but the same conclusion can be drawn for inverters supplied by the mains, where the DC voltage is provided by a rectifier circuit.

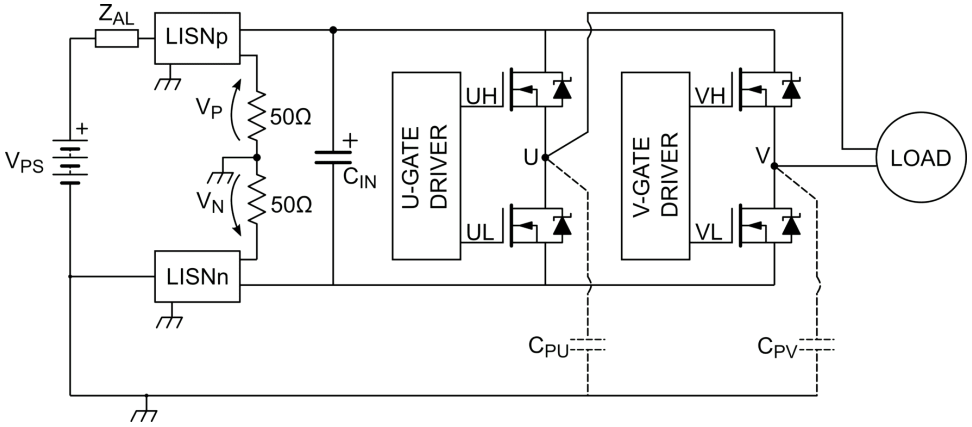

Figure 3.1: Full-bridge inverter circuit.

Focusing on the inverter, each leg is composed of two n-MOS switches, whose gate terminals (UH, UL, ...) are controlled by a dual input-dual output gate driver. The output nodes of the inverter, U and V, provide the voltage waveforms to the load.

The inverter can be driven with different PWM strategies, but, as seen in Chapter 1, the bipolar PWM is useful to reduce the conducted common mode emission. The output waveforms and the respective average voltages are reported in Fig. 3.2.

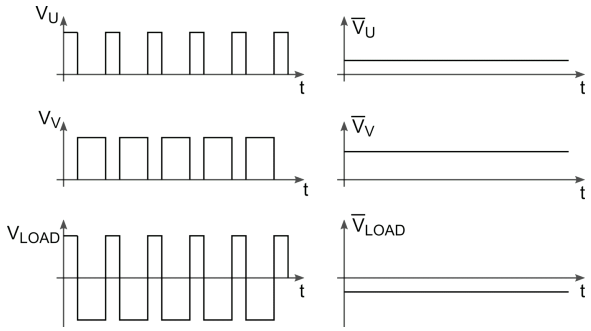

Figure 3.2: Bipolar PWM: output waveforms and voltage on the load ($V_{\mathrm{LOAD}} = V_{\mathrm{U}} - V_{\mathrm{V}}$).

With this PWM strategy, the higher voltage is obtained using a duty cycle D greater than 0.5, while the other lower one is obtained driving the other leg with complementary duty cycle $(1 - D) < 0.5$. Therefore, the voltage on the load, $V_{\mathrm{LOAD}} = V_{\mathrm{U}} - V_{\mathrm{V}}$, could reach values from $-V_{\mathrm{PS}}$ to V_{PS}. In the following section, the contributions to the CM conducted emission are analyzed.

3.1 Contributions to the CM conducted emission

As seen in Chapter 1, the CM emissions are generated by the current flowing in the parasitic capacitances of the EUT towards the reference plane. Considering as example the aforementioned inverter, using the bipolar PWM strategy, whose waveform is shown in Fig. 3.3, the pulsed current injected in the parasitic capacitance referred to an active output is recovered by the capacitance referred to the complementary output, ideally nulling the CM conducted emissions.

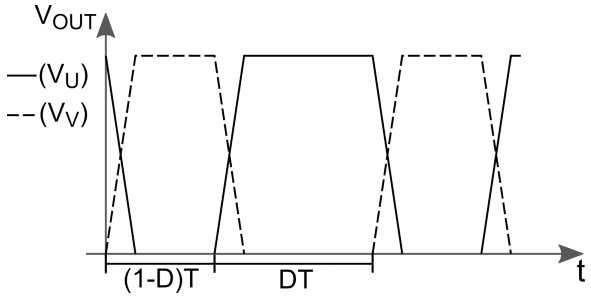

Figure 3.3: Bipolar PWM output waveforms.

This assumption is valid if three conditions are satisfied:

- The parasitic capacitances mismatch is null;
- The output waveforms rise time is equal to the fall time;
- The outputs are perfectly complementary, i.e. there is no phase shift between the waveforms rising and falling edges.

If these conditions are not verified, some current flows back to the LISNs, generating conducted CM emissions. The issues introduced by these non idealities have been sketched out in some works in literature, and they have been partially solved. In [27] the phase shift between the output voltages has been reduced tuning automatically the gating signals. This has been obtained measuring the common mode current using a transformer on the power line. Since this current is composed by narrow spikes, it should be over-sampled in order to obtain useful information on the emission level. The compensation algorithm is therefore slow and it is not able to promptly reduce a sudden variation of the phase shift. Moreover, that technique was able to reduce by only 10 dB the CM emission level. Another attempt in reducing the CM EMI of a full-bridge inverter was proposed by Chang *et al.* [28]. In this paper, a genetic algorithm has been used for tuning the gating commands, in order to reduce the total harmonic distortion of the inverter output voltage. However it is not clear how the output voltage harmonic distortion has been measured, to be given as input to the genetic algorithm. Moreover, the spectra of the produced emission, in order to evaluate the technique effectiveness in reducing the CM EMI, were not provided. The same issue, deriving from the phase shift between the signals, has been sketched out also in other fields, as the communication buses one. In [29], the controller area network (CAN) bus emissions have been modeled. In particular, the CM contribution derives from the asymmetries between the differential signals CAN_H and CAN_L, which are not complementary one another.

Recently, another solution to mitigate the CM emission of three-phase inverters has been proposed by Watase *et al.* [30]. It is based on the synchronization of two three phase inverters, modulated by unipolar PWM, driving two three-phase motors. The two motors are driven oppositely, i.e. the sinusoidal waveforms of the control are shifted by 180° between the two inverters. This means that the phases of the two inverters are complementary one another, if no phase shift is present. Indeed, in this paper the phase shift issue was not discussed. Moreover, this method can be employed only to those systems in which two motors are needed or when double wounded motors should be driven. Another method applicable to three phase inverter has been proposed by Cordes and Klotz [31], optimizing the synchronization of the output transitions. However, also in this case, the contribution of the misalignment of the output edges has not been taken into account.

In order to address the CM EMI generation in bipolar switched circuit, an analysis of the sources of the CM should be performed. In the next sections, the three aforementioned contributions are studied individually.

3.2 Analytical model of CM conducted EMI

If only the CM emissions are considered, the equivalent circuit of the inverter connected to the LISNs is shown in Fig. 3.4. For CM analysis, the two power supply nodes are connected together and the output is modeled as a trapezoidal waveform voltage source. These generators, V_{U} and V_{V} drive the output parasitic capacitance C_{PU} and C_{PV}, respectively. The LISNs are modeled, as seen in Chapter 1, as an impedance $Z_{\mathrm{LISN}} = 25\,\Omega$.

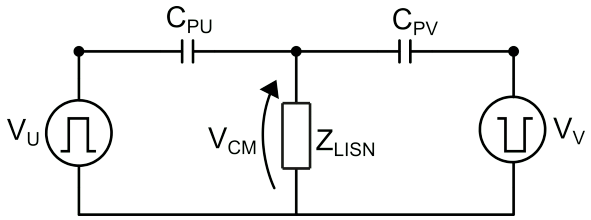

Figure 3.4: Common mode equivalent circuit.

In order to simplify the following analyses, the duty cycle D is fixed to 0.5. The same results can be drawn with other values of D.

The Fourier series of the outputs trapezoidal signal is expressed as:

$$v(t) = \sum_{n=-\infty}^{\infty} V(jn\omega_0) e^{jn\omega_0 t}. \tag{3.1}$$

The term $V(jn\omega_0)$, for the trapezoidal signal is expressed as follows:

$$\begin{aligned} V(jn\omega_0) = {} & \frac{V_0}{2} \frac{\sin(\frac{1}{4}n\omega_0 T)}{\frac{1}{4}n\omega_0 T} \frac{\sin(\frac{1}{2}n\omega_0 t_{\mathrm{r}})}{\frac{1}{2}n\omega_0 t_{\mathrm{r}}} \cdot \\ \cdot e^{-j0.5n\omega_0(\frac{T}{2}+t_{\mathrm{r}})} & \frac{\psi^2 + (2\alpha + \frac{k}{V_0}\omega_{\mathrm{r}})\psi + \alpha^2 + \omega_{\mathrm{r}}^2}{\psi^2 + 2\alpha\psi + \alpha^2 + \omega_{\mathrm{r}}^2}, \end{aligned} \tag{3.2}$$

where V_0 is the signal amplitude at nodes U and V, $\psi = jn\omega_0$, ω_0 is the trapezoidal wave angular frequency, i.e. the PWM switching frequency, t_{r} the rising/falling time; the ringing is characterized by its angular frequency ω_{r}, its amplitude k and its damping coefficient α [5]. In this complete model of the $V(jn\omega_0)$, also the ringing contribution is reported, which can be found to the last fraction of (3.2). In the following analyses this term is neglected, considering only the trapezoidal

waveform contribution:

$$V(jn\omega_0) = \frac{V_0}{2} \frac{\sin(\frac{1}{4}n\omega_0 T)}{\frac{1}{4}n\omega_0 T} \frac{\sin(\frac{1}{2}n\omega_0 t_r)}{\frac{1}{2}n\omega_0 t_r} \cdot e^{-j0.5n\omega_0(\frac{T}{2}+t_r)}. \tag{3.3}$$

The spectrum of $V(jn\omega_0)$ is reported in Fig. 3.5.

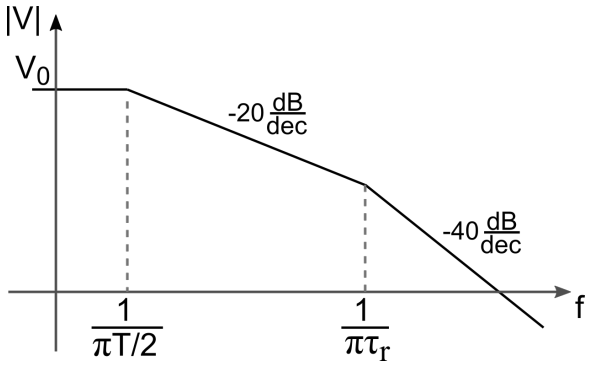

Figure 3.5: Two-sided spectrum of $V(jn\omega_0)$.

Since the two voltages V_U and V_V are complementary, they can be represented as:

$$V_U(jn\omega_0) = V(jn\omega_0), \tag{3.4}$$

$$V_V(jn\omega_0) = V(jn\omega_0) \cdot e^{-jn\omega_0(\frac{T}{2})} \tag{3.5}$$

From these Fourier transforms of the sources, it is possible to compute singularly the effect of the non-ideality presented in the previous Section.

3.2.1 Parasitic capacitances mismatch

Looking at Fig. 3.1, the two parasitic capacitances in which the CM disturbance flows are C_{PU} and C_{PV}. With an accurate layout design it is possible to minimize the value of these capacitance and to make the two values almost equal. However, slight differences between these two capacitances could be present, giving rise to CM emission. Looking at the circuit of Fig. 3.4, the voltage at the LISN can be computed as:

$$V_{CM} = V_U \frac{Z_{Cpv} // Z_{LISN}}{Z_{Cpu} + Z_{Cpv} // Z_{LISN}} + V_V \frac{Z_{Cpu} // Z_{LISN}}{Z_{Cpv} + Z_{Cpu} // Z_{LISN}}, \tag{3.6}$$

where $Z_{Cpu} = 1/(jn\omega_0 C_{PU})$ and $Z_{Cpv} = 1/(jn\omega_0 C_{PV})$. If the duty cycle D is equal to 0.5, since the circuit is an high-pass filter, Eq. (3.6) can be rewritten as:

$$V_{CM} = V(jn\omega_0) \left(\frac{Z_{Cpv} // Z_{LISN}}{Z_{Cpu} + Z_{Cpv} // Z_{LISN}} - \frac{Z_{Cpu} // Z_{LISN}}{Z_{Cpv} + Z_{Cpu} // Z_{LISN}} \right) \tag{3.7}$$

It is possible to define two parameters for evaluating the mismatch effect. The first is the average capacitance, defined as:

$$C_{\mathrm{p,avg}} = \frac{C_{\mathrm{PU}} + C_{\mathrm{PV}}}{2}, \tag{3.8}$$

and the mismatch index as:

$$\delta C_{\mathrm{p}} = \frac{|\Delta C_{\mathrm{p}}|}{C_{\mathrm{p,avg}}}, \tag{3.9}$$

where $\Delta C_{\mathrm{p}} = C_{\mathrm{PU}} - C_{\mathrm{PV}}$. With these two parameters it is possible to evaluate the contribution of the capacitance mismatch on the CM conducted emission, rewriting Eq. (3.7).

$$V_{\mathrm{CM}} = V(jn\omega_0)\left(\frac{jn\omega_0 Z_{\mathrm{LISN}} C_{\mathrm{p,avg}}(1+\delta C_{\mathrm{p}})}{1+2jn\omega_0 Z_{\mathrm{LISN}} C_{\mathrm{p,avg}}} - \frac{jn\omega_0 Z_{\mathrm{LISN}} C_{\mathrm{p,avg}}(1+\delta C_{\mathrm{p}})}{1+2jn\omega_0 Z_{\mathrm{LISN}} C_{\mathrm{p,avg}}}\right) = V(jn\omega_0)\frac{jn\omega_0 Z_{\mathrm{LISN}} 2\delta C_{\mathrm{p}}}{1+2jn\omega_0 Z_{\mathrm{LISN}} C_{\mathrm{p,avg}}}. \tag{3.10}$$

This model shows that a variation in δC_{p} acts proportionally on the conducted emission magnitude. The emissions have been evaluated using three values of the mismatch δC_{p}, in the range 0.1-1. The values used to perform the evaluation are: $V_{\mathrm{PS}} = 12\,\mathrm{V}$, $T = 20\,\mu\mathrm{s}$, $t_{\mathrm{r,f}} = 20\mathrm{ns}$, $C_{\mathrm{p,avg}} = 10\,\mathrm{pF}$ and $Z_{\mathrm{LISN}} = 25\,\Omega$. The result is shown in Fig. 3.6.

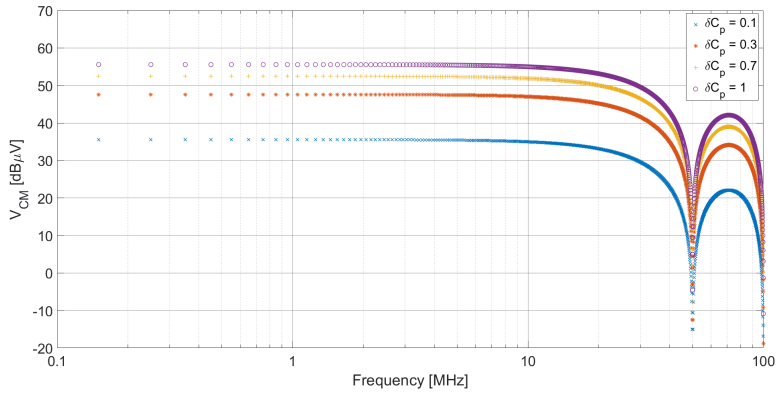

Figure 3.6: Parasitic capacitance mismatch effect on CM emission spectrum.

3.2.2 Transition time mismatch

A second contribution on the CM emission would be due to the transition times mismatch. If the output waveform rising time differs from the falling one, and the

other two conditions are verified, the CM emission can be generated. The Fourier series of a trapezoidal waveform, with $t_\mathrm{r} \neq t_\mathrm{f}$, is expressed as[5]:

$$V(jn\omega_0) = -j\frac{V_0}{2\pi n} \cdot e^{-jn\omega_0(DT+t_\mathrm{r})/2} \cdot \left(\frac{\sin(0.5n\omega_0 t_\mathrm{r})}{0.5n\omega_0 t_\mathrm{r}} e^{jn\omega_0 DT/2} - \frac{\sin(0.5n\omega_0 t_\mathrm{f})}{0.5n\omega_0 t_\mathrm{f}} e^{-jn\omega_0 DT/2} \right). \tag{3.11}$$

This expression, if the transition times are different, cannot be expressed as a product of terms. The two voltage sources, in order to be complementary, can be expressed as:

$$V_\mathrm{U}(jn\omega_0) = V(jn\omega_0), \tag{3.12}$$

$$V_\mathrm{V}(jn\omega_0) = V(jn\omega_0) \cdot e^{-jn\omega_0(\frac{T}{2})} \tag{3.13}$$

If the two parasitic capacitance are equal, the common mode voltage at the LISNs is given by:

$$V_\mathrm{CM}(jn\omega_0) = V(jn\omega_0) \cdot (1 + e^{-jn\omega_0(\frac{T}{2})}) \cdot \frac{jn\omega_0 Z_\mathrm{LISN} C_\mathrm{P}}{1 + 2jn\omega_0 Z_\mathrm{LISN} C_\mathrm{P}} \tag{3.14}$$

If the two transition time are equal, the voltage V_CM would be null. If the transition times are different, it is possible to define an average transition time as:

$$t_\mathrm{t,avg} = \frac{t_\mathrm{r} + t_\mathrm{f}}{2}, \tag{3.15}$$

and the mismatch as:

$$\delta t_\mathrm{t} = \frac{|\Delta t_\mathrm{t}|}{t_\mathrm{t,avg}} \tag{3.16}$$

where $\Delta t_\mathrm{t} = t_\mathrm{r} - t_\mathrm{f}$.

Considering a variation of δt_t between 0.1 and 1 it is possible to derive the spectra in Fig. 3.7. The numeric values are derived with $V_\mathrm{PS} = 12\,\mathrm{V}$, $T = 20\,\mu\mathrm{s}$, $t_\mathrm{t,avg} = 20\,\mathrm{ns}$, $C_\mathrm{P} = 10\,\mathrm{pF}$ and $Z_\mathrm{LISN} = 25\,\Omega$.

From these spectra it is possible to see that also the transition time mismatch acts proportionally for low frequencies. Its contribution on CM EMI, in particular for low frequency, is less important with respect to the capacitance mismatch.

3.2.3 Output waveforms not complementary

The last contribution on CM emissions when a bipolar PWM is used, is the delay present between the ouput waveforms. For this analysis, assume that the capacitance and transition time mismatches are null. In general, the output waveforms

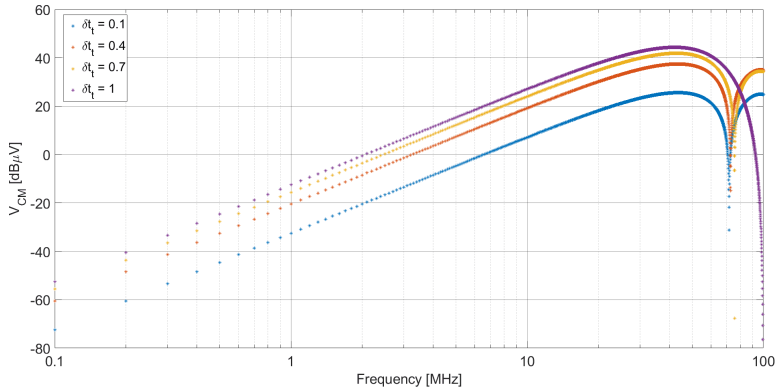

Figure 3.7: Rising-falling time mismatch effect on CM emission spectrum.

are not complementary one another since some delay due to the propagation of the control signals from the microcontroller to the MOSFETs gate can be present.

From this considerations, it is possible to derive an analytical model for the CM emissions. As seen before, the voltage generators at U and V nodes, when the duty cycle is equal to 0.5, can be expressed as:

$$V_{\mathrm{U}}(jn\omega_0) = V(jn\omega_0) \tag{3.17}$$

$$V_{\mathrm{V}}(jn\omega_0) = V(jn\omega_0) \cdot e^{-jn\omega_0(\frac{T}{2}+\tau_{\mathrm{d}})} \tag{3.18}$$

where $V(jn\omega_0)$ is the Fourier series of the trapezoidal waveform, T is the waveform period and τ_{d} is the output delay, as presented in the previous section and shown in Fig. 3.8. For the following analyses, the same results can be obtained with different valued of duty cycle. Indeed, if a generic duty cycle D is used:

$$V_{\mathrm{U}}(jn\omega_0) = DV_0 \frac{\sin(\frac{1}{2}n\omega_0 DT)}{\frac{1}{2}n\omega_0 DT} \frac{\sin(\frac{1}{2}n\omega_0 t_{\mathrm{r}})}{\frac{1}{2}n\omega_0 t_{\mathrm{r}}} \cdot e^{-j0.5n\omega_0(DT+t_{\mathrm{r}})}. \tag{3.19}$$

$$\begin{aligned} V_{\mathrm{V}}(jn\omega_0) = (1-D)V_0 \frac{\sin(\frac{1}{2}n\omega_0(1-D)T)}{\frac{1}{2}n\omega_0(1-D)T} \frac{\sin(\frac{1}{2}n\omega_0 t_{\mathrm{r}})}{\frac{1}{2}n\omega_0 t_{\mathrm{r}}} \cdot \\ \cdot e^{-j0.5n\omega_0((1-D)T+t_{\mathrm{r}})} \cdot e^{-jn\omega_0(DT+\tau_{\mathrm{d}})}. \end{aligned} \tag{3.20}$$

Since $\sin(\frac{1}{2}n\omega_0 T) = 0$, (3.20) can be rewritten simplifying the terms $(1-D)$ and multiplying both numerator and denominator by D:

$$\begin{aligned} V_{\mathrm{V}}(jn\omega_0) = DV_0 \frac{\sin(\frac{1}{2}n\omega_0 DT)}{\frac{1}{2}n\omega_0 DT} \frac{\sin(\frac{1}{2}n\omega_0 t_{\mathrm{r}})}{\frac{1}{2}n\omega_0 t_{\mathrm{r}}} \cdot \\ \cdot e^{-j0.5n\omega_0((1-D)T+t_{\mathrm{r}})} \cdot e^{-jn\omega_0(DT+\tau_{\mathrm{d}})}. \end{aligned} \tag{3.21}$$

Looking at the exponential terms, they can be rewritten as:

$$V_{\mathrm{V}}(jn\omega_0) = DV_0 \frac{\sin(\frac{1}{2}n\omega_0 DT)}{\frac{1}{2}n\omega_0 DT} \frac{\sin(\frac{1}{2}n\omega_0 t_{\mathrm{r}})}{\frac{1}{2}n\omega_0 t_{\mathrm{r}}} \cdot \\ \cdot e^{-j0.5n\omega_0(DT+t_{\mathrm{r}})} \cdot e^{-jn\omega_0(T/2+\tau_{\mathrm{d}})}, \tag{3.22}$$

obtaining the same relation written in (3.18).

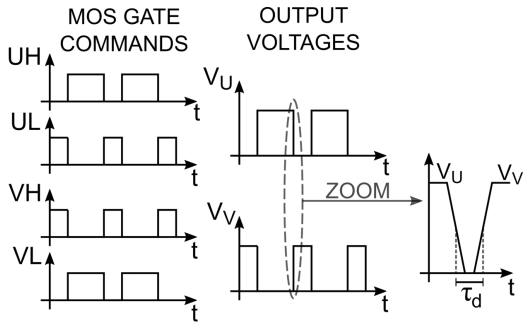

Figure 3.8: Gate signals for the general duty cycle case, τ_{d} delay definition.

The voltage at the LISNs CM output $V_{\mathrm{CM}}(jn\omega_0)$ can be evaluated with the superposition of the effect of V_{U} and V_{V}:

$$V_{\mathrm{CM}}(jn\omega_0) = V(jn\omega_0) \cdot D(jn\omega_0) \cdot H(jn\omega_0) = \\ V(jn\omega_0) \cdot (1 + e^{-jn\omega_0(\frac{T}{2}+\tau_d)}) \cdot \frac{jn\omega_0 RC}{1 + 2jn\omega_0 RC} \tag{3.23}$$

where $C_{\mathrm{PU}} = C_{\mathrm{PV}} = C$ and $R = Z_{\mathrm{LISN}}$. It is possible to evaluate the contribution of τ_{d} on the CM emission, computing the magnitude of $D(jn\omega_0) = (1 + e^{-jn\omega_0(\frac{T}{2}+\tau_{\mathrm{d}})})$:

$$|D(jn\omega_0)| = |(1 + e^{-jn\omega_0(\frac{T}{2}+\tau_{\mathrm{d}})})| = \sqrt{2 - 2\cos(n\omega_0\tau_{\mathrm{d}})} \tag{3.24}$$

This term present a maximum magnitude equal to 2. When τ_d is equal to 0, $D(jn\omega_0) = 0$ and $V_{\mathrm{CM}}(jn\omega_0)$ is ideally nulled. Actually, it does not occur, because of other common mode contributions, like ringing and asymmetries of the output voltage waveforms. The cosine contribution under the square root can be approximated, for low frequencies, with its Taylor expansion. In this range the envelope of $|D(jn\omega_0)|$ has a slope of +20dB/dec, while for higher frequencies it gives a constant contribution of 6 dB.

The $|V_{\mathrm{CM}}(jn\omega_0)|$ Bode diagram is shown in Fig. 3.9. The location of poles and zeros may change according to the waveform parameters values, i.e. rise-falling time, duty cycle, τ_{d}, etc.

Summarizing, if the delay τ_{d} is reduced, the low frequency spectrum of the CM emissions is lowered. In Fig. 3.10 the spectral envelopes derived from the analytical

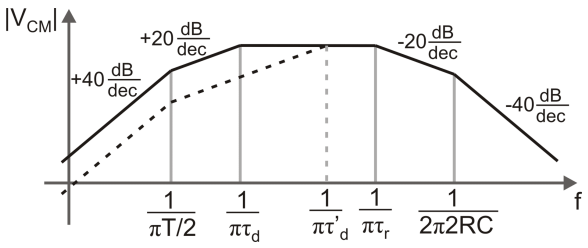

Figure 3.9: CM voltage spectrum. The continuous line is derived with a time delay τ_{d} present between the output waveforms. When the delay is reduced from τ_{d} to τ'_{d} the spectrum is modified as the dashed line indicates.

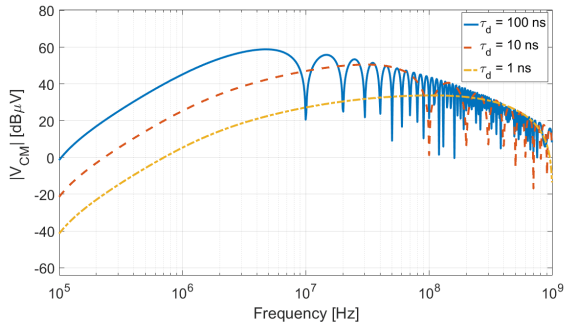

Figure 3.10: Spectral envelopes derived with the proposed analytical model, for different values of τ_{d}.

Table 3.1: Model Parameters

Parameter	**Value**
V_0	12 V
T	20 μs
D	0.5
t_{r}	10 ns
C	6 pF

model for three values of τ_{d} is shown. In Tab. 3.1 are reported the parameter values used to compute the spectra.

In Fig. 3.10 the CM emission spectrum is shown for τ_{d}=100 ns (continuous line), τ_{d}=10 ns (dashed line) and τ_{d}=1 ns (dashed-dotted line). The value of τ_{d} was not set to 0 ns, otherwise V_{CM} voltage would be nulled, as analyzed before. The fixed poles in this simulation are $f_{\mathrm{P1}} = 1/(\pi T/2) = 31.8\,\mathrm{kHz}$, $f_{\mathrm{P3}} = 1/(\pi\tau_{\mathrm{r}}) = 12.7\,\mathrm{MHz}$ and $f_{\mathrm{P4}} = 1/(2\pi 2RC) = 318\,\mathrm{MHz}$. The pole $f_{\mathrm{P2}} = 1/(\pi\tau_{\mathrm{d}})$ instead moves in frequency when τ_{d} changes. Respectively the pole frequencies for the three above mentioned cases are 3.18 MHz, 31.8 MHz and 318 MHz. In the frequency range 1-30 MHz it is evident that the CM emission spectrum is reduced, because of the variation of the

misalignment between the two active legs.

It is important to analyze the source of the delay τ_{d}, in order to evaluate the main responsible of its generation and address this issue. The delay can be due to the following causes:

- PCB traces length mismatch;
- Gate resistance mismatch;
- Gate driver input-output delay mismatch.

The mismatch in the length of the PCB traces carrying the command signals from the microcontroller to the gate drivers can be a cause of output delay. Considering a standard FR4 PCB, with relative permittivity ε_{r} equal to 4.5, the signal speed along the trace can be computed as:

$$v_{\mathrm{f}} = \frac{c}{\sqrt{\varepsilon_{\mathrm{r}}}} = \frac{3 \cdot 10^8\,\mathrm{m/s}}{\sqrt{4.5}} = 141.4 \cdot 10^6\,\mathrm{m/s} \tag{3.25}$$

where c is the speed of light. If a mismatch $\Delta L = 1\,\mathrm{cm}$ is present between the traces carrying the signal to two different gate drivers, the output delay τ_{d} would be equal to:

$$\tau_d = \frac{\Delta L}{v_{\mathrm{f}}} = \frac{1 \cdot 10^{-2}\,\mathrm{m}}{141.4 \cdot 10^6\,\mathrm{m/s}} = 71\,\mathrm{ps} \tag{3.26}$$

The resistances placed in series to the gate of the transistors are used to limit oscillations on the gate command signal. The mismatch between such resistors, referred to two different legs can introduce an output delay. If the MOS is modeled, looking into the gate terminal as its C_{GS} capacitance, and supposing that this capacitance is equal for all the MOSFET present in the inverter, considering an absolute tolerance of the gate resistors ΔR, the delay can be computed as:

$$\tau_d = \ln(10) C_{\mathrm{GS}} \Delta R. \tag{3.27}$$

Therefore, supposing that the resistor tolerance is 5% and the gate resistor values are equal to $3.3\,\Omega$ and C_{GS}=2 nF, the resulting worst case τ_{d} is equal to 760 ps.

Looking now at the third delay contribution, the commercial gate drivers are characterized by an input-output delay which could vary from tens of nanoseconds to hundred of nanoseconds. Using as example the gate driver LM5102 [32] produced by Texas Instruments and used in the following design, using two equal $10\,\mathrm{k}\Omega$ resistances for R_{T1} and R_{T2}, the rising edge propagation delay can vary from 75 ns to 150 ns, and the falling edge propagation time can vary from 27 ns to 56 ns.

It is possible to conclude that the main contribution to the output delay τ_{d} is due to the mismatch in the propagation delay of the gate drivers. This delay is casual and it is hard to compensate *a priori* during the inverter design process.

It is worth underlining that in the previous analysis the ringing contribution and the asymmetries between the output waveforms have not been taken into account.

3.3 Influence of the load parasitics

The parasitics of the load can influence the spectra of the common mode emissions. In particular, the load parasitic capacitances present between the load terminals and its chassis can influence the magnitude of the CM conducted EMI. Indeed, from Eq. (3.23), the increment of the parasitic capacitance C causes the shift of the pole $f_{P4} = 1/(2\pi 2RC)$ to lower frequencies, giving an increment of the spectra magnitude down to the new pole frequency. This behavior is shown in Fig. 3.11.

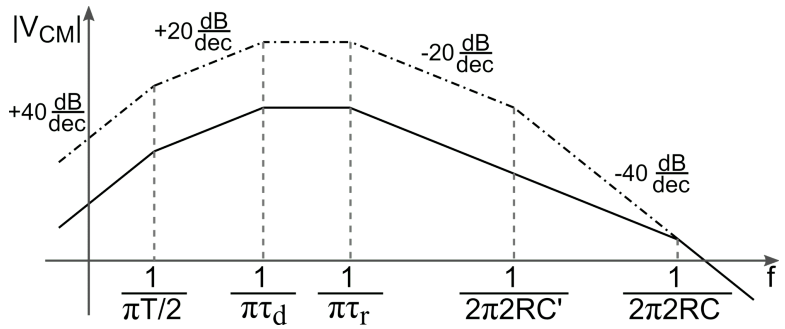

Figure 3.11: Spectral envelope with different values of parasitic capacitance. When the parasitic capacitance is incremented from C to C', the spectrum is increased as the dashed-dotted line indicates.

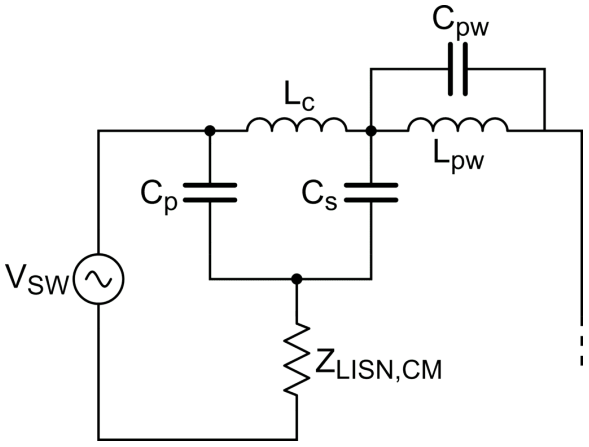

Figure 3.12: CM propagation path considering the load parasitics.

In Appendix B, the characterization of a possible load is presented. The circuit that models the CM propagation path is shown in Fig. 3.12.The capacitances C_s are

part of the propagation path of the common mode disturbance. Also the inductance of the cables, L_c, influences the CM EMI: indeed, after the resonance frequencies given by the couples $C_s - L_c$ (series) and $C_p - L_c$ (parallel) the conducted emissions spectra tends to the one in which only C_p is considered. The cable inductance, therefore, filters the CM component flowing into the parasitic capacitances of the load.

In the following Section the analytical considerations made before are compared with SPICE simulations.

3.4 Simulations

In order to verify the analyses drawn in the previous Section, a simulation of the system has been carried out. The simulation was performed with Spice, and the simulated schematic is shown in Fig. 3.13.

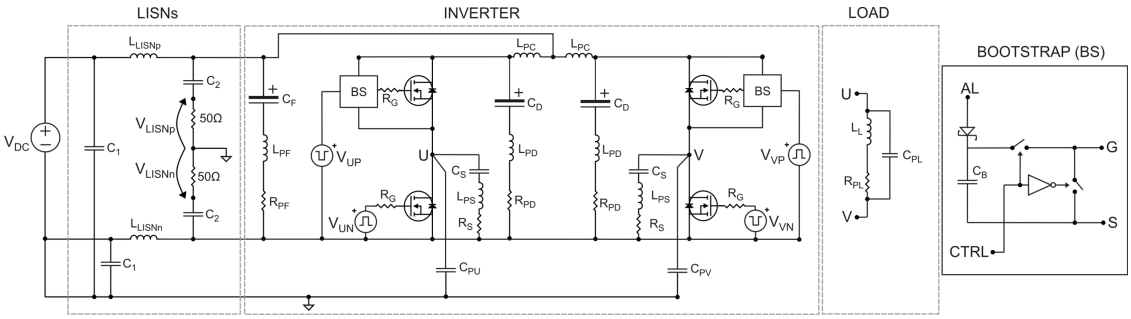

Figure 3.13: Simulated schematic

The values for the parameters presented in Fig. 3.13 are reported in Tab. 3.2. The switching frequency of the inverter $f_{SW} = 1/T$ is equal, as in the analysis carried out before, to 50 kHz.

The CM voltage has been computed as:

$$V_{CM} = \frac{V_{LISNp} + V_{LISNn}}{2} \tag{3.28}$$

and a Fast Fourier Transform (FFT) has been performed on the sampled data. The simulations have been carried out considering two cases: the first with $\tau_d \approx 100\,\text{ns}$ and the second with compensated delay, $\tau_d \approx 5\,\text{ns}$. The simulations have been compared with the analytical model derived in the previous Section. The results are shown in Fig. 3.14 and in Fig. 3.15.

From the comparison the performed analysis has been verified. The analytical model approximate well the behavior of the spectra, confirming that if the delay τ_d is compensated, the conducted emissions are reduced.

Table 3.2: Simulation parameters

Parameter	**Value**	**Parameter**	**Value**
V_{PS}	12 V	C_B	47 nF
L_{LISN}	5 μH	C_1	1 μF
C_2	100 nF	C_F	4700 μF
L_{PF}	20 nH	R_{PF}	60 mΩ
R_G	3.3 Ω	C_D	10 μF
L_{PD}	10 nH	R_{PD}	60 mΩ
$C_{PU,PV}$	6 pF	L_L	695 μH
C_{PL}	30 pF	R_{PL}	60 mΩ
R_S	3.9 Ω	C_S	4.7 nF
L_{PS}	2 nH	L_{PC}	100 nH

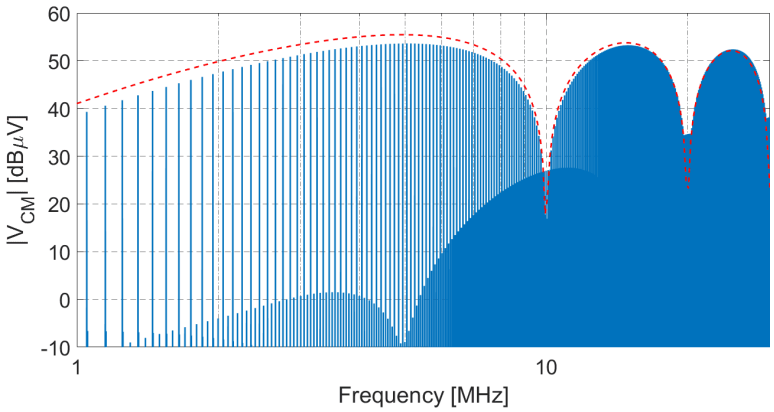

Figure 3.14: Comparison between analytical model and Spice simulation for $\tau_d \approx 100$ ns.

With respect on the previous works, [27, 28, 30, 31], a comprehensive model of the common mode emissions, and in particular the analytical model of the phase delay influence on the CM emissions, has been derived and confirmed by simulations.

3.4.1 Comparison with Spread Spectrum Modulation

The delay compensation technique, to reduce the CM conducted emissions, can be compared with SSM, which has been presented in 2.3. In order to avoid frequency accumulation, the modulation waveform is triangular, with modulation frequency $f_{SSM} = 1/T_{SSM} = 625$ Hz and modulation dept equal to 20%, i.e., since the inverter switching frequency is $f_{SW} = 50$ kHz, $\Delta f = 10$ kHz. The modulation

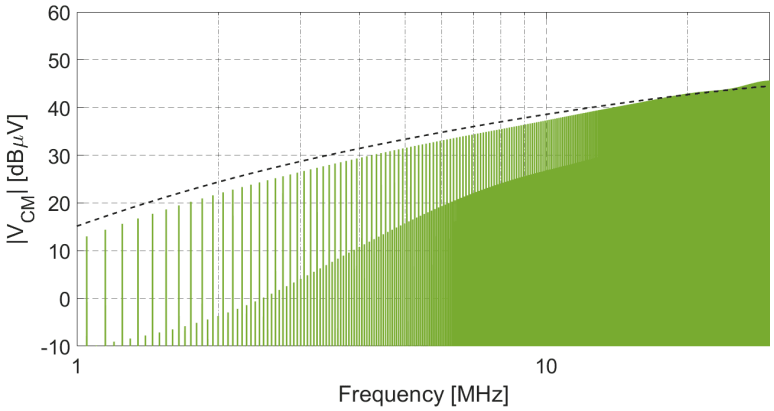

Figure 3.15: Comparison between analytical model and Spice simulation for $\tau_d \approx 5\,ns$.

index resulting from this choice of parameters is $m = \Delta f \cdot T_{SSM} = 16$ [19]. The modulation waveform $m(t)$ is reported in Fig. 3.16.

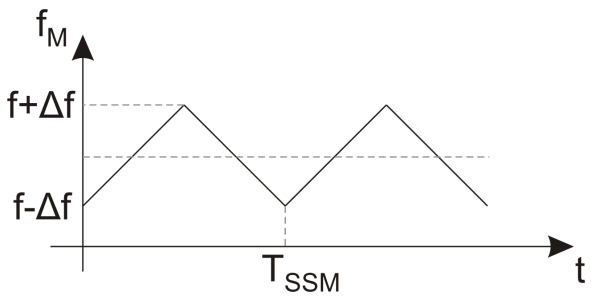

Figure 3.16: Spread spectrum modulation. Modulation waveform.

The resulting spectrum from this simulation, compared with the spectra derived with $\tau_d \approx 100\,ns$ and $\tau_d \approx 1\,ns$, is reported in Fig. 3.17.

From the simulation, it can be seen that the proposed technique reduces the CM emission 10 dB more than SSM up to 24 MHz, with the aligning accuracy that can be reached by commercial microcontrollers. Over this frequency the two reduction techniques show similar performances. Since the working principles of SSM and delay compensation are independent, the two techniques can work at the same time, further reducing the CM emission generated. Applying the two techniques together would mean that the harmonics of the red spectrum in Fig. 3.17 are spread over the SSM Carson's bandwidth, reducing their peak value, when the spectral energy has already been minimized by the delay compensation technique.

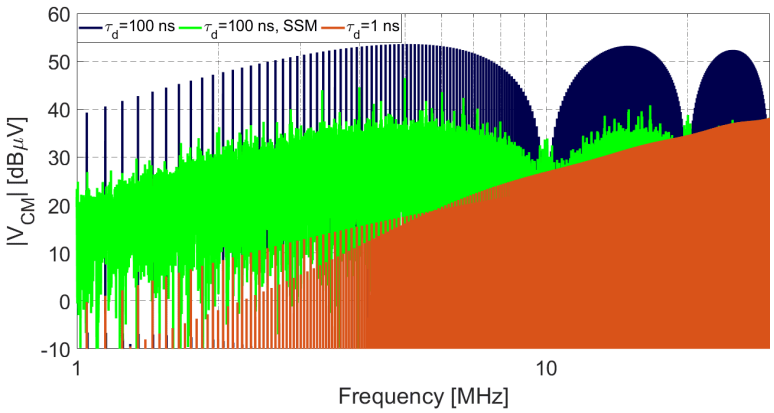

Figure 3.17: Comparison of the two software EMI reduction techniques. In blue the reference spectrum, obtained with $\tau_d \approx 100\,ns$, in green the SSM in applied and in red τ_d is compensated to be approximately equal to 1 ns.

3.5 Delay compensation technique

In order to obtain the output waveforms complementary one another, it is necessary to act on the PWM parameters of duty cycle and phase. In order to simplify the procedure, one leg is identified as Master and the remaining as Slave. The Master's phase parameter is set to be null, and its duty cycle is computed by the control. The Slave's phase and duty cycle parameters are set to obtain an output waveforms complementary to the Master's one, as defined in Fig. 3.18.

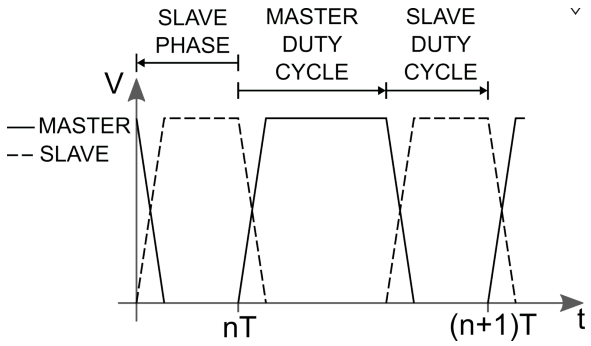

Figure 3.18: PWM parameters.

As explained before, the gating signals are affected by an unwanted time delay, τ_d. In general, considering the two switching events present in a PWM period, the delay present in the first transition can be different to the one referred to the second transition, as shown in Fig. 3.19. In order to compensate such delays, the compensation technique acts only on the Slave's PWM parameters. Therefore, a part of the delay is compensated adjusting the Slave's phase, while the residual delay is compensated acting on the Slave's duty cycle.

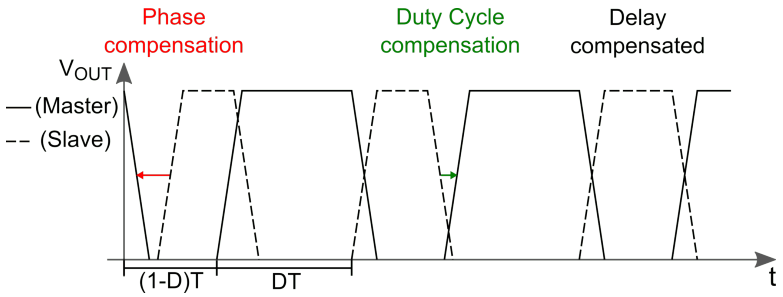

Figure 3.19: Compensation of the delay τ_d.

According to the previous parameter definition, it is possible to obtain a truth table that summarizes the actions to be performed in order to compensate the delay, as shown in Tab. 3.3. it is possible to distinguish between four cases according to the transition, i.e Master rising-Slave falling or vice versa, and the point in which the two waveforms meet: the outputs are overlapping high if this point is above one half the output voltage swing, or overlapping low if this point in under it.

Table 3.3: Delay Compensation Truth Table

	Outputs Overlapping High	**Outputs Overlapping Low**
Master rising	Decrease	Increase
Slave falling	Duty Cycle	Duty Cycle
Master falling	Decrease	Increase
Slave rising	Phase	Phase

In order to verify the effectiveness of the proposed technique in reducing the CM EMI, some preliminary measurements have been performed.

3.6 Preliminary measurements

Since the proposed technique can be applied to all the switching circuits in which a bipolar PWM is used, in order to evaluate its effectiveness, a three-phase inverter, used to drive a 350 W, 12 V BLDC motor has been designed and prototyped [33]. Such an inverter is made of three legs, each one composed of two n-MOS transistors driven by a dual input-dual output gate driver. The BLDC motors are driven, as explained in Appendix A, by trapezoidal waveforms. These waveforms are obtained modulating the power supply voltage with two out of three legs. The third leg transistors are kept off. The system can therefore be approximated to a full-bridge

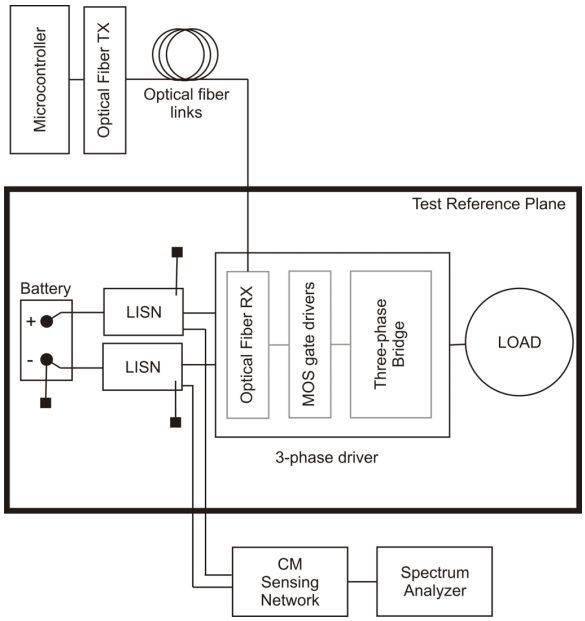

Figure 3.20: Preliminary CM EMI measurement test bench.

inverter, and the voltage at the third leg does not contribute to CM conducted emissions.

In order to measure only the disturbances generated by the inverter power circuitry, the microcontroller, which generates the PWM signals, is isolated from the inverter and it is placed out from the reference plane, as shown in Fig. 3.20. The gate signals generated by the microcontroller are provided to the gate drivers input through fiber optic connection. The inverter board is isolated by the reference plane and the parasitic capacitances C_{PU}, C_{PV} and C_{PW} have been estimated from the geometry of both the PCB and the test bench.

Since the motor used in these measurements is sensorless and the microcontroller is isolated from the inverter board, the motor is driven in open-loop. Two cases have been considered, as in the simulations previously performed: the first with $\tau_{\mathrm{d}} \approx 100\,\mathrm{ns}$, and the second with this delay manually compensated. The manual delay compensation consists in visualizing the output waveforms by means of an oscilloscope, and to compensate the delay reprogramming the microcontroller with adjusted PWM phase and duty cycle parameters. In Fig. 3.21 the output waveforms for $\tau_{\mathrm{d}} \approx 100\,\mathrm{ns}$ are presented, while in Fig. 3.22 the ones in which τ_{d} is compensated manually are shown.

The resulting EMI spectra for the two cases is shown in Fig. 3.23. The increase of the spectra in the lower frequency range, i.e. up to 3 MHz, is due the DM emission, which appears in the CM spectra because of a difference between the two LISN impedances.

Comparing the obtained results with the simulations, it can be seen that the two

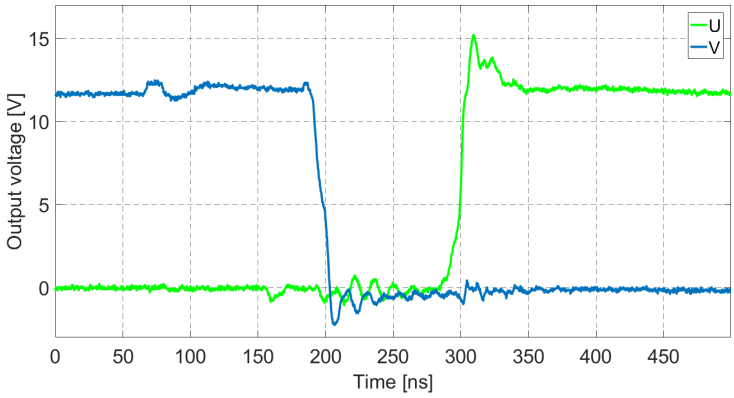

Figure 3.21: Active output waveforms: $\tau_d \approx 100\,\text{ns}$.

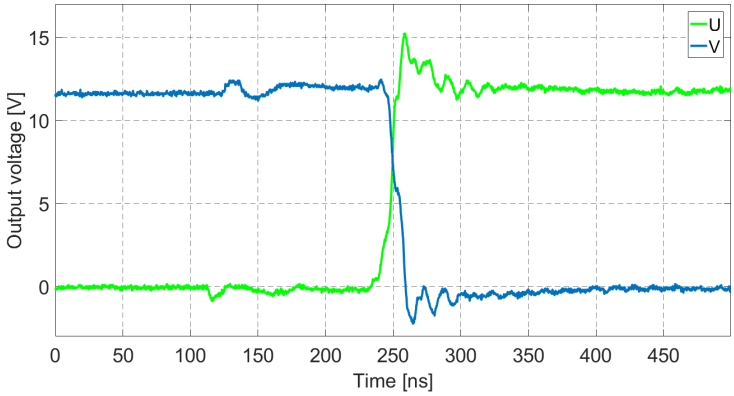

Figure 3.22: Active output waveforms: $\tau_d \approx 0\,\text{ns}$.

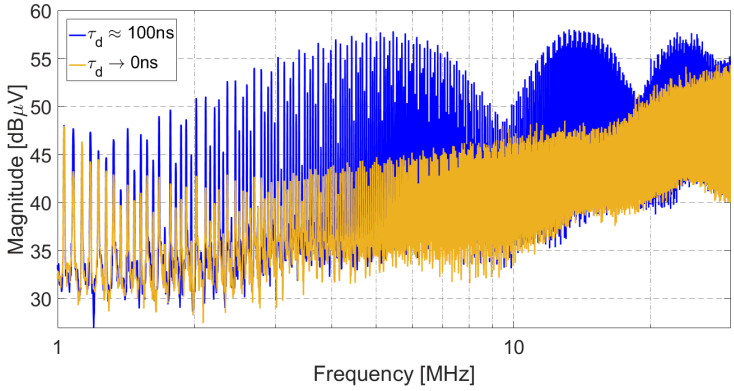

Figure 3.23: Measured spectra with $\tau_d \approx 100\,\text{ns}$ and $\tau_d \approx 0\,\text{ns}$.

results are in good accordance. From the simulations, the reduction in the range 1-30 MHz is around 10-15 dB, value which is confirmed by the measured 15 dB reduction peak. The differences between the simulated spectra and the measured

ones are due mainly to parasitic couplings which are not reported in the simulation schematic and to the fact that the delay is compensated in open loop. In order to further reduce the CM emission, a closed loop delay compensation should be designed and employed.

Chapter 4

Closed Loop Delay Compensation

The compensation delay technique, presented in the previous chapter and tested aligning manually the output edges, has shown good results in reducing the CM emission. However, the delay τ_d is not a fixed quantity: it could present variations due to temperature and load changes, aging of the components, etc. For this reason, in this Chapter, the design of a closed loop delay compensation technique is presented.

4.1 Feedback quantity for τ_d compensation

In order to automatically compensate the delay τ_d, a feedback quantity has to be provided to the microcontroller. The common mode voltage measured at the LISNs is the quantity that should be reduced. If such voltage is sampled as feedback quantity and it is elaborated by means of a controller, which varies the PWM parameters compensating τ_d, the CM EMI can be reduced. However, the CM voltage at the LISNs is not accessible on-board, and neither the reproduction of the LISN circuit on the PCB is possible, since the reference plane node can not be used. For these reasons, an on-board indirect quantity, related to the delay τ_d, should be sensed, without a direct connection to the reference plane node. For the following analysis, the circuit used to design the closed loop delay compensation system is the three-phase inverter used to drive a BLDC motor. The schematic of the inverter is reported in Fig. 4.1.

Since the CM EMI, as seen in Chapter 1, is generated by the output common mode voltage, i.e. the average voltage of the three inverter outputs, a possible solution is to sense the average of the three output voltages, V_U, V_V and V_W. Analyzing the LISNs circuit for the common mode, the series of the parasitic capacitances and the LISNs CM impedance represents an high-pass filter for the CM voltage of the outputs. If this high-pass filter is replicated on-board, with a lower cutoff frequency,

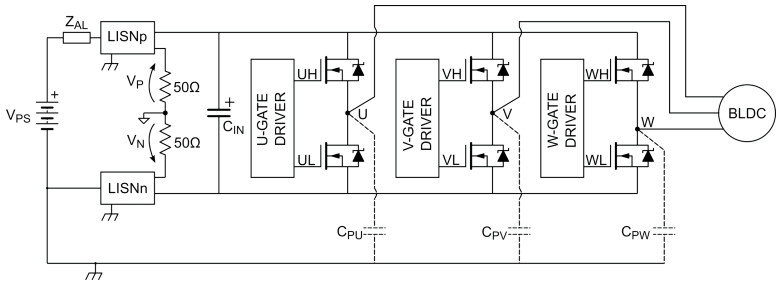

Figure 4.1: Three-phase inverter circuit.

the signal generating the CM emission can be sensed by the microcontroller. Looking at eq. (3.23), the first two terms of the product represent the open circuit CM voltage. Such a voltage, in time domain, can be expressed as the average of the three output voltages:

$$V_{\mathrm{CM,OC}}(t) = \frac{V_{\mathrm{U}}(t) + V_{\mathrm{V}}(t) + V_{\mathrm{W}}(t)}{3}. \tag{4.1}$$

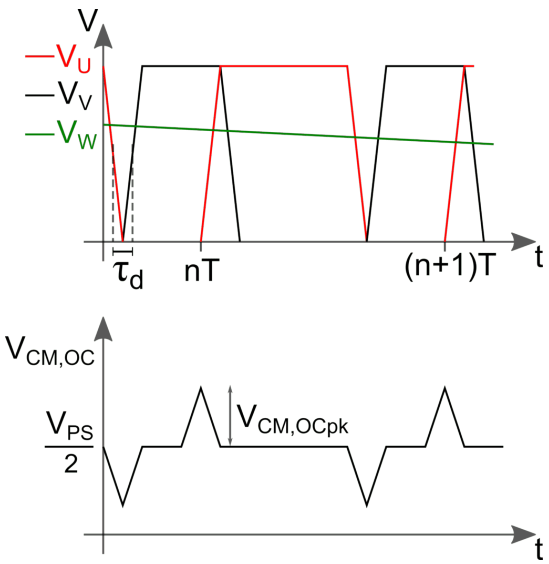

Figure 4.2: Open circuit common mode voltage.

In Fig. 4.2 a simplified representation for the $V_{\mathrm{CM,OC}}$ is shown, referred to the control step in which the U and V outputs are active and the output W is not driven. This voltage is the superposition of a DC component equal to $V_{\mathrm{PS}}/2$ and some voltage spikes dependent on the τ_{d} magnitude. These spikes are the responsible of the CM EMI. From the analysis performed, it is possible to see that the peak amplitude (positive or negative) for the open circuit CM voltage, $V_{\mathrm{CM,OCpk}}$, is proportional to the value of τ_{d} when this delay is lower than the rising/falling time t_{r}:

$$V_{\mathrm{CM,OCpk}} = \frac{V_{\mathrm{PS}}}{3} \cdot \frac{\tau_{\mathrm{d}}}{t_{\mathrm{r}}} \tag{4.2}$$

When $\tau_{\mathrm{d}} > t_{\mathrm{r}}$, $V_{\mathrm{CM,OCpk}}$ saturates at $V_{\mathrm{PS}}/3$. In Fig. 4.3 all the possible shapes for $V_{\mathrm{CM,OC}}$ are reported, considering, for instance, the control step with U and V outputs active.

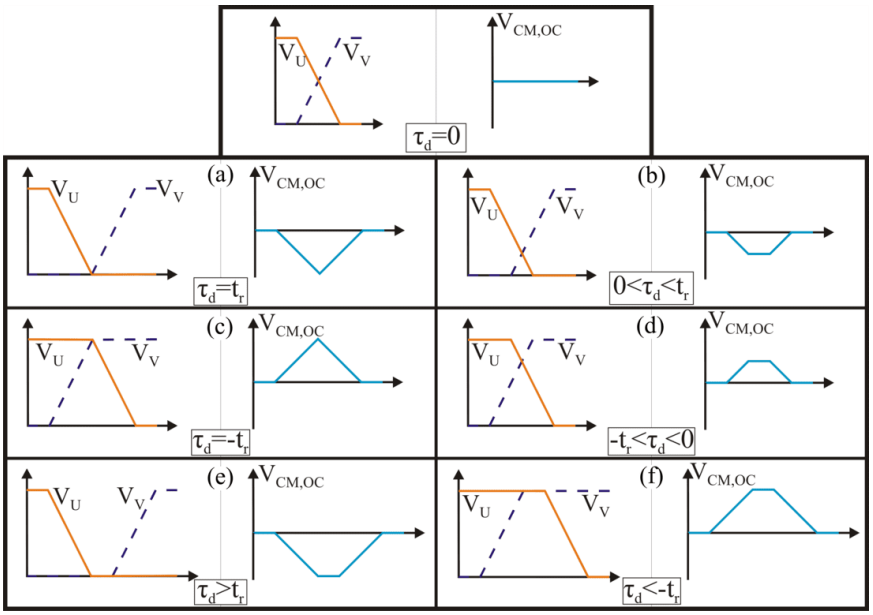

Figure 4.3: $V_{\mathrm{CM,OC}}$ shapes according to the delay τ_{d}.

This peak value $V_{\mathrm{CM,OCpk}}$, therefore, can be used as feedback quantity by the microcontroller to compensate τ_{d}, acting on the PWM parameters.

4.2 Signal conditioning circuit

The spikes superimposed to the voltage $V_{\mathrm{CM,OC}}$, present a width of few ns, therefore, for the direct sampling of this voltage, an high sampling rate ADC would be needed, without the guarantee of sampling the maximum peak voltage. Moreover, the spikes amplitude, in general, is out of the microcontroller ADC input voltage range. For these reasons, the $V_{\mathrm{CM,OC}}$ signal has to be given as input to a conditioning circuit. Such a circuit, shown in Fig. 4.4, is composed of three blocks: an high-pass filter and two envelope detectors. The high-pass filter is used to obtain the common mode voltage of the output waveforms, rejecting the DC component, which is useless for CM EMI. The three output nodes are so connected to three equal capacitors, terminated on a common resistor. The filter components C_{S} and R_{S} are chosen in order have a cutoff frequency $f_{\mathrm{t}} = 100$ kHz, which is higher than

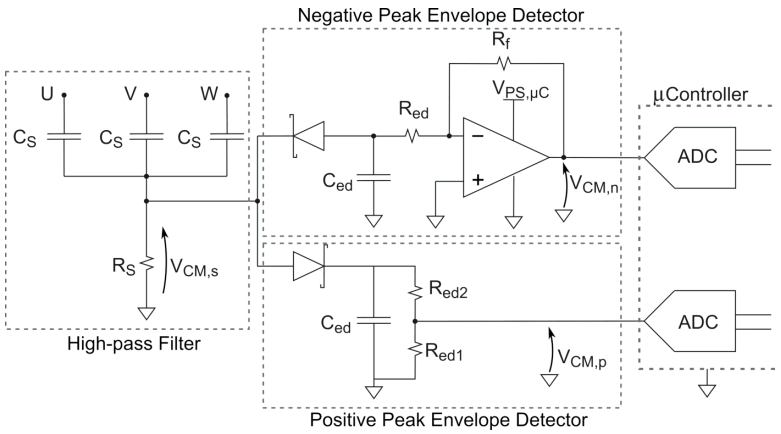

Figure 4.4: Signal conditioning circuit for common mode voltage sensing.

the switching frequency and lower than the minimum frequency for the conducted emission range. Moreover, such components are chosen to not load significantly the output nodes. Therefore, the C_S capacitance value can be chosen arbitrarily in the order of hundred of pF. The resistance value turns out to be:

$$R_\mathrm{S} = \frac{1}{2\pi f_\mathrm{t} C_\mathrm{S}}. \tag{4.3}$$

The signal at the output of the high-pass filter, $V_\mathrm{CM,s}$, is composed of positive and negative voltage spikes, which can be as narrow as few ns. Since such a signal cannot be sensed directly by the microcontroller, in which resides the delay compensation controller, two envelope detectors, one for the positive peaks and the other for the negative ones, are connected to the high-pass filter output. These circuits are highlighted in the schematic of Fig. 4.4 as *Positive peak envelope detector* and *Negative peak envelope detector*, respectively.

Both envelope detectors are designed in order to have a time constant reasonably fast with respect to the PWM period. In the designed circuit, a time constant near to $T/10$ has been chosen.

$$R_\mathrm{ed} C_\mathrm{ed} \approx \frac{T}{10} \tag{4.4}$$

The capacitor C_ed is designed to be lower than C_s. Once C_ed has been chosen, the resistance R_ed can be computed as:

$$R_\mathrm{ed} \approx \frac{T}{10}\frac{1}{C_\mathrm{ed}}. \tag{4.5}$$

The voltage at the output of each envelope detector should be scaled to the voltage input range of the microcontroller ADC. This range, in general, is from 0 V to the supply voltage of the microcontroller. For this reason, a voltage divider for

the positive peak envelope detector, and an attenuating inverting amplifier for the negative one, are employed. Such an amplifier should have an high slew rate in order to follow the input signal, since the rise time of the spikes is equal to the rise time of the output signal. For the positive envelope detector, considering Eq. (4.5), the two resistances of the voltage divider should satisfy the following relation:

$$R_{\mathrm{ed}} = R_{\mathrm{ed1}} + R_{\mathrm{ed2}}. \tag{4.6}$$

Finally, the scaling factor is designed as:

$$|K| = R_{\mathrm{ed1}}/R_{\mathrm{ed}}, \tag{4.7}$$

For the negative envelope detector, the impedance seen in parallel to the capacitor should be equal to R_{ed}. Therefore, the inverting amplifier input series resistance is equal to that value. The feedback resistance, instead, is designed using the same scaling factor of the positive branch:

$$|K| = R_{\mathrm{f}}/R_{\mathrm{ed}} \tag{4.8}$$

so $R_{\mathrm{f}} = R_{\mathrm{ed1}}$. In Tab. 4.1 designed component values have been reported.

The two voltages $V_{\mathrm{CM,p}}$ and $V_{\mathrm{CM,n}}$ are given as input to two independent ADC inputs of the microcontroller. The relation between the peak amplitude of $V_{\mathrm{CM,p}}$, $V_{\mathrm{CM,n}}$ and the peak voltage $V_{\mathrm{CM,pk}}$ is:

$$V_{\mathrm{CM,pk}} = V_{\mathrm{CM,p/n}} \frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} e^{\frac{t_{\mathrm{s}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_{\gamma}, \tag{4.9}$$

where t_{s} is the time interval between the commutation instant and the sampling instant and V_{γ} is the diode forward voltage. The definition of t_{s} is not straightforward, since the commutation instant is not known exactly due to the delay. A possible solution to address this issue consist in using an average commutation instant according to the circuit characteristics and, in case of oscillations between positive and negative delay after each cycle compensation, to perform a fine tuning, by compensation steps equal to the PWM resolution. This would minimize the CM emission, even if more PWM cycles would be needed.

The following paragraph presents how these measured voltages are used by the delay compensation loop controller.

4.2.1 Delay Compensation Algorithm

As seen in the previous paragraph, the microcontroller samples the conditioned signals and it adjusts the PWM parameters through a finite state machine (FSM), in order to compensate τ_{d}. For each BLDC control step, the leg whose duty cycle D is greater than 0.5 can be defined as Master, while the other active leg is defined as Slave. In case of a single-phase, full-bridge inverter, the choice of the Master

Table 4.1: Designed Component Values

Component	Value
C_S	680 pF
R_S	2.2 kΩ
C_{ed}	100 pF
R_{ed}	18 kΩ

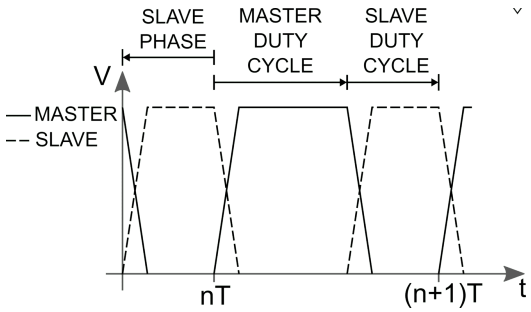

Figure 4.5: PWM parameters definition. In continuous line the Master output voltage, in dashed line the Slave one.

and Slave legs makes no difference. The Master leg has null phase and a duty cycle defined by the speed and current control loops, while the Slave has duty cycle equal to (1-D) and its phase value is set in order to obtain the complementary output waveform. In order to compensate the delay τ_d, the FSM acts only on the Slave's phase and duty cycle parameters, whose definition is shown in Fig. 4.5.

For each control step, two storage variables are defined for the compensation: one for the duty cycle, corr$x$.dc and one for the phase, corr$x$.ph, where $x = 1...6$ is related to the step. According to the possible cases shown in Fig. 4.3, the control acts using the truth table shown in Tab. 4.2, following the flow chart algorithm shown in Fig. 4.6.

The level of the measured voltage peak leads to two cases for computing the correction term. In the first case the measured voltage indicates that the delay is greater or equal to the rise time, as in the cases (a), (c), (e) and (f) of Fig. 4.3; the measured voltage will be greater than a voltage denoted in the flow-chart as $V_{CM,P-SAT}$ or $V_{CM,N-SAT}$, which can be computed substituting t_r in (4.2) and (4.9). The magnitude of the correction term in these cases will be equal to the rise time. Otherwise, the measured voltage indicates that the delay is lower than the rising/falling time, as shown in the cases (b), (d) of Fig. 4.3; the correction in these cases can be computed with a proportional relation derived by (4.2) and (4.9):

$$\tau_d = \frac{V_{\mathrm{ADC}} \frac{R_{\mathrm{ed}}}{R_{\mathrm{ed1}}} e^{\frac{t_{\mathrm{s}}}{R_{\mathrm{ed}} C_{\mathrm{ed}}}} + V_\gamma}{V_{PS}/3} t_{\mathrm{r}} \tag{4.10}$$

The above equation is denoted as *Formula* in the flow chart graph. The derived corrections, *corrPH* and *corrDC*, are so summed to the current step compensation variables, corr*x*.dc and corr*x*.ph, in each PWM cycle. Using this kind of control, the compensation variables are stored and recalled promptly each time the BLDC control state machine changes the active step.

Table 4.2: Delay Compensation Truth Table

	Positive peak	**Negative peak**
Master rising	Decrease	Increase
Slave falling	Duty Cycle	Duty Cycle
Master falling	Decrease	Increase
Slave rising	Phase	Phase

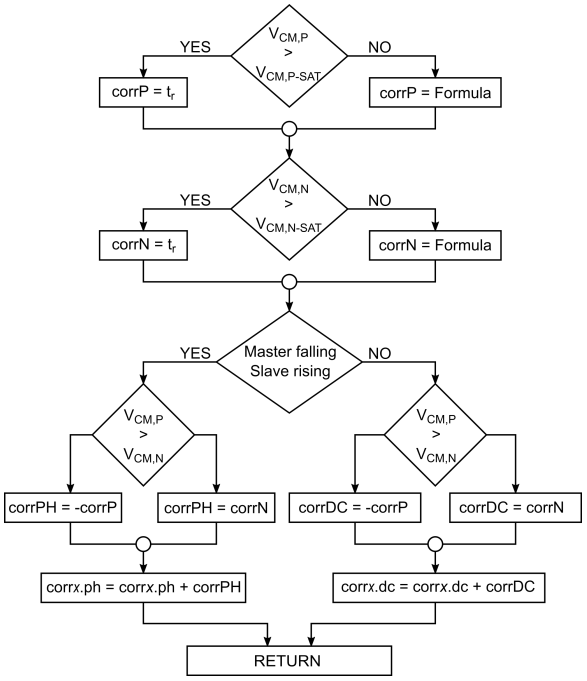

Figure 4.6: Delay compensation algorithm flow chart.

In the following section the proposed delay compensation technique is tested through mixed signal simulation.

4.3 Technique validation through simulation

In order to prove the effectiveness of the proposed technique in reducing the CM interference, the system was simulated with a Spice-like mixed signal simulator [34]. The simulation performed does not include the effect of the PCB parasitics, in order to reduce the circuit complexity and to improve the simulation convergence. The models of the active components used in the simulation can be found in the respective manufacturer website.

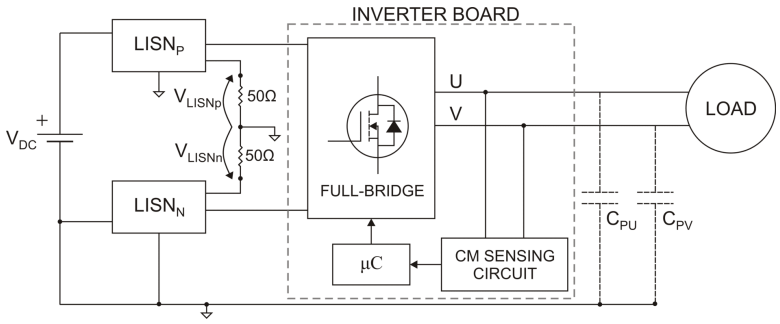

Figure 4.7: Simulated system

The circuit is composed of the two LISNs, as prescribed in CISPR25, the three-phase inverter, the signal conditioning circuit for the common mode output voltage and the controller, as shown in Fig. 4.7. The system is supplied at 12 V and the PWM modulation frequency was set to $f_s = 50\,\text{kHz}$. The rise time, in this simulation is $t_r = 14\,\text{ns}$. The system was simulated considering only one BLDC motor control step, i.e. the one in which the U and V outputs are active. The same results can be obtained considering the other control steps. Initially, the simulation was carried out with the control disabled and τ_d set approximately to 100 ns; then, after 0.5 ms, the EMI control loop was activated. From Fig. 4.8 it is possible to see the results of the delay compensation on the output transitions.

The results for the common mode voltage are shown in Fig. 4.9. From this graph it is possible to see both the CM voltage at the LISNs in the upper plot, and the voltage at the output of the high-pass filter in the lower one. The delay of 100 ns has been compensated in a few PWM periods, thus minimizing the CM emissions. The number of PWM cycles required to compensate the delay depends on its magnitude: if $\tau_d > t_r$, in every PWM cycle the delay is reduced by a quantity equal to t_r and when the delay becomes lower than the rise time, relation (4.10) is used to compensate the remaining delay.

The signals sensed by the microcontroller are shown in Fig. 4.10. The sampling instant occurs t_s ns after the output commutation command. The two signals are sampled by two independent ADC in the same time instant; then, according to the flow chart, they are compared and the information on the delay is given by the higher voltage between $V_{CM,p}$ and $V_{CM,n}$. From this graph it is possible to see that

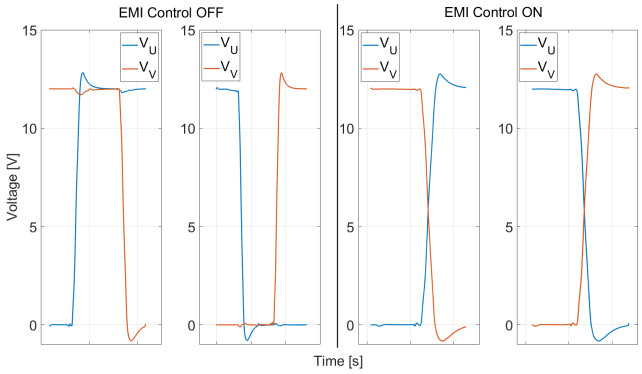

Figure 4.8: Active output waveforms. On the left the EMI control is deactivated, on the right the delay is compensated in closed loop.

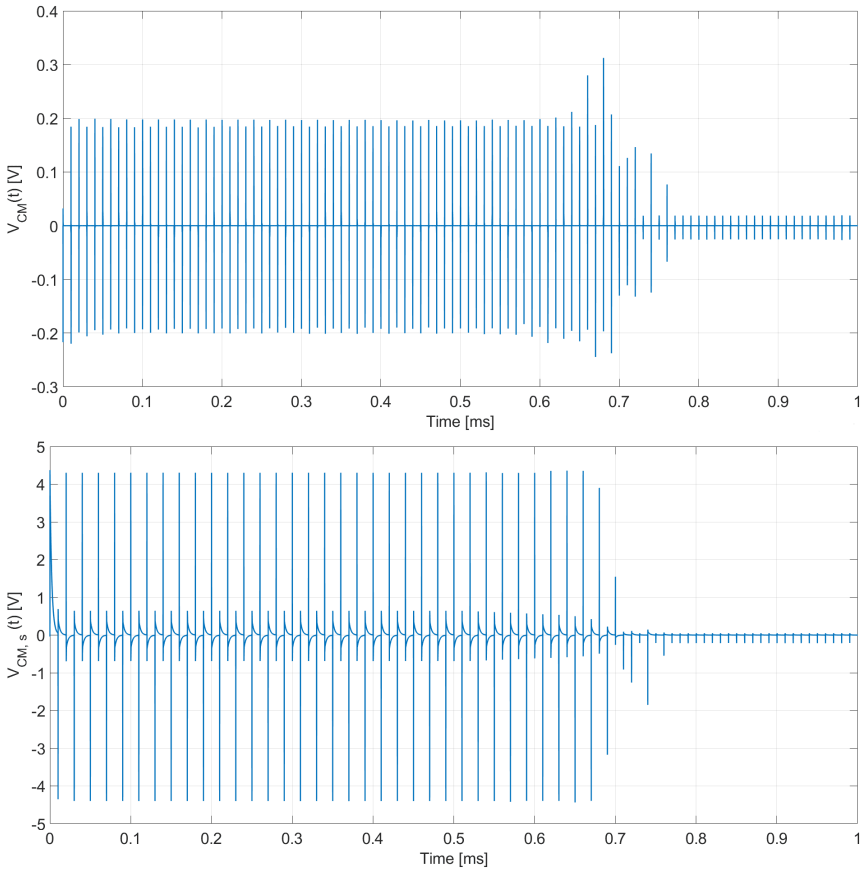

Figure 4.9: Simulation results: sensed CM noise and measured at the LISNs. The EMI control is activated at 0.5 ms.

the signal related to the negative spikes has a DC component, due to the offset of the operational amplifier, which contributes as an error on the delay compensation

loop. This justifies the reason because the negative spikes of Fig. 4.9 are larger (in magnitude) with respect to the positive ones.

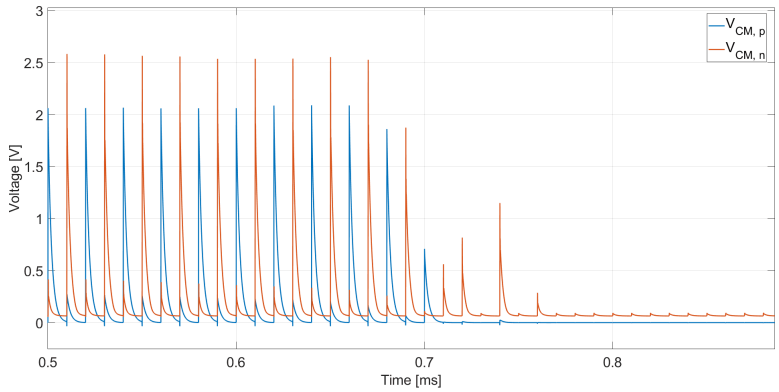

Figure 4.10: Simulation results. Voltages at the ADC input.

The CM disturbances at the LISNs, for the two cases of deactivated and activated control, were processed performing an FFT, in order to evaluate the conducted CM EMI spectra between 150 kHz and 30 MHz. The result is shown in Fig. 4.11. It is possible to see that the emissions are significantly reduced with the EMI control system turned on.

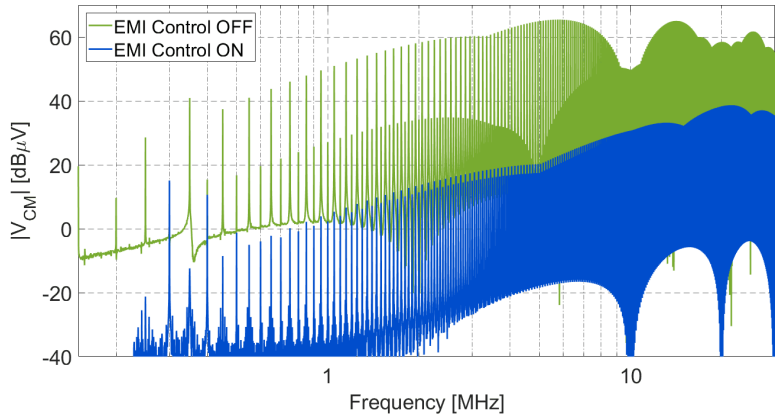

Figure 4.11: Simulation results: CM EMI spectra without (green) and with (blue) EMI control

Chapter 5

Prototype Design

In order to prove the effectiveness of the proposed technique, a BLDC motor driver has been designed. Such a inverter drives a BLDC motor for automotive applications, used in particular to drive the fan of radiator coolers. The PCB has to present limited dimensions in order to be mounted directly on the chassis of the BLDC motor. In the following sections the design specifications and the design procedure of the motor driver are presented.

5.1 Design Specifications

The load used for the following analysis is a BLDC motor used in automotive applications, which present maximum power lower than 1 kW. In this case the BLDC motor presents higher power and it is bigger with respect to the one used in preliminary measurements. This motor has been chosen in order to prove the technique in a more realistic context, i.e. the automotive one. In this case, Hall sensors are mounted on the stator in order to provide the rotor position. The presence of the sensors does not influence the CM emission reduction technique and the board will be designed to drive both sensored and sensorless motors.

5.1.1 Motor characterization

For the motor used in this application, the datasheet is not provided by the manufacturer. For this reason the motor was characterized, evaluating the main electromechanical parameters in order to design both the inverter hardware and the control. The only datum provided by the manufacturer is the rated power, which is equal to 600 W. The motor characterization is composed of the following phases:

- Electrical characterization: phase inductance and resistance;
- Electromechanical characterization: measurement of k_e;

- Sensor characterization: Hall effect sensor phasing.

The phase resistance of the motor was measured with an Agilent 34401A multimeter, performing a 4 wire measurement. The resulting line-to-line resistance is:

$$R_{\mathrm{l,l}} = (18 \pm 4)\mathrm{m}\Omega. \tag{5.1}$$

The phase resistance, therefore, turns out to be around 9 mΩ.

The phase inductance was evaluated injecting a square wave between two motor phases and measuring the time constant. Knowing that the series impedance of the waveform generator is $R_{\mathrm{g}} = 50\,\Omega$, the voltage on the motor phases has been measured by means of an oscilloscope. The result is shown in Fig. 5.1.

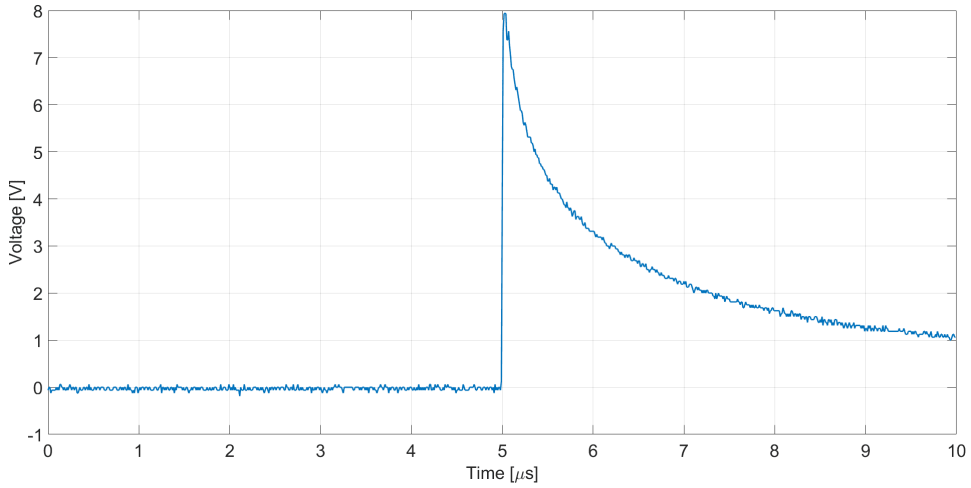

Figure 5.1: Line-to-line inductance measurement using time constant.

From the voltage decay, the $L_{\mathrm{S}}/R_{\mathrm{g}}$ time constant can be computed, neglecting the series resistance of the phase. The resulting phase inductance is equal to:

$$L_{\mathrm{S}} = 45.7\mu\mathrm{H} \tag{5.2}$$

The last parameters to be measured, in order to characterize the motor, are the BEMF constant k_{e} and the torque constant k_{t}. The k_{e} value can be found experimentally, while for the value of k_{t} an estimation is provided. The BEMF constant is measured forcing the rotor to rotate with an external motor, and measuring the open circuit voltages at the motor phase terminals. The ratio between the BEMF voltage and the rotor angular speed provides the value of k_{e} in V/(rad/s). Knowing that the number of pole pairs of the motor $p = 2$, the performed measurements gave as result a value of $k_{\mathrm{e}} = 11.4\mathrm{mV}/(\mathrm{rad/s})$.

The k_{t} constant, instead, can be estimated starting from k_{e}. If the BEMF waveforms are perfectly trapezoidal and the phase currents are rectangular, considering

null losses, the following relation is valid:

$$2 \cdot BEMF \cdot I = T \cdot \omega_{\mathrm{r}} \tag{5.3}$$

i.e. all the electrical power is converted in mechanical power. Using the definition of k_{t}:

$$k_{\mathrm{t}} = \frac{T}{I}, \tag{5.4}$$

and the one of k_{e}:

$$k_{\mathrm{e}} = \frac{BEMF}{\omega_{\mathrm{r}}}, \tag{5.5}$$

it is possible to write the following relation:

$$k_{\mathrm{t}} = 2k_{\mathrm{e}}. \tag{5.6}$$

From calculations it results $k_{\mathrm{t}} = 0.023\,\mathrm{Nm/A}$.

The control of the sensored BLDC motor is based on the Hall sensor outputs, which give information on the position of the rotor. In order to know the relation between the sensors outputs and the output phases to be activated, a characterization has been performed. The rotor was forced to rotate, and both the BEMF voltages and the Hall sensors outputs have been acquired together by a mixed signal oscilloscope. The result is shown in Fig. 5.2.

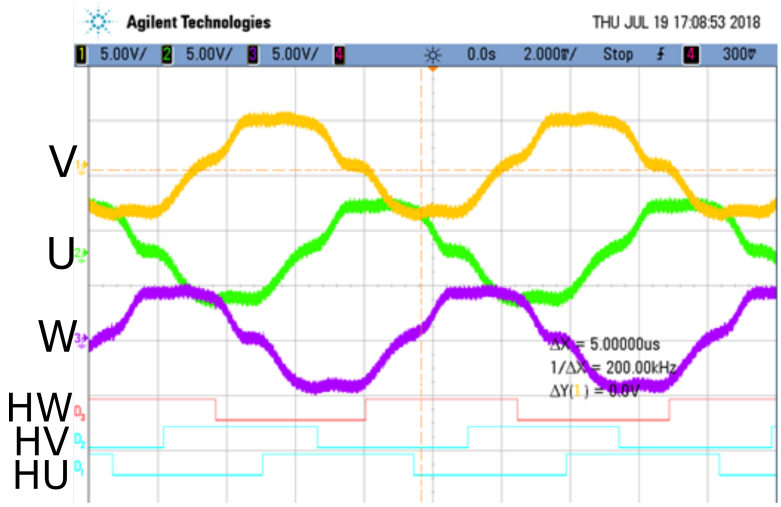

Figure 5.2: Measurement of the relation between Hall sensors outputs and BEMF.

Using this measurement, the configuration of the outputs according to the Hall sensors is summarized in Tab. 5.1. The colors are referred to the wire colors of the used motor, presented in Appendix B.

In conclusion, the used load has the following characteristics:

Table 5.1: Hall sensors outputs - BEMF phasing

HU (Brown)	**HV (Black)**	**HW (White)**	**U (Green)**	**V (Black)**	**W (Blue)**
1	0	1	High	Low	Float
0	0	1	Float	Low	High
0	1	1	Low	Float	High
0	1	0	Low	High	Float
1	1	0	Float	High	Low
1	0	0	High	Float	Low

- Power: 600 W
- Voltage Rating: 12 V
- Pole pairs p: 2
- $R_{\mathrm{l,l}}$: 18 mΩ
- $L_{\mathrm{l,l}}$: 91.4 μH
- k_{e} : 11.4 mV/(rad/s)
- k_{t} (estimated): 0.023 Nm/A

The inverter PWM modulation should be complementary PWM, in order to implement the CM EMI reduction technique proposed in this thesis. The motor should be controlled with two control loops, one controlling the current and one the speed. Since no encoder is mounted on the rotor, the Hall sensors should be used also as speed sensors.

5.2 Hardware design

The first step in the inverter design is the choice of the switches to be used. Since the DC voltage supply is $V_{\mathrm{PS}} = 12\,\mathrm{V}$ and the maximum current to the load is:

$$I_{\mathrm{max}} = \frac{600\,\mathrm{W}}{12\,\mathrm{V}} = 50\,\mathrm{A}, \tag{5.7}$$

power MOSFETs can be employed. Since the maximum current is relatively high, the MOS transistors should have a low on-resistance.

The schematic of the inverter is reported in Fig. 5.3.

The components or circuits to be designed and selected are:

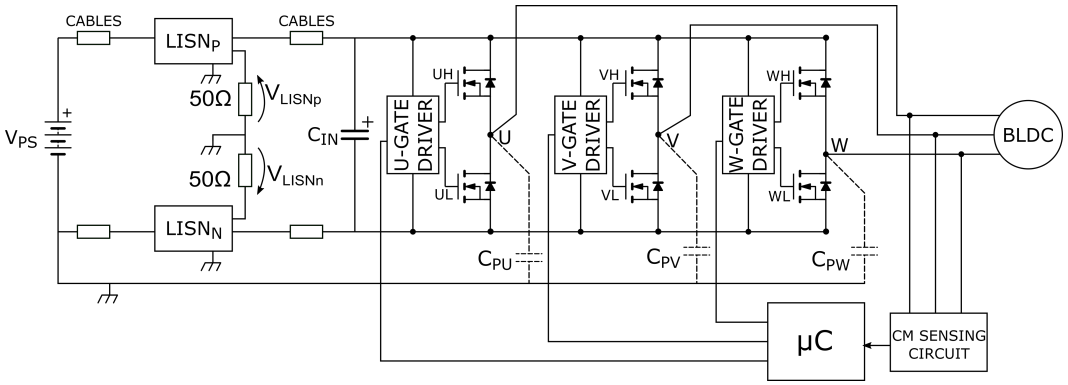

Figure 5.3: Inverter

- MOS transistors
- MOS gate drivers
- Snubbers
- Input capacitance
- Current sense circuits
- Microcontroller
- Voltage regulators
- Power supply filter (for DM EMI).

Moreover, although the BLDC motor described in the specifications is equipped with Hall sensors, the circuitry used to sense the BEMF, for sensorless motor drive, should be designed.

5.2.1 MOSFET selection

In order to select the MOS transistors, the following parameters should be chosen:

- Breakdown voltage
- Maximum drain current
- On-resistance
- Thermal resistance junction to case.

The breakdown voltage should be at least 50% higher than the DC supply voltage. The maximum continuous current should be at least 50 A. If the motor is driven at full load, i.e. the inverter output current is 50 A, it is desirable that less than 10% of the supply voltage drops on the on-resistance of the switches. Since two switches conduct for each time instants, the drain-source voltage for a single switch, according to the consideration drawn before, can be evaluated as:

$$V_{\mathrm{DS,on}} = \frac{(12\,\mathrm{V} \cdot 0.1)}{2} = 0.6\,\mathrm{V}. \tag{5.8}$$

Therefore, the on-resistance is:

$$r_{\mathrm{DSon,hot}} = \frac{V_{\mathrm{DS,on}}}{I_{\mathrm{max}}} = \frac{0.6\,\mathrm{V}}{50\,\mathrm{A}} = 12\,\mathrm{m\Omega} \tag{5.9}$$

This resistance is the so called the "hot" resistance of the MOS, i.e. the resistance that the MOSFET presents when it works and its junction temperature is well above the ambient temperature. The on-resistance declared on the MOS datasheet is the "cold" one, i.e. the one the MOS presents when its junction temperature is near to the ambient one. When the MOS transistor operates with its junction temperature near to the maximum allowed, the on-resistance is higher than the one referred to the ambient temperature [9]. Therefore, to select the MOS transistor, the following approximated relation can be used:

$$r_{\mathrm{DSon,cold}} \approx \frac{r_{\mathrm{DSon,hot}}}{1.5 \div 2} \approx 7\,\mathrm{m\Omega} \tag{5.10}$$

If 50 A flow in the transistor having a $r_{\mathrm{DSon}} = 12\,\mathrm{m\Omega}$, the power dissipated is 30 W. This means that, for thermal requirement, the r_{DSon} should be reduced. The device that has been chosen is Infineon IPD90N04S4-02 [35], with the characteristics reported in Tab. 5.2.

Table 5.2: Infineon IPD90N04S4-02 MOSFET main features.

V_{DS}	40 V
r_{DSon}	2.4 mΩ
I_{D}	90 A
Θ_{JA}	40 K/W
$T_{\mathrm{j,max}}$	175 °C
$V_{\mathrm{GS,th,max}}$	4 V
C_{iss}	9430 pF
C_{oss}	2120 pF
C_{rss}	127 pF
$Q_{\mathrm{g,tot}}$	118 nC

Using the thermal information provided by the manufacturer, it turns out that:

$$T_J = T_A + \Theta_{JA} \cdot P_d = 25°C + 40\,K/W \cdot r_{DSon} \cdot I_{max}^2 = 265°C \tag{5.11}$$

So, if the inverter works at full load, a heat-sink should be designed and inserted. The needed thermal resistance is:

$$\Theta_{JA} = \frac{T_J - T_A}{P_d} = 25\,K/W \tag{5.12}$$

5.2.2 MOS gate driver

Both the MOS transistors of each leg are n-channel MOSFETs. Therefore, a bootstrap circuit is needed to turn on the high-side transistor. The gate driver chosen for this inverter is the Texas Instruments LM5102 [32]. Such a device is a dual input high-side and low-side driver. Their supply voltage is 9-14 V and the output current is 1.6 A. The maximum device voltage for the bootstrap side is 40 V. Using this device, the input-output delay can be tuned adding two resistors at the terminals R_{t1} and R_{t2} of the integrated circuit, but in this project this feature is not used. A bootstrap capacitor is needed to drive the high-side MOS. The main parameters useful for the bootstrap capacitor design are listed in Tab. 5.3.

Table 5.3: Parameters for bootstrap capacitor selection.

Parameter	Value	Description
V_{DH}	1.1 V	Bootstrap diode forward voltage drop
V_{HBR}	7.1 V	HB Rising Threshold
V_{HBH}	0.4 V	HB Threshold Hysteresis
V_{PS}	12 V	Supply voltage of the gate drive IC
F_{sw}	50 kHz	Switching Frequency
I_{HBO}	10 μA	Total HB Operating Current
$Q_{g,max}$	118 nC	Total gate charge
D_{max}	0.95	Maximum Duty Cycle

The bootstrap capacitor is designed as follows. The maximum voltage loss on the capacitor terminals is computed as:

$$\Delta V_{HB} = V_{PS} - V_{DH} - V_{HBR} + V_{HBH} = 12\,V - 1.1\,V - 7.1\,V + 0.4\,V = 4.2\,V. \tag{5.13}$$

Then, it is possible to evaluate the total charge delivered to the gate of the MOS and the one lost in the driver:

$$Q_{tot} = Q_{g,max} + I_{HBO}\frac{D_{max}}{F_{sw}} = 108\,nC + 10\,\mu A \cdot \frac{0.95}{50\,kHz} = 108.2\,nC. \tag{5.14}$$

Therefore, the bootstrap capacitor turns out to be:

$$C_{\mathrm{B}} = \frac{Q_{\mathrm{tot}}}{\Delta V_{\mathrm{HB}}} = 26\,\mathrm{nF} \rightarrow 33\,\mathrm{nF}. \tag{5.15}$$

The voltage rating of such a capacitor should be at least twice V_{PS}, so a capacitor with maximum rating voltage of 50 V and X7R dielectric for good thermal behavior, has been used.

Moreover, in order to damp the oscillations at the MOS gate, given by the resonance between the gate capacitance and the parasitic inductance of the PCB traces and of the gate driver, a low resistance resistor (1-10 Ω) should be added in series with the gate terminal.

5.2.3 Inverter Leg

Each inverter leg is composed by the gate driver, the high-side and low-side MOSFETs, the BEMF filter and some snubbers. The BEMF filter is made of a voltage divider and a first order, low-pass filter, whose cutoff frequency is located at least one decade below the PWM switching frequency.

The snubbers are designed in the prototyping phase, looking at the output waveforms ringing. A first estimation of the needed snubber can be obtained from Spice simulations. There are two kinds of snubbers placed in the schematic: the classic dissipative RC [36] snubber and a RCD clamp snubber circuit [37]. This last circuit is used only if the overshoot voltage during the transition exceeds by 20% the supply voltage. This circuit is shown in Fig. 5.4.

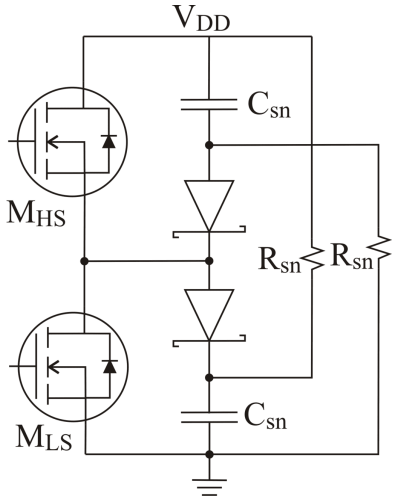

Figure 5.4: RCD clamp snubber.

At steady state, the snubber capacitor voltage is equal to V_{PS}. During, for instance, the low-to-high transition, the voltage at the output rise up to the supply

voltage plus the threshold voltage of the diode. Then, the diode begin to conduct, charging the capacitor, which will discharge on the resistance. This kind of snubbers presents relatively low losses, since the power dissipated in the resistor is equal to:

$$P_{\mathrm{d}} = \frac{1}{2} C_{\mathrm{sn}} (V_{\mathrm{pk}}^2 - V_{\mathrm{PS}}^2) f_{\mathrm{sw}}. \tag{5.16}$$

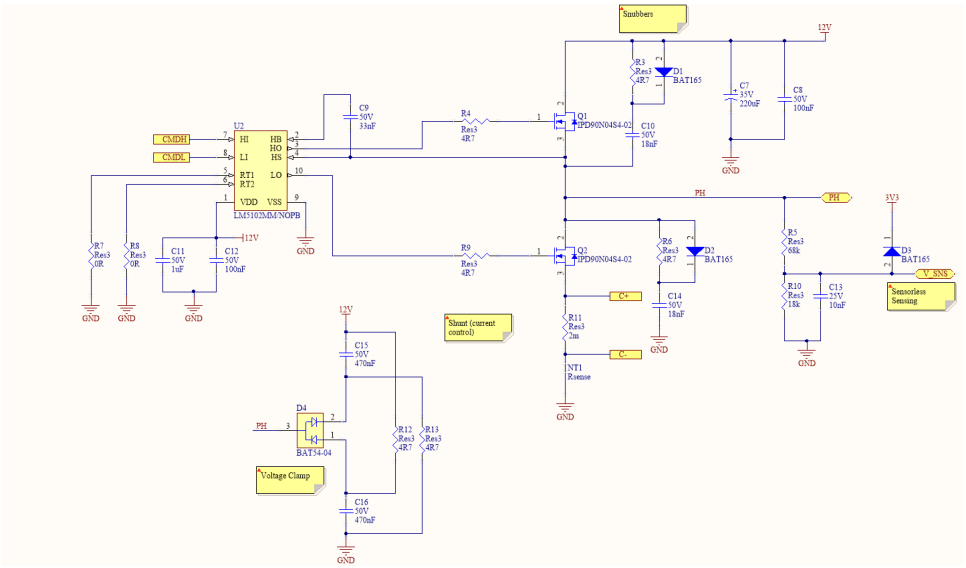

Figure 5.5: Inverter Leg

The classical RC snubber, instead, is designed starting from the measurement of the output oscillation frequency, f_{osc}. Then, a capacitor C_1 of few nF is placed between the oscillating node and ground, and the new oscillation frequency is measured, f_{osc1}. Since the oscillation is due to an LC resonant circuit, it can be written that:

$$f_{\mathrm{osc}} = \frac{1}{2\pi\sqrt{L_{\mathrm{p}} C_{\mathrm{p}}}} \quad , \quad f_{\mathrm{osc1}} = \frac{1}{2\pi\sqrt{L_{\mathrm{p}} (C_{\mathrm{p}} + C_1)}}. \tag{5.17}$$

Comparing the two equations, it can be derived that:

$$C_{\mathrm{p}} = C_1 \frac{f_{\mathrm{osc1}}^2}{f_{\mathrm{osc}}^2 - f_{\mathrm{osc1}}^2} \tag{5.18}$$

Once the parasitic capacitance is known, it is possible to compute the parasitic inductance:

$$L_{\mathrm{p}} = \frac{1}{C_{\mathrm{p}} (2\pi f_{\mathrm{osc}})^2} \tag{5.19}$$

The snubber capacitance is chosen in the range [36]:

$$6C_{\mathrm{p}} < C_{\mathrm{s}} < 8C_{\mathrm{p}} \tag{5.20}$$

The characteristic impedance of the network is:

$$Z_{\mathrm{c}} = \sqrt{\frac{L_{\mathrm{p}}}{C_{\mathrm{p}} + C_{\mathrm{s}}}} \tag{5.21}$$

The quality factor of the resonator has to be low, therefore the optimum value of the snubber resistance R_{s} is in the range:

$$Z_{\mathrm{c}} < R_{\mathrm{s}} < 2Z_{\mathrm{c}} \tag{5.22}$$

Once the snubber is designed, it can be tuned in order to damp other oscillation that can be present in the circuit. The schematic of each inverter leg is reported in Fig. 5.5.

5.2.4 Input Capacitance

The input capacitance should be dimensioned in order to filter the ripple current going to the load, keeping the power supply voltage stable. The ripple current, when the duty cycle is at 50 %, is:

$$I_{\mathrm{ripple}} = \frac{V_{\mathrm{PS}} D}{2 L_{\mathrm{S}} f_{\mathrm{sw}}} \tag{5.23}$$

$$I_{\mathrm{ripple}} = \frac{12\,\mathrm{V} \cdot 0.5}{91.4\,\mu\mathrm{H} \cdot 50\,\mathrm{kHz}} = 1.3\,\mathrm{A} \tag{5.24}$$

In order to keep the voltage ripple within 1% the capacitor should have an ESR as follows:

$$\mathrm{ESR} < \frac{V_{\mathrm{PS}} \cdot 0.01}{I_{\mathrm{ripple}}}. \tag{5.25}$$

The ESR value turns out to be:

$$\mathrm{ESR} < \frac{12\mathrm{V}}{1.3\,\mathrm{A}} \cdot 0.01 = 91\,\mathrm{m\Omega} \tag{5.26}$$

Since the pole given by the ESR, for electrolytic capacitor is usually located at f_{p} = 8-10 kHz, it is possible to estimate a capacitance value:

$$C_{\mathrm{in}} > \frac{1}{2\pi \mathrm{ESR} f_{\mathrm{p}}} = 330\,\mu\mathrm{F}. \tag{5.27}$$

Looking at the catalog, in order to have a capacitor with series resistance lower than 60 mΩ, minimum operating voltage greater than 25 V, rated ripple current greater than 2 A and reduced dimensions, the choice is United Chemi-Con EGPD250ELL472ML25H [38]. The features of this capacitor are listed in Tab. 5.4.

Table 5.4: Input capacitor features.

Parameter	Value
C	4.7 mF
ESR	28 mΩ at 100 kHz
V_W	25 V
I_{ripple}	4.26 A at 100 kHz
Case diameter	16 mm
Height	26.5 mm

5.2.5 Microcontroller

The first parameter for the selection of the microcontroller used to drive the motor and to host the delay compensation controller, is the PWM resolution. This parameter describes the minimum time variation that the microcontroller is able to impose for the duty cycle and phase parameters. An acceptable value for this resolution is around 1 ns. Therefore, the choice of the microcontroller is restricted on the models with dedicated PWM generation hardware, since the clocking frequency of the microcontroller is usually lower than 1 GHz.

Moreover, the microcontroller should present the following features:

- PWM output channels : 6 (one for each transistor).
- ADC inputs:

  3 for current sensing;

  power supply voltage sensing;

  analog speed reference;

  2 for delay compensation control loop;

  3 for sensorless control (BEMF sensing).

- Digital inputs/outputs:

  Start/Stop switch;

  3 Hall sensors input;

  SPI channel.

- Power supply voltage: 5 V or 3.3 V.

The microcontroller which collects all these features is the Microchip dsPIC33EP128GS704 [39]. It is a 16-bit microcontroller, supplied at 3.3 V, with PWM resolution for duty cycle, dead time and phase equal to 1.04 ns. The maximum CPU speed is 70 MHz,

but both the PWM unit and the ADC are clocked at 120 MHz with an internal PLL frequency multiplier. It presents 5 SAR ADC, with 17 input pins. Therefore, it is possible to sample in the same time instant up to 5 different quantities.

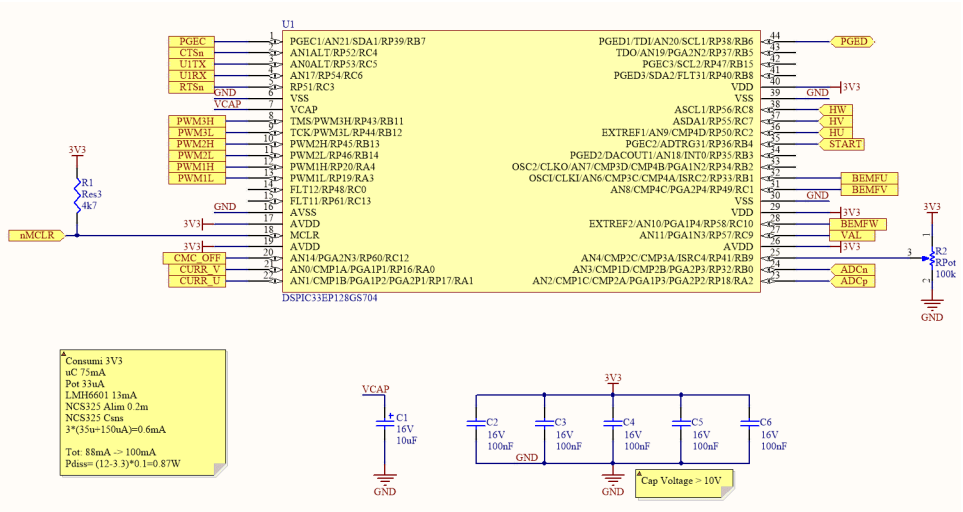

Figure 5.6: Microcontroller

5.2.6 Current sensing

In order to acquire a feedback quantity for the motor current controller, a current sensing circuit should be designed. The current is sensed on the low-side MOSFET of each leg with a shunt resistor. The voltage across the resistor is filtered and amplified in order to be sensed by the microcontroller.

The shunt resistor should be able to dissipate the power generated by the current flowing through it. Since most of the SMD shunt resistors are able to dissipate power up to 3 W, the maximum resistance value will be:

$$R_{\mathrm{s,max}} = \frac{P_{\mathrm{r}}}{I_{\mathrm{max}}^2} = \frac{3\,\mathrm{W}}{(50\,\mathrm{A})^2} = 1.2\,\mathrm{m\Omega}. \tag{5.28}$$

The current can flow in the resistor in both directions, depending on whether the MOS or the recirculating diode is conducting. The microcontroller ADC input voltage range can vary from 0 to 3.3 V. Therefore, the input ADC signal should have a polarization of $3.3\,\mathrm{V}/2 = 1.65\,\mathrm{V}$, and the current span 0-50 A should correspond to 0-1.65 V. This means that:

$$V_{\mathrm{Rs}}(I = 50\,\mathrm{A}) = 1.2\,\mathrm{m\Omega} \cdot 50\,\mathrm{A} = 0.06\,\mathrm{V}, \tag{5.29}$$

and the amplifier gain can be derived as:

$$\text{Gain} = \frac{V_{\max}}{V_{\text{Rs}}(I = 50\,\text{A})} = \frac{1.65\,\text{V}}{0.06\,\text{V}} = 27.5. \tag{5.30}$$

The main drawback of such a wider current range is that, for low currents, the sensing accuracy is low. In fact, for 1 A current, the input ADC voltage will be 33 mV, and since the ENOB of the ADC is 10.3 bits, the minimum voltage resolution is $(3.3\,\text{V}/2^{10.3}) = 2.61\,\text{mV}$, that corresponds to 80 mA.

The voltage drop across the shunt resistor should be filtered in order to avoid to sense voltage spikes and to sense only the average current flowing into the load. Moreover, the common mode voltage given by the ground bouncing should be rejected. To this purpose, a differential amplifier, with common mode and differential mode filters has been designed. The schematic is shown in Fig. 5.7.

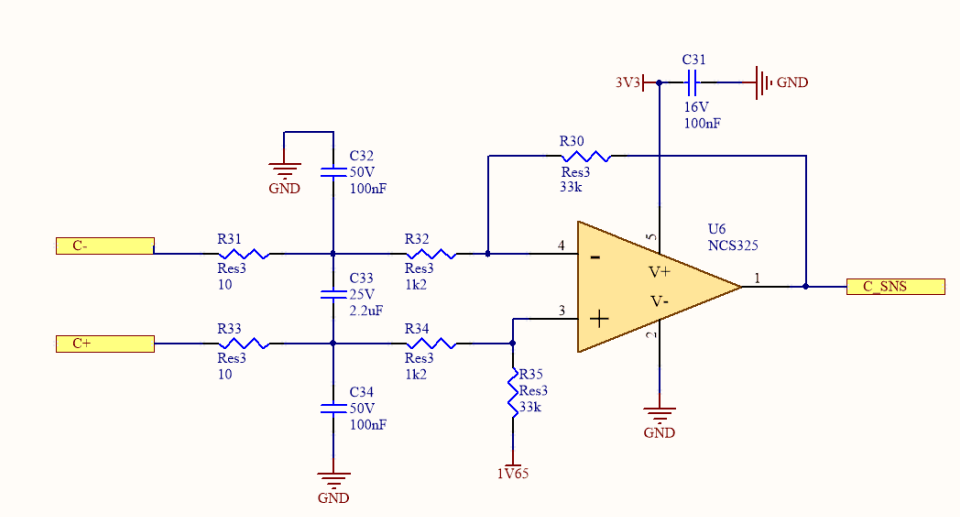

Figure 5.7: Current sensing circuit schematic.

Looking at the schematic, the component values have been designed as follows:

$$\text{Gain} = R_{30}/R_{32} = R_{35}/R_{34} = 27.5. \tag{5.31}$$

The differential pole is place one decade below the PWM switching frequency. The resistances R_{31}, R_{33} are equal in value and should be significantly lower than the differential gain resistances, so $R_{31} = R_{33} = 10\,\Omega$.

$$f_{\text{p,diff}} = \frac{1}{2\pi 2 R_{31} C_{33}} < 5\,\text{kHz}, \tag{5.32}$$

so,

$$C_{33} > \frac{1}{2\pi 2 \cdot 20\,\Omega \cdot 5\,\text{kHz}} = 1.6\,\mu\text{F} \rightarrow 2.2\,\mu\text{F}. \tag{5.33}$$

The common mode filter is not mandatory, but if needed, its pole frequency is:

$$f_{\mathrm{p,comm}} = \frac{1}{2\pi R_{31} C_{32}}, \quad C_{34} = C_{32} \tag{5.34}$$

The operational amplifier most important parameters to be taken into account are: single supply voltage at 3.3 V, low offset voltage, rail-to-rail output. The gain-bandwidth product is not critical since the current is filtered. The operational amplifier that has been chosen is the On Semiconductor NCS325 [40].

5.2.7 Voltage regulator selection

The board is supplied by a battery, whose voltage is around 12 V. The microcontroller, the current sensing circuits and the CM voltage sensing circuit are supplied at 3.3 V. It is necessary to choose the topology needed for the voltage regulator, according to the current consumption of the 3.3 V supplied circuits.

The current consumption of each circuit is reported in the following table.

Device	**Consumption**
DSPIC33EP128GS704	75 mA
Potentiometer	33 μA
CM Sensing	13 mA
Current sensing	0.2 mA + 3*(35 μA+150 μA)=0.8 mA
Total	88 mA $\rightarrow$ 100 mA

Considering the dropout voltage V_{do} as the difference between the input and output voltages of the regulator, it is possible to evaluate the dissipated power of a low dropout regulator (LDO):

$$P_{\mathrm{diss}} = V_{\mathrm{do}} \cdot I_{\mathrm{supply}} = (12\,\mathrm{V} - 3.3\,\mathrm{V}) \cdot 0.1\,\mathrm{A} = 0.87\,\mathrm{W}. \tag{5.35}$$

Since the dissipated power is not too high, a LDO can be used to regulate the supply voltage. The ST-Microelectronics LD1117D33TR [41] has all the features required. The schematic is reported in Fig. 5.8. The thermal resistance Θ_{JA} is equal to 55 K/W, so the temperature increase at full load is $(55\,K/W \cdot 0.87\,W = 47.9\,K)$. With an ambient temperature of 25°C, the junction temperature will be 72.9°C, which is lower than the maximum operating junction temperature of 125°C.

5.2.8 DM EMI filter design

The differential mode (DM) current, as seen in Section 5.2.4, is generated by a 1.2 A peak to peak ripple current flowing in the input capacitance. In order to comply with the CISPR25 standard Class 5 conducted emission limits, presented in 1.4.2, the DM current has to be attenuated with a second-order low-pass filter.

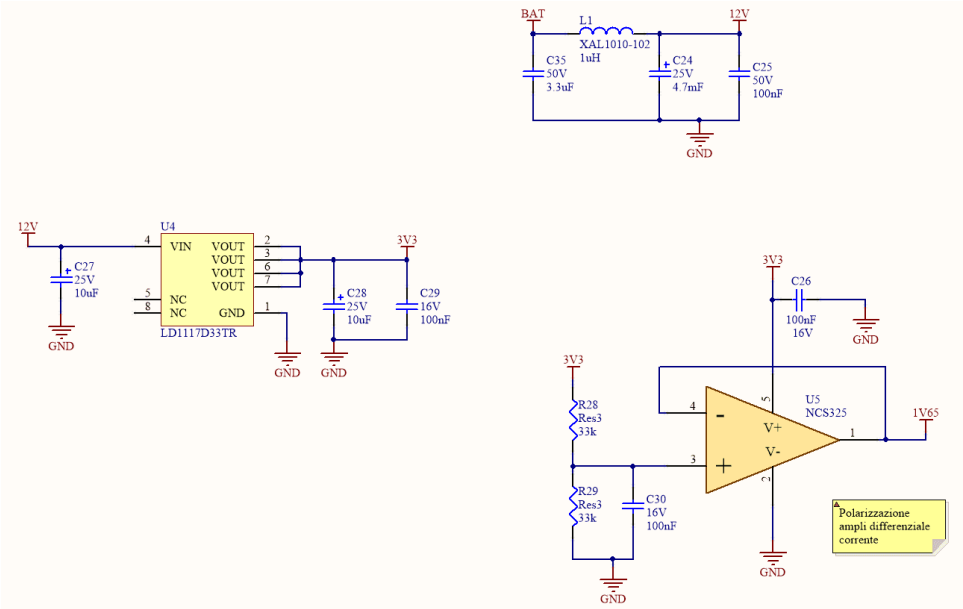

Figure 5.8: Supply circuits schematic.

The spectrum envelope of the ripple current flowing in C_{in} can be described as [42]:

$$I_{\text{ripple}} = \frac{I_{\text{pp}} \cdot \omega_{\text{sw}}}{\pi} \frac{1}{\omega}, \tag{5.36}$$

where I_{pp} is the peak to peak current and $\omega_{\text{sw}} = 2\pi f_{\text{sw}}$. This current flows in the input capacitance impedance $Z_{\text{C}_{\text{in}}}$. So there are one pole in $f_{\text{p}} = 0\,\text{Hz}$ and two zeros in:

$$f_{\text{zESR}} = \frac{1}{2\pi CESR} = 1.2\,\text{kHz} \quad , \quad f_{\text{z,ESL}} = \frac{ESR}{2\pi ESL} = 220\,\text{kHz} \tag{5.37}$$

The flat region level is equal to the ESR value, i.e. $28\,\text{m}\Omega$, which means -31 $\text{dB}\Omega$ as can be seen in Fig. 5.9.

Since $Z_{\text{C}_{\text{in}}} << 100\,\Omega$ it is possible to generate an equivalent Thevenin circuit, with a negligible series impedance. The equivalent voltage is:

$$V_{\text{DM}} = I_{\text{ripple}} \cdot Z_{\text{C}_{\text{in}}} \tag{5.38}$$

The resulting spectrum is reported in the following graph.

From the spectrum it is possible to note that the DM voltage should be reduced by 9 dB at 150 kHz. According to the filter design presented in Chapter 2, the two poles should be placed at:

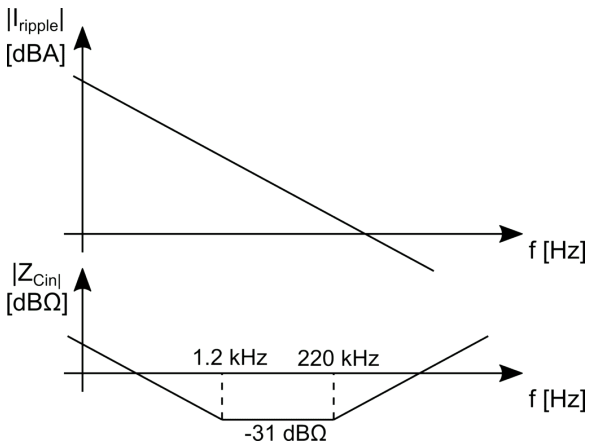

Figure 5.9: Ripple current spectrum envelope and input capacitor impedance.

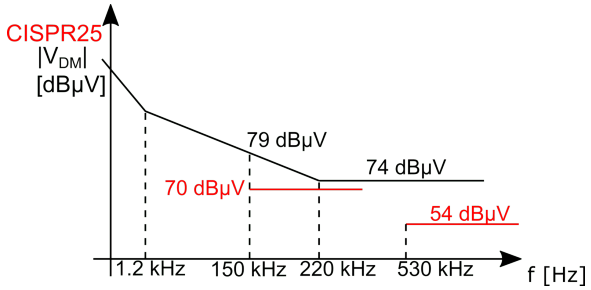

Figure 5.10: DM voltage spectrum. In red the imposed CISPR25 Class 5 limits [3].

$$f_{\mathrm{c,DM}} = \sqrt{10^{(-9\,\mathrm{dB}/20)}}150\,\mathrm{kHz} = 89\,\mathrm{kHz} \tag{5.39}$$

The poles frequency is:

$$f_{\mathrm{c,DM}} = \frac{1}{2\pi\sqrt{L_{\mathrm{DM}}C_{\mathrm{x}}}} \tag{5.40}$$

and the filter quality factor is:

$$Q = \frac{Z_0}{Z_{\mathrm{LISN,DM}}} \tag{5.41}$$

where $Z_{\mathrm{LISN,DM}}$ is equal to the LISN differential impedance, i.e. $100\,\Omega$.

$$Z_0 = \sqrt{\frac{L_{\mathrm{DM}}}{C_{\mathrm{x}}}}. \tag{5.42}$$

Aiming to obtain a quality factor equal to 1, the following relation has been derived:

$$\sqrt{\frac{L_{\mathrm{DM}}}{C_{\mathrm{x}}}} = 100\,\Omega \tag{5.43}$$

It results that:

$$L_{\mathrm{DM}} = 180\,\mu\mathrm{H} \quad , \quad C_{\mathrm{x}} = 18\,\mathrm{nF} \tag{5.44}$$

The filter has be re-dimensioned since the inductor manufacturer does not produce high inductance components for high current applications. The highest inductance value for I_{rms} equal to 50 A is 1 μH, so the corresponding capacitor value to obtain the same cutoff frequency is 3.3 μF. Using this filter also the CISPR limit present at 530 kHz is satisfied. The filter schematic is reported in Fig. 5.8.

5.2.9 PCB Layout

The PCB layout includes the designed inverter and the additional circuitry for the delay compensation technique, presented in Chapter 4. The signals to be routed are too many for a two layer board; the four layer PCB has been chosen. The PCB traces have been routed on the top and on the bottom layer; the middle layers are both ground planes. All the components have been mounted on the top layer, and the positive power supply has been routed on the same layer. On the bottom layer are present the thermal pads of the MOSFETs and some signal that cannot be routed on the top layer and require an environment that is not polluted by EM fields.

The layout of the inverter has been reported in Fig. 5.11. The PCB dimensions are 100 mm x 80 mm and the board is intended to be mounted directly on the motor frame. In the upper part of the board the power supply input and the differential filter are present, in the middle there are the three inverter legs with the three output pads for the phases U, V and W. Just below the legs there are the three shunt resistors for the current sensing connected to the respective differential amplifier. In the middle of the PCB the delay compensation feedback network has been routed. It is worth underlining that the circuit occupies a minimal PCB area, with respect to a generic common mode filter. In the lower part of the board is present the microcontroller with its own supply circuits. The Hall sensors can be connected to the bottom-left connector, while on the left of the microcontroller, the circuits for sensorless control have been predisposed. Some additional component such as the switch and the potentiometer on the bottom-left are used to turn on/off the motor and to regulate the speed, respectively.

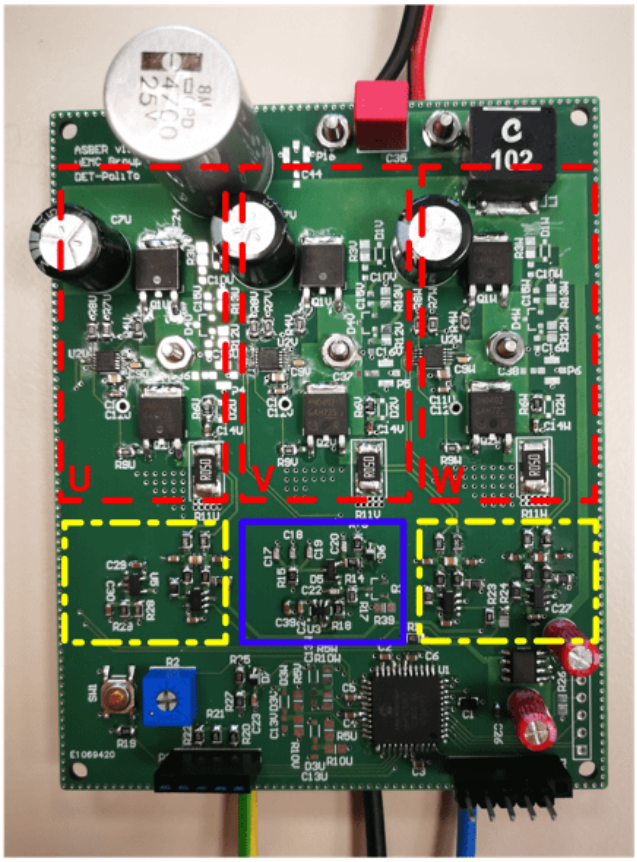

Figure 5.11: BLDC motor driver PCB. The main PCB blocks are highlighted: in the dashed boxes the three legs; in the dashed-dotted boxes the current sensing circuits; in the continuous box the delay compensation sensing circuit. The microcontroller and its power supply regulator are located in the lower part of the board.

5.3 Software design

Once the hardware has been designed, it is possible to proceed with the design of the firmware to be loaded on the microcontroller. This software can be divided in three main parts:

- Microcontroller configuration;
- Motor control loop;
- Delay compensation control loop.

The block diagram of the microcontroller internal devices is shown in Fig. 5.12. In this figure, the used peripheral modules are highlighted.

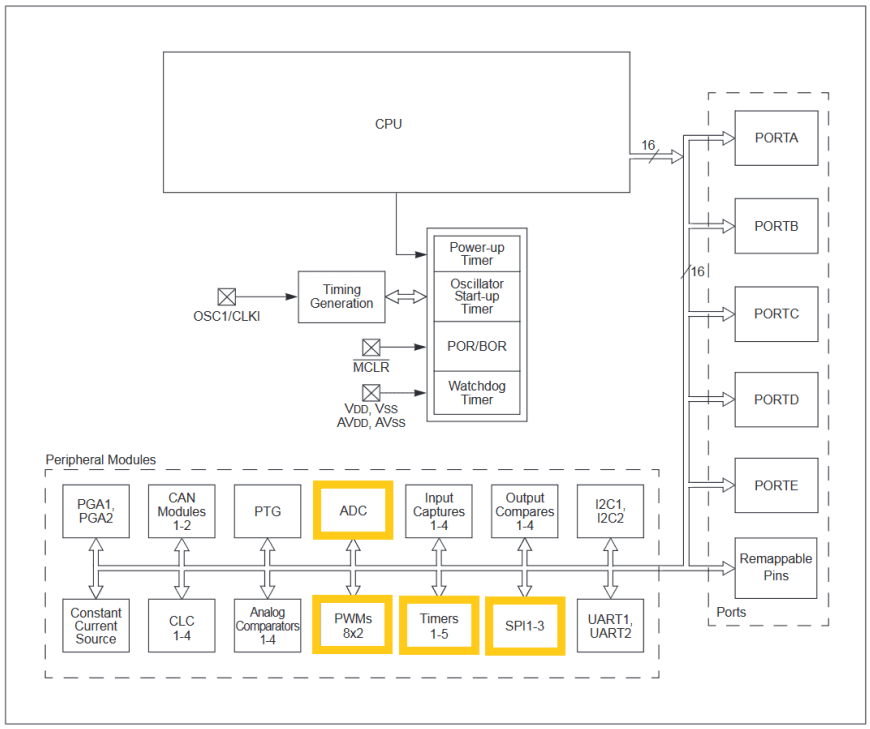

Figure 5.12: Microcontroller block diagram [39]. The peripheral modules used in this project are highlighted.

5.3.1 Microcontroller configuration

The first configuration to be set in the microcontroller is the timing generation. The source of the clock signal is the internal RC oscillator, which provides an oscillation frequency of 7.37 MHz. The oscillator output is connected to a PLL, which boosts the clock frequency up to 70 MHz. Fig. 5.13 shows the timing generation block diagram.

The parameters shown in Fig. 5.13 have been configured to obtain a $f_{\mathrm{PLL}} = 120\,\mathrm{MHz}$ and therefore a clock frequency $f_{\mathrm{CK}} = f_{\mathrm{PLL}}/2 = 60\,\mathrm{MHz}$.

$$f_{\mathrm{PLL}} = f_{\mathrm{RC}} \frac{(PLL_{\mathrm{DIV}} + 2)}{(PLL_{\mathrm{PRE}} + 2) \cdot 2(PLL_{\mathrm{POST}} + 1)} = 7.37\,\mathrm{MHz} \cdot \frac{65 + 2}{2 + 2} \approx 123.4\,\mathrm{MHz} \tag{5.45}$$

The clock frequency is therefore $f_{\mathrm{CK}} = f_{\mathrm{PLL}}/2 = 61.7\,\mathrm{MHz}$.

Once configuration of the timing generation has been done, the other peripheral modules used in the project should be configured. The PWM module configuration has been performed as follows:

- Time resolution: 1.04 ns;

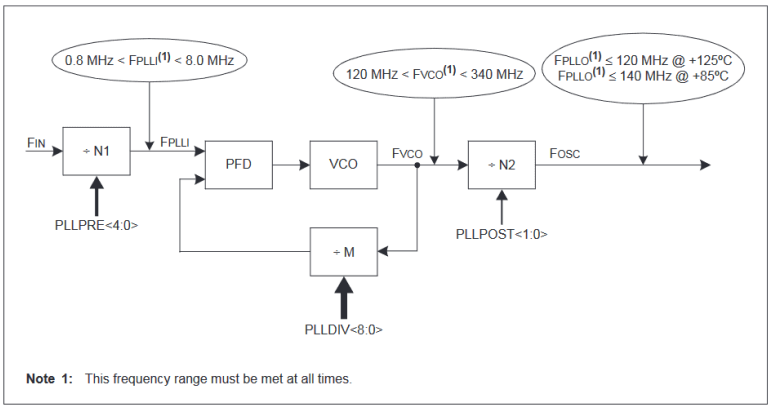

Figure 5.13: Timing generation block diagram [39].

- Period: $19230 \cdot 1.04\,\text{ns} = 20\,\mu\text{s} \;\rightarrow\; f_{\text{sw}} = 50\,\text{kHz}$;
- Modulation type: Complementary outputs;
- Dead time: $100 \cdot 1.04\,\text{ns}$;
- Enable2 PWM Special Interrupt generation.

The ADC has to be configured, too. For such a module the parameters to be set are:

- Conversion clock frequency: 120 MHz;
- Resolution n_{bit}: 12 bits;
- Type of measurement: single ended;
- Reference voltage V_{ref}: microcontroller positive supply voltage;
- Turn on and internal calibration.

In order to compute the current, the actual value for the offset voltage of the current sensing circuits is needed: when the motor is OFF, the three outputs of the current amplifier are acquired and used as reference. The conversion between the ADC output and the actual current value can be computed as:

$$I = V_{\text{ADC}} \frac{V_{\text{ref}}}{2^{n_{\text{bit}}}} \cdot \frac{1}{R_{\text{s}}} \cdot \frac{1}{\text{Gain}} \tag{5.46}$$

Once these parameters have been set, it is possible to analyze the flow charts for the motor speed control and the delay compensation loop.

5.3.2 Motor control

The speed control of the motor has been designed using two control loops: an internal current control loop, in order to control the torque and avoid overcurrents, and an external speed control loop. The control is discussed in A.4, but it is reported hereinafter for convenience. In Fig. 5.14 the control is shown.

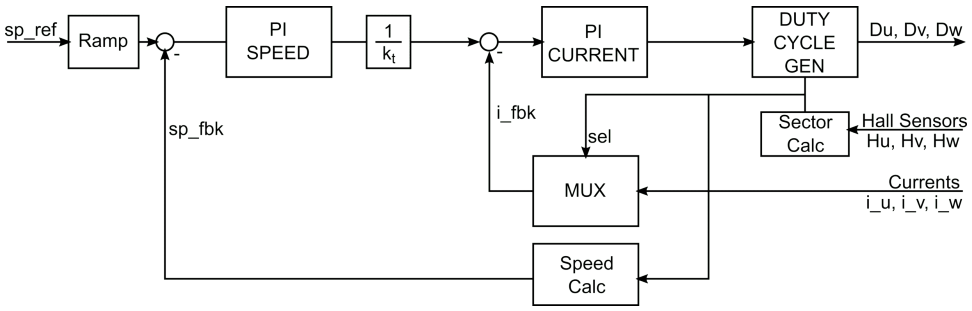

Figure 5.14: Motor speed controller.

The control acts as follows. At the beginning of each PWM period, one of the three currents I_{U}, I_{V} and I_{W} is acquired by means of the ADC. The sampled current is the one related to the active leg with the lower duty cycle, and it acts as feedback quantity for the current control loop.

The current reference value is provided by the speed controller. The speed reference is set by the user, by means of a potentiometer. The speed feedback is computed starting from the Hall sensor value variation. Since the Hall sensors indicate in which of the six steps the rotor is, when the sensors values changes it means that a rotation of 60 electric degrees occurred. Therefore the rotor speed can be computed as:

$$\omega_{\mathrm{r}} = \frac{2\pi f_{\mathrm{sw}}}{6 \cdot n \cdot p}, \tag{5.47}$$

where n is the number of PWM periods between two Hall sensor output changes and p is the number of pole pairs.

Once the speed has been computed, the outputs are configured according to the active step. The gate signals referred to the floating output are brought to low value, while the remaining two are activated. The ADC input for the current sensing is set.

Then, the current flowing in the load is evaluated. The measured current I_{m} is computed using Eq. 5.46, then the load current can be expressed as:

$$I_{\mathrm{fb}} = \frac{I_{\mathrm{m}} - I_{\mathrm{ref}}}{D}. \tag{5.48}$$

After the feedback quantities for the two control loops (rotor speed and load current) have been evaluated, the FSM driving the motor is launched. The FSM is

composed of two states: $\text{MOTOR}_{\text{OFF}}$ and MOTOR_{ON}. When the microcontroller starts to work the FSM is in $\text{MOTOR}_{\text{OFF}}$ state; in this state all the parameters controlling the motor are initialized. When the start button is pressed the FSM moves to MOTOR_{ON} state and the motor control starts to work. In this state two possible controllers can be set: the current control and the speed control. The first is composed of the current control loop only, it uses the voltage value measured from the potentiometer as current reference; the second, instead, is the complete control, made of the two control loops of current and speed. The two controller are proportional-integrative (PI) controllers. Every time the FSM is recalled and the state is equal to MOTOR_{ON}, the PI output is evaluated, according to the error, i.e. the difference between the reference value and the measured feedback quantity.

Considering the complete control, the PI parameters for the speed control loop and the ones for the current control are designed. The current PI output provides the duty cycle D to be set.

5.3.3 Delay compensation control loop

The delay compensation loop is recalled twice a period, i.e. after every output transition occurs. The input signals V_{CMp} and V_{CMn} are acquired around 300 ns from the output change event, i.e. the sampling instants are:

- First sampling instant: $t_{\text{s1}} = 300\,\text{ns}$
- Second sampling instant: $t_{\text{s2}} = D \cdot T + 300\,\text{ns}$

Therefore the sampling trigger for the ADC is changed twice a period. The data related to t_{s1} are collected directly at the start of the PWM ISR. After the collection the ADC trigger event is moved to t_{s2}, the ADC interrupt enable is set and the data are therefore collected in the ADC ISR.

The application oriented flowchart is reported in Fig. 5.16. This flowchart is the same presented in Chapter 4, but it has been structured for the microcontroller architecture and timing. As stated before the two voltages V_{CMp} and V_{CMn} are sampled in two time instants. The first sampling event stores the converted values into two variables, *CMPp_ph* and *CMPn_ph*. Once the second samples are acquired and stored in the variables *CMPp_dc* and *CMPn_dc*, the phase correction terms *corrP* and *corrN* are computed. If the phase has not yet been compensated, i.e. the measured contribution is above a minimum value (*LOW_lim*) the phase compensation procedure is carried out. Instead, if the phase is already compensated, the duty cycle compensation variables are computed and, if necessary the duty cycle compensation occurs, computing the correction *corrDC*, otherwise both the compensation terms of phase (*corrPH*) and duty cycle (*corrDC*) are zeroed. Then, such terms are summed to the active step compensation variables corr$x$.dc and corr$x$.ph.

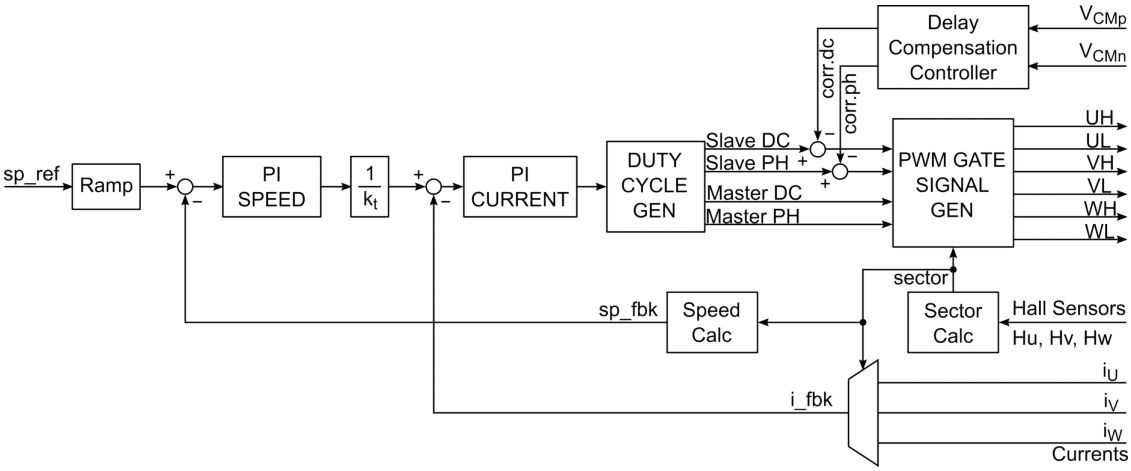

Figure 5.15: Complete control block diagram.

As last step the PWM parameters are set for the active legs as follows, where x= 1...6 is the actual step:

- Master Leg:

  Duty cycle = $D \cdot T$;

  Phase = 0.

- Slave Leg:

  Duty cycle = $(1 - D) \cdot T$ + corr$x$.dc;

  Phase = $(1 - D) \cdot T$ + corr$x$.ph.

Once the PWM ISR finishes, the microcontroller CPU returns in the main loop in which waits for another interrupt event.

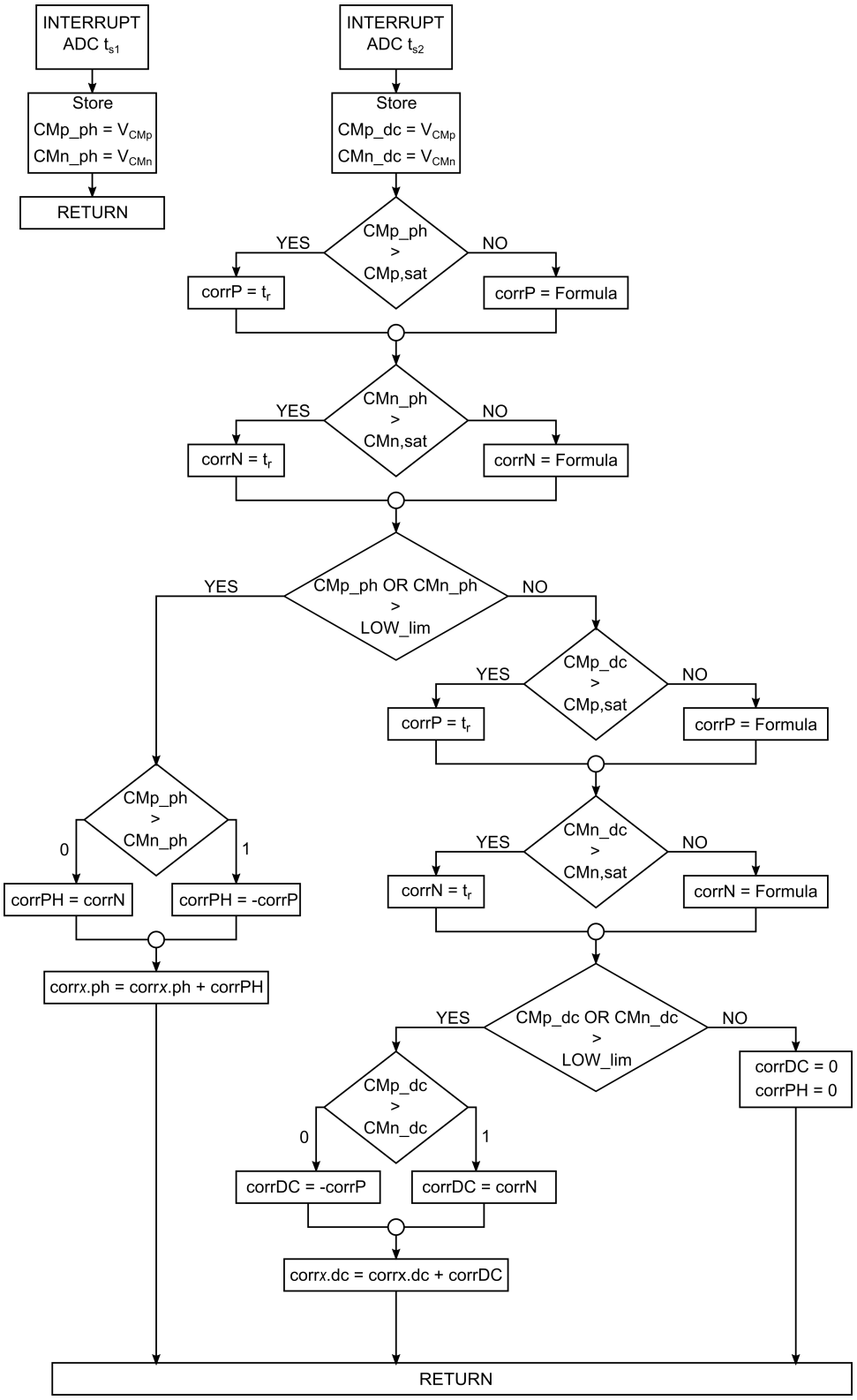

Figure 5.16: Delay compensation controller flow chart.

Chapter 6

Experimental validation

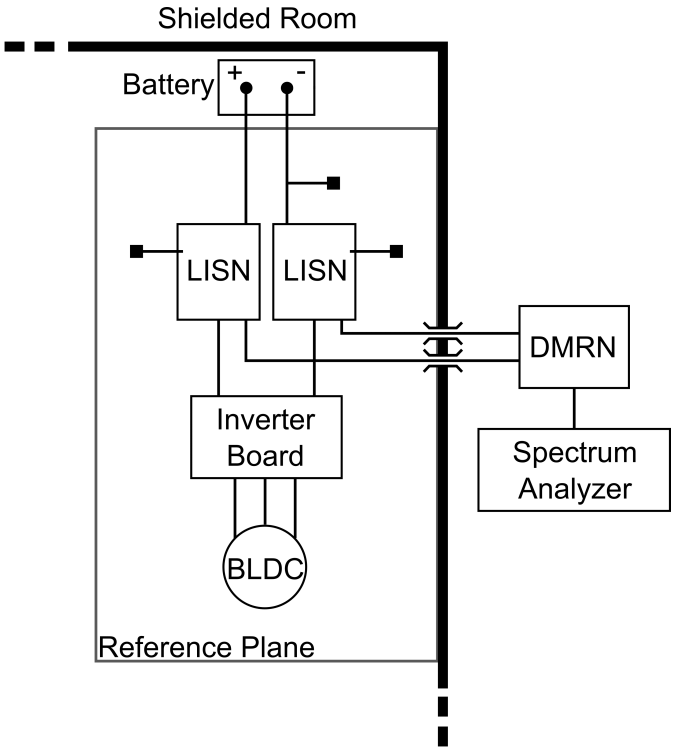

Figure 6.1: Conducted EMI test bench.

In this Chapter, the conducted emission measurements performed on the inverter prototype are presented. Such measurements are aimed to validate the effectiveness of the closed loop delay compensation technique on reducing the CM EMI.

The block diagram of the test bench used to perform the EMC tests is sketched in Fig. 6.1. The battery providing the 12 V supply voltage is connected to two

LISNs, whose chassis is contacted to a copper reference plane, as prescribed by CISPR 25 for remotely grounded equipments [3]. The BLDC driver and the load are isolated from the reference plane by means of a paper sheet and a 50 mm high wooden board, respectively. The test bench is enclosed in a shielded cabin in order to prevent the measurements to be influenced by external RF signals.

6.1 Measurement of CM emission

In Figs. 6.2 and 6.3 the test bench pictures are reported.

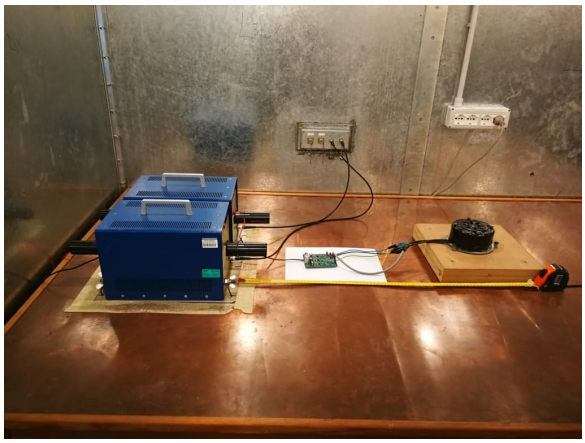

Figure 6.2: Conducted EMI test bench.

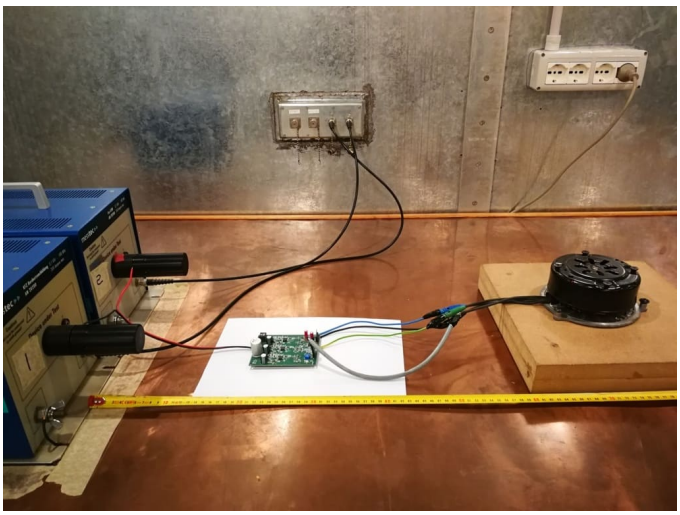

Figure 6.3: Conducted EMI test bench - Zoom.

The EMI signal at the output of each of the two LISNs is summed in order to measure only the CM voltage. The circuit used to perform such an operation

is a passive differential mode rejection network (DMRN) [7], which schematic is shown in Fig. 1.12. Ports 1 and 2 are connected to the LISN_p and LISN_n outputs, respectively, whereas port 3 is connected to a Rigol DSA815 spectrum analyzer. The V_{CM} voltage at the output of the DMRN is scaled by a factor 0.536 (-5.4 dB), which is compensated in the measurement post processing.

6.1.1 Closed Loop Delay Compensation Technique

The conducted emission measurements have been performed on the system in two cases: the first, with the delay compensation control loop is deactivated, which corresponded to $\tau_d \approx 100\,\text{ns}$; the second, where the control loop was activated, meaning with the delay compensated at each PWM period. The emission measurements have been performed in the frequency ranges 150 kHz - 30 MHz and 30 MHz - 108 MHz. The results are shown in Fig. 6.4 and 6.5.

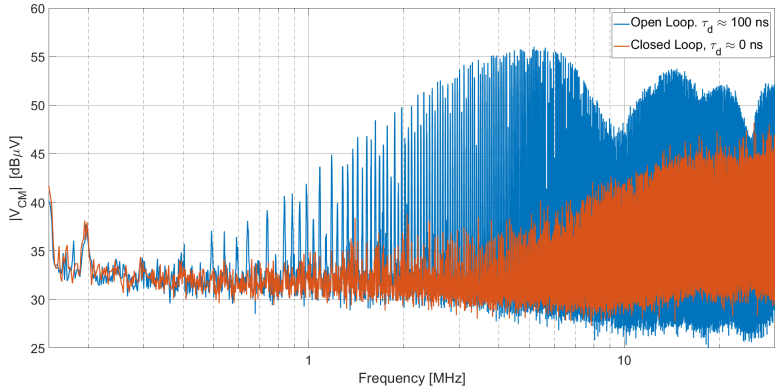

Figure 6.4: Measurement results: open loop and closed loop CM EMI spectra in the frequency range 150 kHz - 30 MHz .

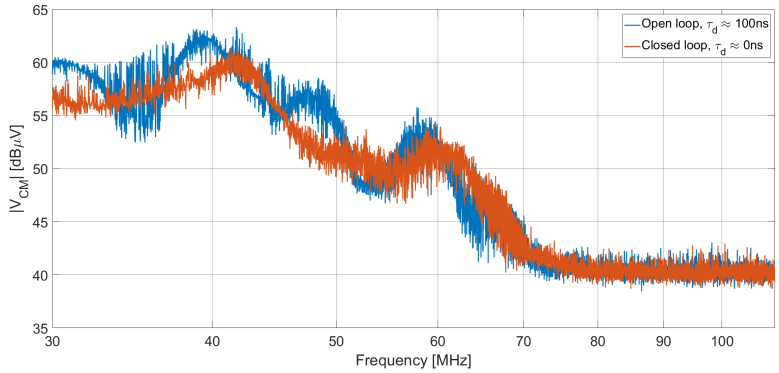

Figure 6.5: Measurement results: open loop and closed loop CM EMI spectra in the frequency range 30 MHz - 108 MHz.

It can be seen that, from 150 kHz to 30 MHz, the delay compensation control loop reduces the conducted CM EMI in the whole frequency range, with a maximum reduction of 17 dB at 4 MHz. This result has been obtained without CM filter neither at the PCB nor at the connector level.

In the frequency range from 30 MHz to 108 MHz the technique is not as efficient as in the lower part of the spectra, but the emission are not worsened. This is due to the residual delay between the outputs and to the asymmetries present between the output voltage edges.

Looking at the previous works, in particular to [27], the proposed technique reduces more the EMI level in the frequency range from 150 kHz to 30 MHz, and the reduction is achieved in less time, since the oversampling it is not needed in this case. Instead, with respect to [28], since no information on the CM spectrum is provided, the only advantage that can be highlighted is that the proposed algorithm requires less computational effort than the genetic-based one.

6.2 Effect of the motor parasitics on CM EMI

In order to evaluate the effect of the motor parasitic elements on the conducted CM EMI, which value has been measured and reported in Appendix B, the motor has been placed in three positions: the first on a 50 mm thick wooden board, the second on a paper sheet an the last directly connected to the conductive reference plane. The load is placed on a conductive sheet, as shown in Fig. B.1, in order to obtain consistent measurements. What is expected from such measurements is an increment of the conducted emission, since the parasitic capacitances grew in value with the reduction of the distance between the motor and the reference plane. The CM EMI was evaluated in the aforementioned three cases for both open loop and closed loop.

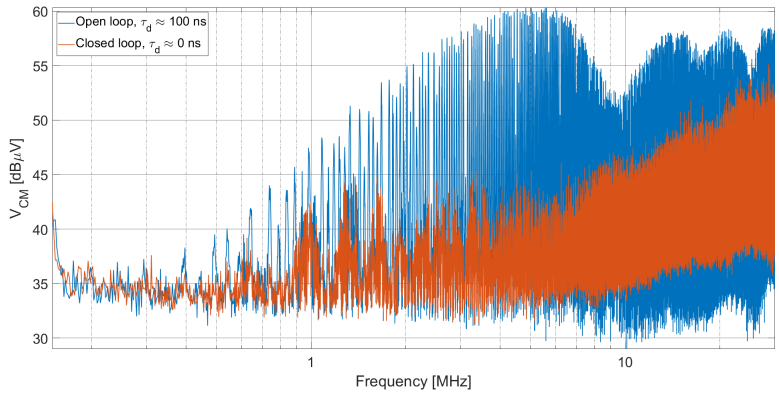

Figure 6.6: Motor placed on 50 mm thick wood, load configuration of Fig. B.1. Measurement results 150 kHz - 30 MHz.

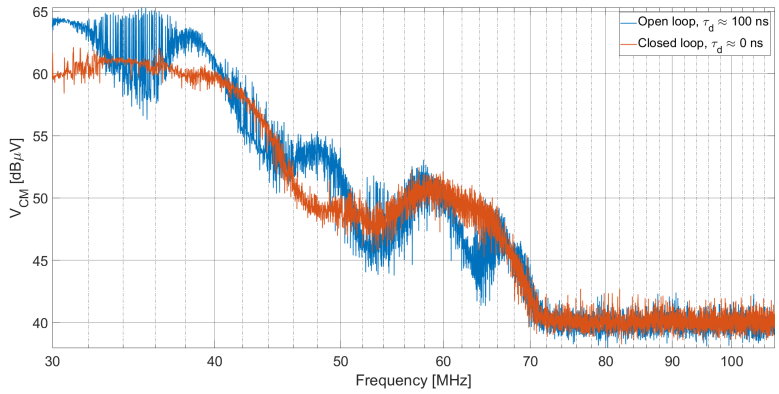

Figure 6.7: Motor placed on 50 mm thick wood, load configuration of Fig. B.1. Measurement results 30 MHz - 108 MHz.

The emission related to the first case are higher with respect to the one seen in Section 6.1, since the parasitic capacitance between the chassis and the plane has been incremented by adding the 330 mm x 170 mm conductive plane.

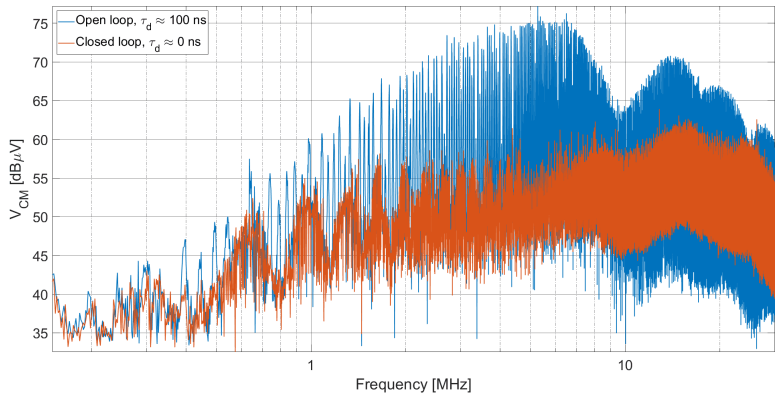

Figure 6.8: Motor placed on a paper sheet, load configuration of Fig. B.1. Measurement results 150 kHz - 30 MHz.

Considering the case of the load placed on a paper sheet, the parasitic capacitance between the motor chassis and the reference plane can be computed as:

$$C_{\mathrm{p}} = \varepsilon_0 \varepsilon_{\mathrm{rp}} \frac{S_{\mathrm{c}}}{d_{\mathrm{ps}}}, \tag{6.1}$$

where $\varepsilon_{\mathrm{rp}} = 2$ is the paper permittivity, $S_{\mathrm{c}} = (0.33 \cdot 0.17)\,\mathrm{m}^2$ is the conductive sheet surface and $d_{\mathrm{ps}} = 0.1\,\mathrm{mm}$ is the paper sheet thickness. From these data it results $C_{\mathrm{p}} = 9.9\,\mathrm{nF}$. This capacitance is in series with $C_{\mathrm{s}} = 43\,\mathrm{pF}$, so the equivalent capacitance is around 42 pF. According to this analysis, the result of this measurement is comparable with the third case, in which the chassis is connected directly on the reference plane.

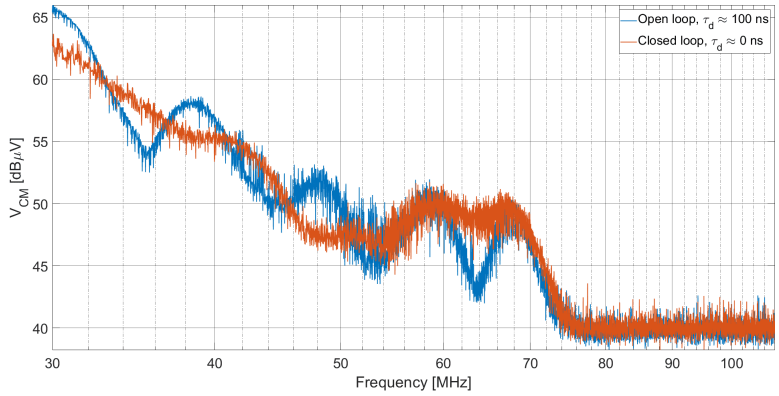

Figure 6.9: Motor placed on a paper sheet, load configuration of Fig. B.1. Measurement results 30 MHz - 108 MHz.

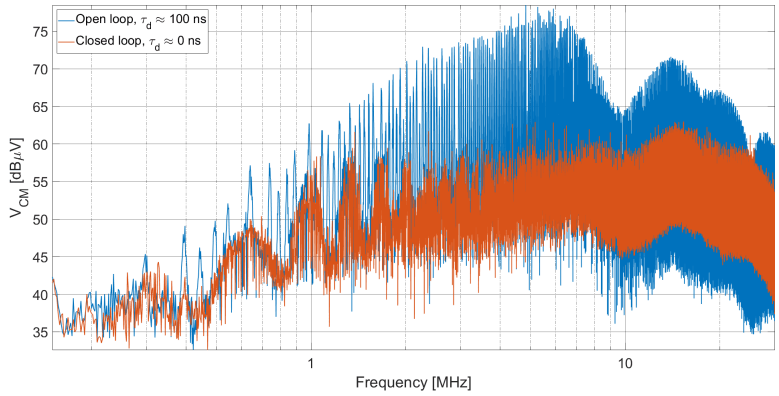

Figure 6.10: Motor chassis connected to the reference plane. Measurement results 150 kHz - 30 MHz.

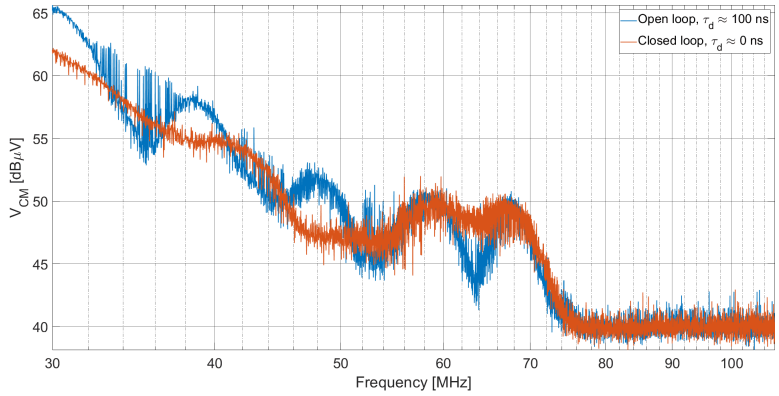

Figure 6.11: Motor chassis connected to the reference plane. Measurement results 30 MHz - 108 MHz.

From the measurements related to the third case, it turns out that the emissions are increased only by approximately 1.5 dB. This validates the hypothesis made before.

The performed measurements confirm the validity of the technique in reducing the CM EMI spectrum, independently on the parasitic element magnitude.The residual CM EMI is due to the mismatch between the parasitic capacitances related to the three phases and to the differences present between the rising and the falling times of the output waveforms. In order to mitigate the residual emissions, it is possible to add a filter, which is definitely smaller with respect to a classical power line filter. This analysis is presented in the following Section.

6.3 Power line filter reduction

The proposed technique can be used to minimize the CM EMI of bipolar PWM switched circuits. It is possible to compare the two cases in which the EMI are reduced only using a power supply filter and the one in which the power line filter is used with the proposed technique.

The power line filter is designed as explained in Chapter 2. The filter has been initially designed in order to reduce the CM EMI of the same value of the proposed technique, i.e. 17 dB at 4 MHz. In order to obtain such a reduction, the cutoff frequency has been designed to be:

$$f_{\mathrm{c,CM-OL}} = f_{\mathrm{A,CM-OL}}\sqrt{A_{\mathrm{CM,OL}}} = 1.5\,\mathrm{MHz}. \tag{6.2}$$

Therefore it is possible to compute the two components of the filter: $L_{\mathrm{CM,OL}}$ and $C_{\mathrm{y,OL}}$.

$$C_{\mathrm{y,OL}} = \frac{1}{2 \cdot 2\pi f_{\mathrm{c,CM-OL}} Z_{\mathrm{LISN,CM}}} = 2.1\,\mathrm{nF} \rightarrow 2.2\,\mathrm{nF}; \tag{6.3}$$

$$L_{\mathrm{CM,OL}} = 2Z^2_{\mathrm{LISN,CM}} \cdot C_{\mathrm{y,OL}} = 2.75\,\mu\mathrm{H} \tag{6.4}$$

The designed filter is therefore mounted at the board power supply input and the CM EMI are measured. The result is shown in Fig. 6.12.

It is possible to see that the insertion of the filter causes an increment of the CM EMI around the cutoff frequency. This is due to the high quality factor Q given by the LISNs components effect, in particular by the LISN inductances. In order to avoid that the emission limits are exceeded, the cutoff frequency should be moved at lower frequencies, at which the limit value is higher. This results in an increment of both the capacitor and CM choke values, which leads to larger physical dimensions. The cutoff frequency is so moved to 300 kHz, which means $L_{\mathrm{CM,OL}} = 12.5\,\mu\mathrm{H}$ and $C_{\mathrm{y,OL}} = 10\,\mathrm{nF}$. In order to evaluate the filter efficiency in reducing the CM EMI, the insertion loss of the filter has been derived and applied

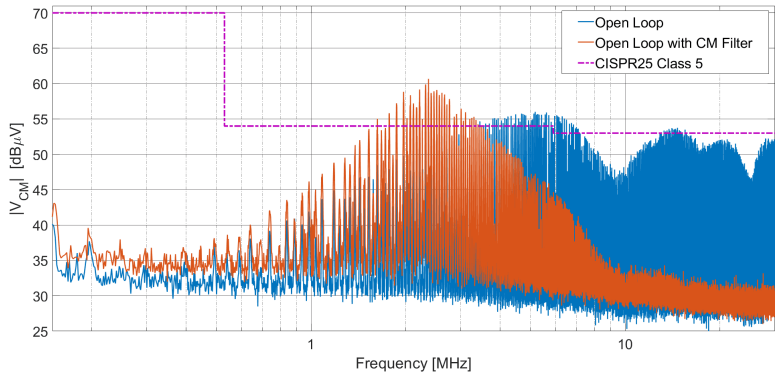

Figure 6.12: Measurement results: open loop and closed loop CM EMI spectra in the frequency range 30 MHz - 108 MHz.

to the performed measurements. The spectra obtained with this new filter are shown in Figs. 6.13 and 6.14.

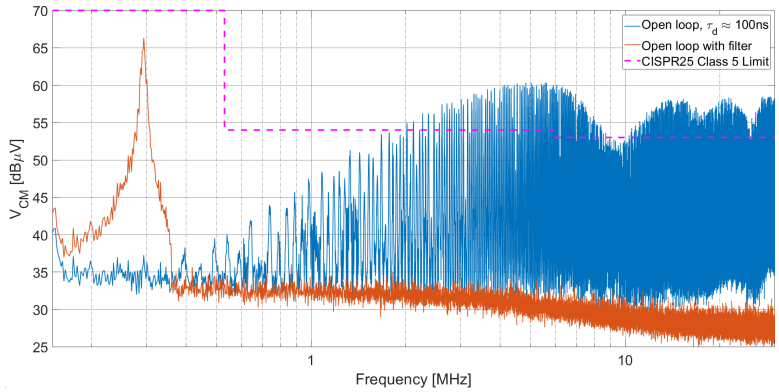

Figure 6.13: Filtering results: open loop ($\tau_{\mathrm{d}} = 100\,\mathrm{ns}$) and filtered open loop CM EMI spectra in the frequency range 150 kHz - 30 MHz.

It is possible to see that the peak due to the quality factor is higher, but the emission are within the CISPR25 Class 5 limits. However, this filter is large, and the capacitance value, if the filter is placed on the mains, exceeded the maximum C_{y} value.

The use of the proposed technique allows the reduction of the filter size, in order to lower the emissions only in the higher frequency range of the spectrum. Therefore, in order to reduce the EMI in the range 30MHz - 108 MHz, using the CISPR25 Class 5 requirements, it is necessary to reduce the CM EMI to comply with the TV Band I limit (34 dBμV from 41 MHz to 88 MHz). This means that the filter should reduce the EMI by $A_{\mathrm{CM,CL\,dB}} = 26\,dB$ at $f_{\mathrm{A,CM-CL}} = 41\,MHz$, that means:

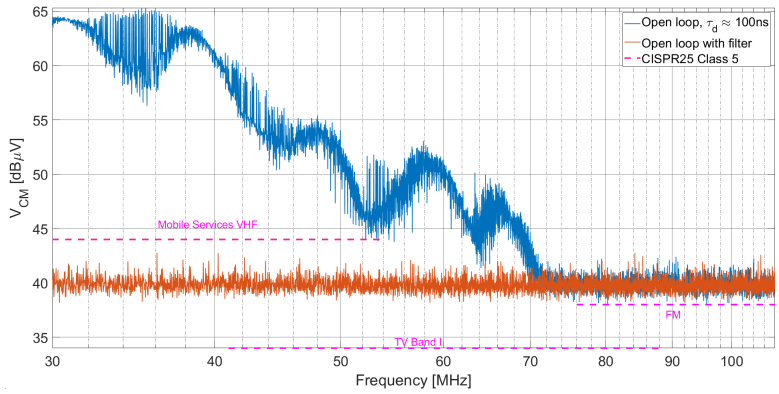

Figure 6.14: Filtering results: open loop ($\tau_\mathrm{d} = 100\,\mathrm{ns}$) and filtered open loop CM EMI spectra in the frequency range 30 MHz - 108 MHz.

$$f_{\mathrm{c,CM-CL}} = f_{\mathrm{A,CM-CL}}\sqrt{A_{\mathrm{CM,CL}}} = 9.2\,\mathrm{MHz}, \tag{6.5}$$

where $f_{\mathrm{c,CM-CL}}$ is the cutoff frequency of the CM filter for the delay control closed-loop case. The filter components are therefore designed:

$$C_{\mathrm{y,CL}} = \frac{1}{2 \cdot 2\pi f_{\mathrm{c,CM-CL}} Z_{\mathrm{LISN,CM}}} = 346\,\mathrm{pF} \rightarrow 330\,\mathrm{pF}; \tag{6.6}$$

$$L_{\mathrm{CM,CL}} = 2Z^2_{\mathrm{LISN,CM}} \cdot C_{\mathrm{y,CL}} \approx 400\,\mathrm{nH}. \tag{6.7}$$

With these two values, it is possible to derive the insertion loss of this new filter, and to estimate the behavior of the spectrum. The two spectra for both the frequency ranges, 150 kHz-30MHz and 30MHz-108MHz respectively, are shown in Figs. 6.15 and 6.16.

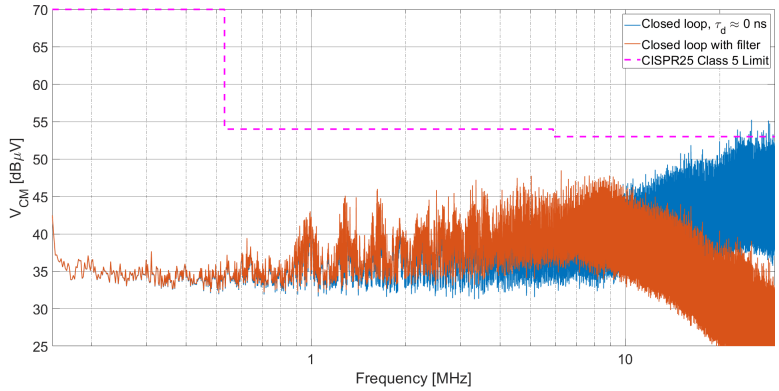

Figure 6.15: Filtering results: closed loop and filtered closed loop CM EMI spectra in the frequency range 150 kHz - 30 MHz.

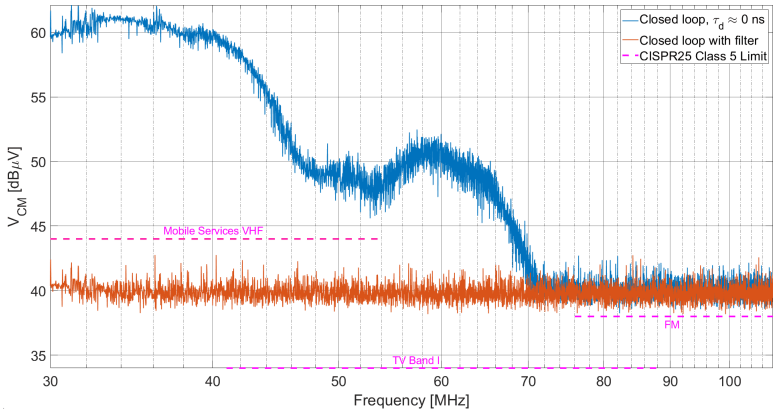

Figure 6.16: Filtering results: closed loop and filtered closed loop CM EMI spectra in the frequency range 30 MHz - 108 MHz.

Looking at the spectra 30 MHz-108 MHz, the noise floor of the spectrum analyzer used to perform the measurements is 40 dBμV, so it would not be possible to verify if the filter works also for the 34 dBμV limit indicated in CISPR25 for TV Band I.

Considering the filter occupied volume and its weight, the main contribution to these parameters is given by the CM choke. The choke dimensions are roughly proportional to its inductance. In the present case, the inductor value is reduced by a factor $k_{\mathrm{r,f}}$ equal to:

$$k_{\mathrm{r,f}} = \frac{L_{\mathrm{CM,OL}}}{L_{\mathrm{CM,CL}}} = \frac{12.5\,\mu\mathrm{H}}{400\,\mathrm{nH}} = 31.25. \tag{6.8}$$

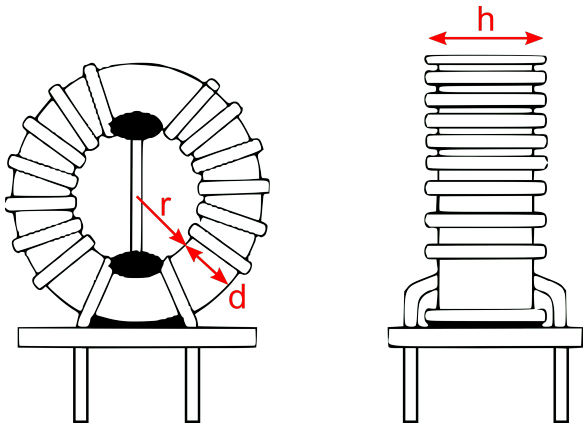

Figure 6.17: CM Choke.

The CM choke are usually made of a toroidal ferrite core, on which the two coupled inductors are wounded. A generic toroidal model is reported in Fig. 6.17. The CM inductance of the choke can be put in relation with the ferrite core volume:

$$L_{\mathrm{CM}} \propto V_{\mathrm{core}} = 2\pi(r+d)h. \tag{6.9}$$

The reduction of the inductance can be obtained reducing the spire area, i,e.:

$$\frac{L_{\mathrm{CM,OL}}}{L_{\mathrm{CM,CL}}} \propto \frac{2\pi(r+d)h}{2\pi(r+\frac{d}{\sqrt{k_{\mathrm{r,f}}}})\frac{h}{\sqrt{k_{\mathrm{r,f}}}}}. \tag{6.10}$$

This means that the inductor size is reduced approximately by a factor $k_{\mathrm{r,f}} = 31.25$. It is possible to optimize the size of the inductor, considering an appropriate reduction of the number of spires and of the core size.

In Fig. 6.18 a commercial power line EMI filter [43] is shown. It is worth underlining that this filter weights 0.9 kg and occupies a volume of (116 mm x 57 mm x 30 mm).

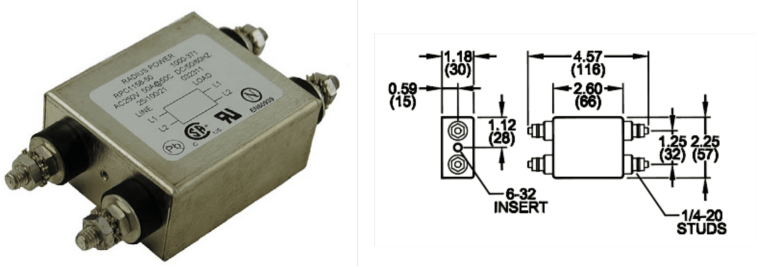

Figure 6.18: Commercial power line EMI filter.

The proposed filter, instead, can be mounted on-board. The common mode choke inductance is low, and it can be designed ad hoc. Firstly the wire is selected: according to American Wire Gauge (AWG) standard, for 50 A current, the wire that can be used is AWG 10. This wire has a diameter of 2.6 mm. Once the wire has been selected, it is possible to choose the ferrite toroidal core. The parameter used for its dimensioning is the inductance factor A_{L}. Choosing a $A_{\mathrm{L}} = 75\,\mathrm{nH/turn^2}$ core, with inner diameter equal to 12.4 mm and an outer one of 21.85 mm it is possible to derive the number of turns:

$$N_{\mathrm{T}} = \sqrt{\frac{L}{A_{\mathrm{L}}}} = \sqrt{\frac{400\,\mathrm{nH}}{75\,\mathrm{nH/turn^2}}} = 2.3. \tag{6.11}$$

The CM choke size is therefore equal to the dimensions of the toroid, plus two times the wire diameter: (12.3 mm x 27.05 mm x 27.05 mm). To this choke the filter capacitances should be added, but the overall filter dimensions are significantly lower with respect to the commercial filter presented before.

In conclusion, the proposed technique allows the designer to reduce the power line filter size, adding only few low-cost components on the PCB and a simple FSM coded on the same microcontroller used for the inverter control.

Chapter 7

Conclusion

In this thesis a new software method, able to reduce the CM conducted emission has been presented. The technique is based on the compensation of the parasitic delay between the complementary output waveforms of a switching circuit. After an initial analysis of the influence of the parasitic delay τ_d on the conducted CM emission, the compensation technique effectiveness has been verified firstly with simulations, and then by preliminary measurements. In such measurements, the technique has been implemented in open loop, i.e. the delay τ_d was compensated manually, modifying the PWM duty cycle and phase parameters. From this first test, it resulted that the proposed technique was able to reduce the CM emission of 10-15 dB maximum in the range 150 kHz-30 MHz. However, the open loop control of the delay gives non-optimal results, since in general the delay τ_d is not fixed. Indeed, the delay could vary with the temperature, the aging of the components, the working conditions of the inverter, etc. Moreover, the alignment process is time consuming and it is not practical for large scale productions.

For these reasons, a closed loop delay compensation technique has been designed. The closed loop has been obtained with simple and low cost sensing circuitry, used to acquire the instantaneous average voltage of the outputs, which is related to the CM conducted emissions, and an appropriate control software, which does not require strong additional computational effort by the microcontroller. Since only the output voltages are aligned and the dead time between the gate signals of a single leg is fixed, no cross conduction, thus no safety issues, can occur.

In order to validate the closed loop delay compensation technique, a three-phase inverter driving a 600 W BLDC motor was prototyped. The designed system included both the motor control circuitry and the one used to reduce the CM EMI. The proposed approach has been demonstrated to be effective in reducing the CM EMI up to 30 MHz, with reduction peaks of 17 dB. The delay compensation technique, unlike the SSM, reduces the energy of the CM disturbance. Since these two software techniques are independent, they could be used simultaneously, further

reducing the emission spectrum magnitude.

The use of the proposed technique allows the use of a CM EMI filter, if needed, with a cutoff frequency higher with respect to the commercial power line filters. The filter component which waists more volume is the common mode choke. With the proposed technique, its value can be reduced approximately by 31 times. The reduction in value corresponds to a reduction in volume, since less windings are needed and therefore the toroidal ferrite core can be shrank. The size reduction of the CM choke reflects a less expensive, more compact and lighter system, important characteristics in particular in automotive environments.

Appendix A

BLDC Motors

The use of electric motors for power-train purposes has gained interest in the last decade, in particular in the automotive scenario. In this field, the electric motor should work for a wide speed range; for this reason the synchronous motors are not used, although they are reliable and not expensive. Moreover, the motor should produce low torque ripple; for this reason in the automotive field the brushed DC motors are widely used. These motors, however, present some disadvantages, introduced by the brushes: brushes consumption and electromagnetic compatibility (EMC) problems, introduced by the spark generation when the phase is commutated. For these reasons, automotive companies began to use permanent magnet brushless motors, which combines the advantages of synchronous motors with the ones of DC motors.

Permanent magnet brushless motors can be divided into two main categories: Permanent Magnet Synchronous Motors (PMSM) and Brushless DC motors (BLDC). Both types are based on the same working principle, the main difference resides in their back electromotive force (BEMF), i.e the voltage generated on the windings when the rotor is forced to rotate. In PMSM the BEMF is a sinusoidal waveform, while in BLDC motors it has a trapezoidal shape. This difference comes from a different way to coil the stator windings[44].

Since the two motors are equal from the working principle point of view, it is worth underlining them pros and cons [42]. The main advantage of using a BLDC motor resides in its power density, which is 15.5% more than the PMSM one. They present lower power dissipation and their control is easy to implement when rotor position sensors are present. On the other hand, they present an higher torque ripple with respect to PMSM, but for low performance application, as automotive traction or fan driving, this is not relevant. The present work focuses on the BLDC motors.

A.1 Electro-mechanical structure

A BLDC motor is composed of a permanent magnet rotor and of wire-wound stator poles. The electrical energy is converted into mechanical energy by the attractive forces between the rotor and the excited windings.

Most of BLDC motors have three stator windings, so they should be excited by three-phase waves. Each wave is shifted in phase from the others of 120 degrees.

A.1.1 Stator and windings

The stator is the fixed part of the motor made of laminated steel. In the caves of the stator, the three phase windings are wounded. Such windings can be connected in a star pattern (Y) or in a delta pattern (Δ). The Y configuration is preferable, since it provides higher performance at a lower cost [44]. These windings represent the three motor phases, which, in order to make the motor rotate, should be excited sequentially with trapezoidal voltages. Each phase is wounded on the stator iron core with a sequence of one or more pole pairs.

A.1.2 Rotor

The rotor of a BLDC motor is made up of permanent magnets with pole pairs embedded on the surface or inside of the iron core. This magnets are made of rare-earth permanent magnetic materials, like NdFeB [44]. According to the position of such magnets, the BLDC motors can be classified as:

- Surface mounted PM rotor: the magnets are mounted on the surface of the rotor.
- Magnet-embedded rotor: the PM are inserted in specific slots present in the rotor iron core.
- Magnetic loop rotor: used in low power motors, the rotor is a rare earth permanent magnet magnetized radially.

The number of poles determines the maximum speed and the torque characteristic. An higher number of poles gives an increased torque, but at the same time leads to a reduction of the maximum speed. The flux density of the material used to construct the motor is also important for the torque characteristic. In the following section it is shown how these motors work.

A.2 BLDC motor working principle

When a BLDC motor is rotating, a voltage called Back Electromotive Force (BEMF) is generated, which opposes to the voltage waveforms driving the motor.

The BEMF magnitude depends on three main factors:

- angular speed of the motor;
- magnetic field generated by rotor magnets;
- number of turns in stator winding.

Summarizing, it is possible to say that:

$$V_{\text{BEMF}} \propto N\omega_{\text{e}} lrB \tag{A.1}$$

where N is the number of turns in the stator windings, ω_{e} the electrical angular speed, l the rotor length, r the internal rotor radius and B the magnetic field generated by the PM.

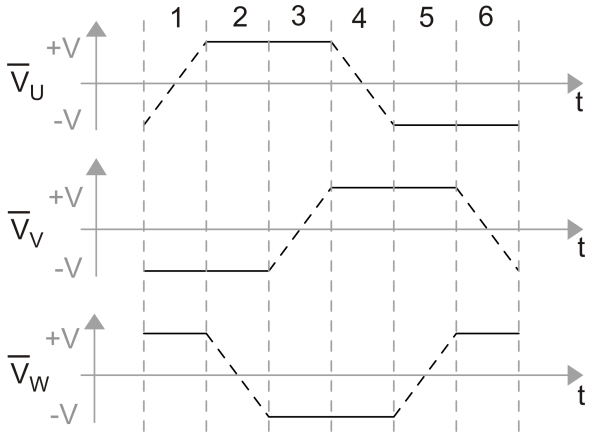

Figure A.1: BLDC motor driving waveforms.

In order to obtain the trapezoidal waveforms driving the motor, shown in Fig. A.1, the three windings are connected respectively to a positive voltage (+V), to a negative voltage (-V) and left floating (ramp) sequentially. The three voltage waveforms are shifted in phase by 120 degrees. From this diagram, it is possible to see that a single electrical rotation period can be divided in six step. In each step two out of three phases are driven by a positive and negative voltage, respectively, while the third phase is left floating, i.e. in that winding the current does not flow. The simplified model of the motor and the direction of the currents flowing in the windings for each step are reported in Fig. A.2.

In order to design the control for such motor, an electrical equivalent model should be derived. Each winding can be represented with the series of an inductor, representing the winding inductance, and a resistance, representing the ohmic losses of the windings. In addition to those components, a voltage source, representing the BEMF is present. For each step of the control two out of three phase voltages

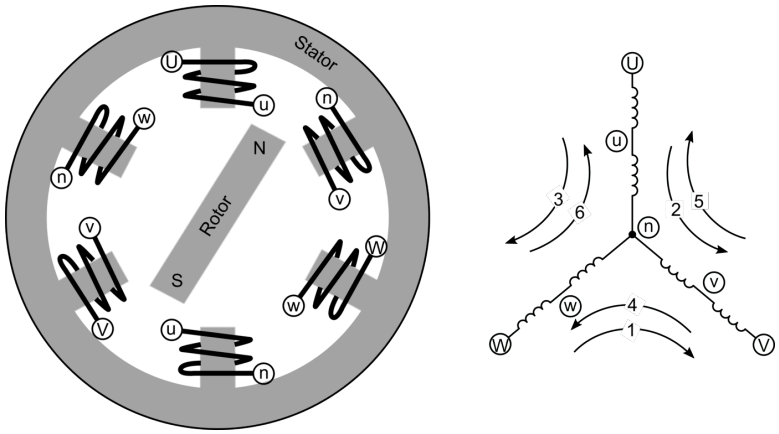

Figure A.2: Simplified BLDC motor representation with current direction for each phase.

are imposed. Such a model is shown in Fig. A.3, for the control step in which the V phase is connected to the highest voltage potential, $+V = V_{\mathrm{PS}}$, W to the lower one, $-V = 0\,V$, and U is left floating.

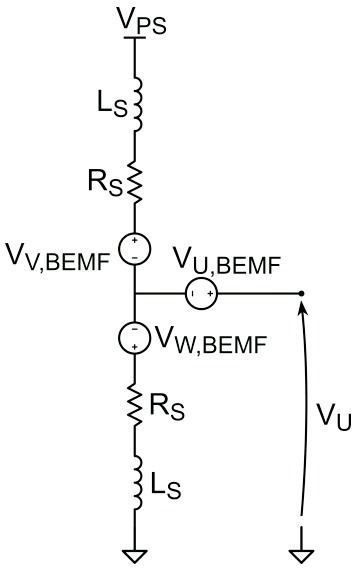

Figure A.3: BLDC equivalent circuit.

The BEMF voltage can be measured at the floating phase, whose potential is not externally imposed. This voltage, in stationary conditions, could be written as:

$$V_{\mathrm{U}} = V_{\mathrm{U,BEMF}} + \frac{[V_{\mathrm{PS}} - (V_{\mathrm{V,BEMF}} - V_{\mathrm{W,BEMF}})]R_{\mathrm{S}}}{2R_{\mathrm{S}}} - V_{\mathrm{W,BEMF}}, \qquad \text{(A.2)}$$

hypothesizing that the three windings are equal. Such a relation can be rewritten

as:

$$V_{\mathrm{U}} = V_{\mathrm{U,BEMF}} + \frac{V_{\mathrm{PS}}}{2} - \frac{V_{\mathrm{V,BEMF}} + V_{\mathrm{W,BEMF}}}{2}. \tag{A.3}$$

From this result, the value of the resistance cancels out, so it is not relevant for BEMF measurement. Since the BEMF of the two conducting phases has the same magnitude, but opposite sign, the terminal voltage of the floating phase is:

$$V_{\mathrm{U}} = V_{\mathrm{U,BEMF}} + \frac{V_{\mathrm{PS}}}{2} \tag{A.4}$$

Another important quantity to be evaluated is the motor electrical torque, T_{e}. From this electrical torque it is possible to compute the electric power P_{e} as:

$$P_{\mathrm{e}} = T_{\mathrm{e}} \cdot \omega_{\mathrm{e}}, \tag{A.5}$$

where ω_{e} is the electrical angular speed. If the winding resistances are negligible in a first approximation, i.e. there are no losses, the electrical power is totally converted in mechanical power. The electric torque can be computed as:

$$T_{\mathrm{e}} = \frac{V_{\mathrm{U,BEMF}} I_{\mathrm{U}} + V_{\mathrm{V,BEMF}} I_{\mathrm{V}} + V_{\mathrm{W,BEMF}} I_{\mathrm{W}}}{\omega_{\mathrm{e}}}. \tag{A.6}$$

Alternatively, the torque can be computed with the motion equation:

$$T_{\mathrm{e}} = T_{\mathrm{L}} + J\frac{d\omega_{\mathrm{e}}}{dt} + B\omega_{\mathrm{e}}. \tag{A.7}$$

Comparing the two expressions, and solving the equation in s domain, the angular speed of the rotor and its angular position can be computed. From the previous equations, a complete electromechanical model of the motor is derived. Two important relations for the motor control are the links between the BEMF and the rotor speed and the one between the generated torque and the current circulating in the windings. The BEMF is linked to the rotor speed by the following equation:

$$BEMF = c_{\mathrm{E}} \Phi_{\mathrm{f}} \omega_{\mathrm{e}} = k_{\mathrm{E}} \omega_{\mathrm{e}} \tag{A.8}$$

where c_{E} is the BEMF constant and Φ_{f} the excitation magnetic flux. Instead the other relation can be expressed as:

$$T = c_{\mathrm{T}} \Phi_{\mathrm{f}} I = k_{\mathrm{T}} I \tag{A.9}$$

where c_{T} is the torque constant and Φ_{f} the excitation magnetic flux [45]. The motor manufacturer provides the values of k_{E} and k_{T}, which are constant too, since for the BLDC motors Φ_{f} is almost constant. In the following section the control technique for BLDC motor is presented.

A.3 Control of a BLDC Motor

In order to drive the BLDC motor the trapezoidal voltage waveforms should be generated starting from a DC power supply. This supply voltage, V_{PS}, is generally provided by a battery. Since, as stated before, the BEMF voltage is proportional to the motor angular speed, the voltages $+V$ and $-V$ should be controlled in order to set the desired motor speed. Aiming to obtain these voltages for each step of the control, the DC power supply is modulated using PWM by means of a BLDC motor driver, usually consisting in a three-phase inverter. As stated before, two out of three legs are modulated, while the third is left floating. On the non modulated leg, the BEMF can be sensed as feedback quantity for the speed control loop.

A.3.1 Sensorless and Sensored Control

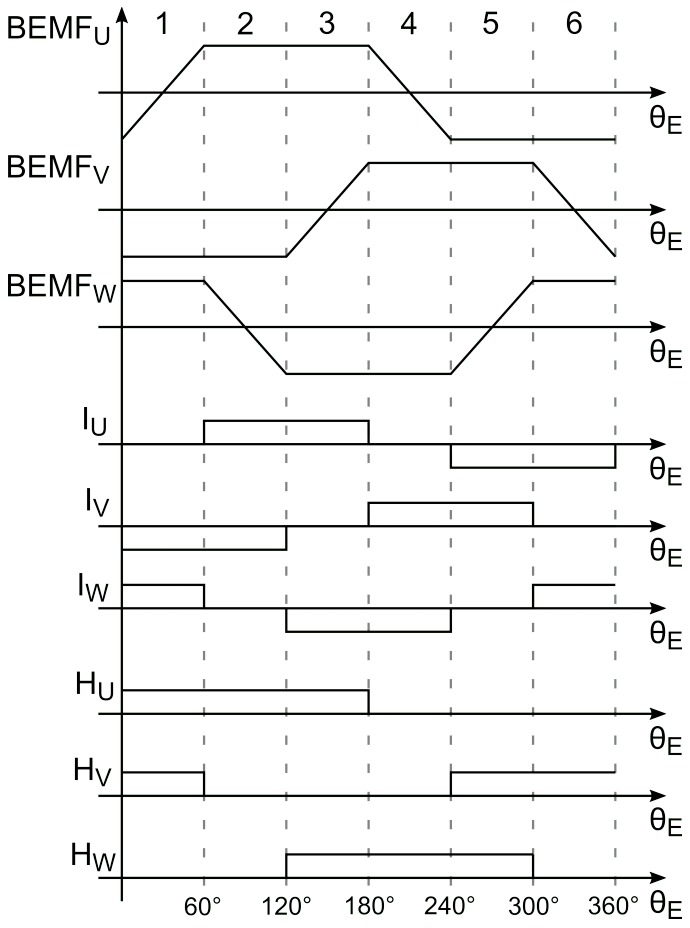

Figure A.4: BEMF, phase currents and Hall sensors outputs (for sensored motors) on the motor phases.

BLDC motors can be controlled mainly in two ways: sensorless and sensored control. In sensorless control, the feedback is the BEMF voltage of the floating output. Since a linear relation with the angular speed (i.e. the speed of the rotating magnetic field) is present, it is necessary to make the motor rotate at a minimum speed to have a measurable BEMF voltage. For this reason the motor has to be started in open loop way, and then, once almost one third of the nominal maximum speed is reached, the loop can be closed. From this speed over the BEMF voltages can be sensed without large errors. The control algorithm for this kind of control is the following: the motor speed is linearly dependent on the voltage applied, and the step changing instant can be estimated starting from the BEMF. Indeed, the step should be changed thirty degrees after the BEMF voltage sensed at the floating output crosses one half of the power supply voltage (for single supply DC EUTs), as shown in Fig. A.4. This control algorithm is advantageous because it does not require additional Hall effect sensors to estimate the rotor position; on the other hand the control is more difficult to implement, the sensed voltages can be affected by disturbances and the control is not as precise as the sensored one.

In sensored control, three Hall effect sensor are positioned in three different points of the stator, displaced one each other of 60 degrees. The presence of these sensors makes the control easier to implement, with respect to the sensorless case. The voltage waveforms driving the motor are generated through a look up table based on the sensor outputs. The relationship existing among the back EMF, the phase currents and the Hall sensors output signals is shown in Fig. A.4.

A.4 Behavioral Simulation of BLDC motor control

The control of the BLDC motor can be simulated in Matlab-Simulink [46], in order to design the controller to be implemented in the real application. The block scheme of the simulated system is shown in Fig. A.5.

The schematic is composed of a three-phase inverter supplied by a constant voltage V_{PS}. The BLDC motor is connected to the inverter outputs, and some electrical and mechanical quantities are measured from the model. The motor model is a library component of the Simulink environment, based on the electromechanical equation presented in the previous section. The inverter block used in this simulation can be configured to be behavioral, i.e. it provides the voltages +V and -V as constant tunable voltages, ot it can be configured to model a real inverter, choosing the switching devices (MOSFETs, thyristors, IGBTs, etc.). The control is behavioral, and according to the model of the inverter chosen, it provides the value of the output voltages or the gating signals for the inverter switching devices.

The feedback quantities are provided by the motor measurement ports, and they are given as input to the Digital Control block, in which resides the finite

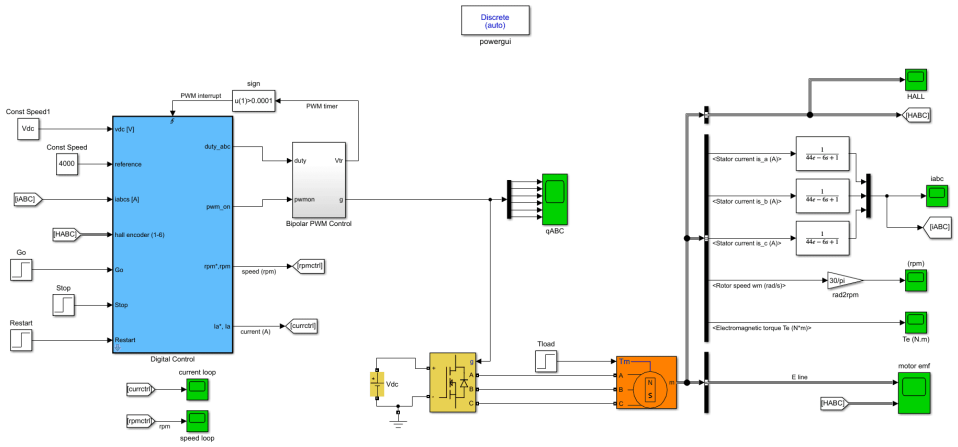

Figure A.5: Block diagram of Simulink simulation of the system.

state machine (FSM) of the system. The FSM is written in C language, allowing the re-use of the code when programming the real microcontroller.

The Bipolar PWM Control block is a behavioral representation of the hardware embedded in the microcontroller: it generates the six gate control waveform, modulated with complementary PWM. The modulation acts only on the two active legs, the on or off state for each leg is controlled by the PWM_on signal.

The signals used by the control as feedback are:

- The Hall sensors outputs, for the speed control loop;
- The three load currents for the current control loop, filtered with a low-pass filter.

The speed measurement is performed knowing that each change in the Hall sensor outputs corresponds to a rotation equal to 60 electrical degrees. The rotor electric speed, in radians, is computed as:

$$\omega_{\mathrm{r}} = \frac{\pi}{3} \frac{f_{\mathrm{sw}}}{p \cdot n} \tag{A.10}$$

where p is the number of the motor poles and n is the number of PWM periods from the previous Hall sensors value change. The control scheme is reported in Fig. A.6.

The current loop is controlled by a Proportional-Integrative (PI) controller, which has a bandwidth of $\omega_{\mathrm{a}} = 500\mathrm{rad/s}$, whose constants are:

$$k_{\mathrm{p,a}} = \omega_{\mathrm{a}} \cdot L_{\mathrm{s}} \quad , \quad k_{\mathrm{i,a}} = \frac{1}{4} \omega_{\mathrm{a}} \cdot k_{\mathrm{p,a}} \tag{A.11}$$

The speed loop is controlled by a PI too, but it has a lower bandwidth than the current one, $\omega_{\mathrm{s}} = 100\mathrm{rad/s}$, and its constants are:

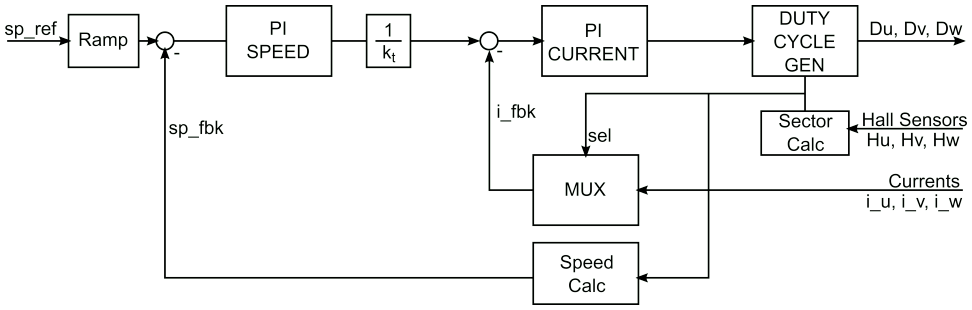

Figure A.6: Block diagram of Simulink simulation of the system.

$$k_{\mathrm{p,s}} = \omega_{\mathrm{a}} \cdot J_{\mathrm{m}} \quad , \quad k_{\mathrm{i,s}} = \frac{1}{4}\omega_{\mathrm{s}} \cdot k_{\mathrm{p,s}} \tag{A.12}$$

J_{m} is the rotor inertia, which is not known a priori. A computation based on the rotor mechanical dimensions can give an approximation of this value, as $36 \cdot 10^{-6}\mathrm{kgm}^2$.

The speed reference of the control system is given as input to a slew rate limiter, the "Ramp" block, in order to limit the inrush current into the motor phases. An acceleration limit of 50 krpm/s has been imposed. The simulation results are shown in the following graphs.

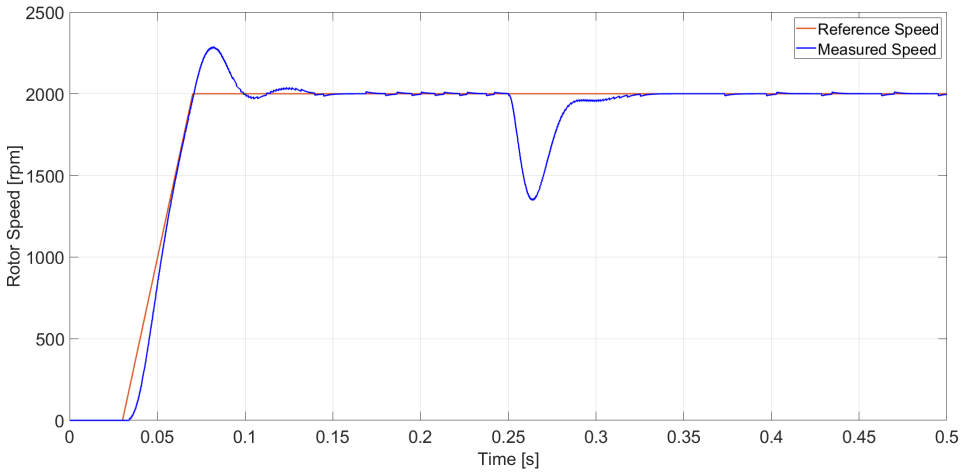

Figure A.7: Reference speed Vs rotor speed.

The speed overshoot is around 10% of the reference value, which means that the phase margin is around 60 degrees.

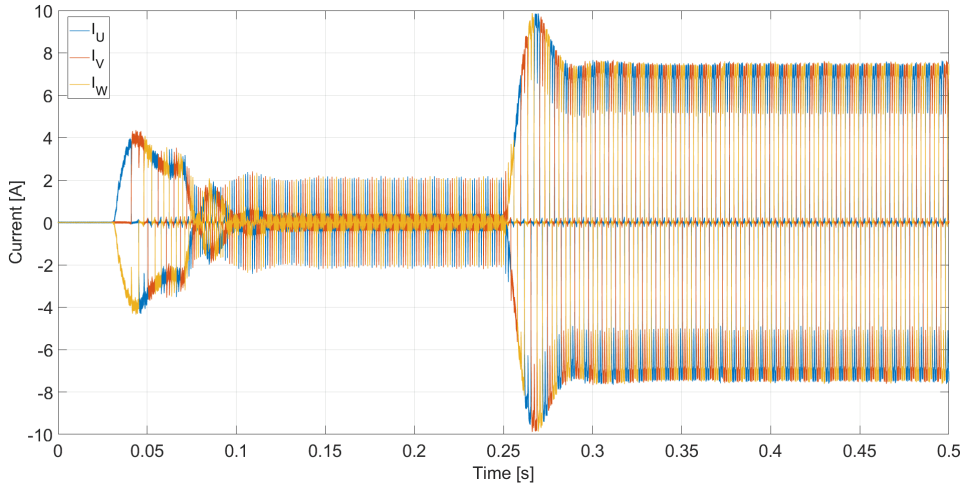

Figure A.8: Phase currents.

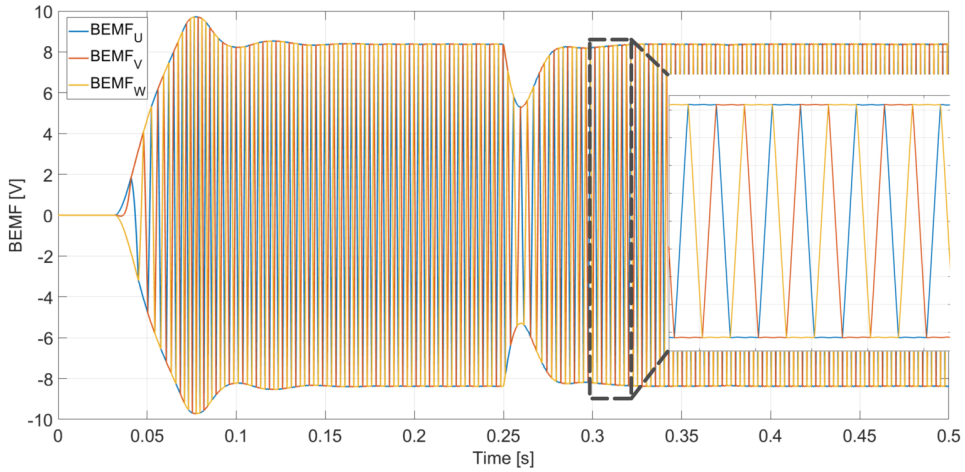

Figure A.9: BEMF.

Appendix B

Characterization of the load parasitics

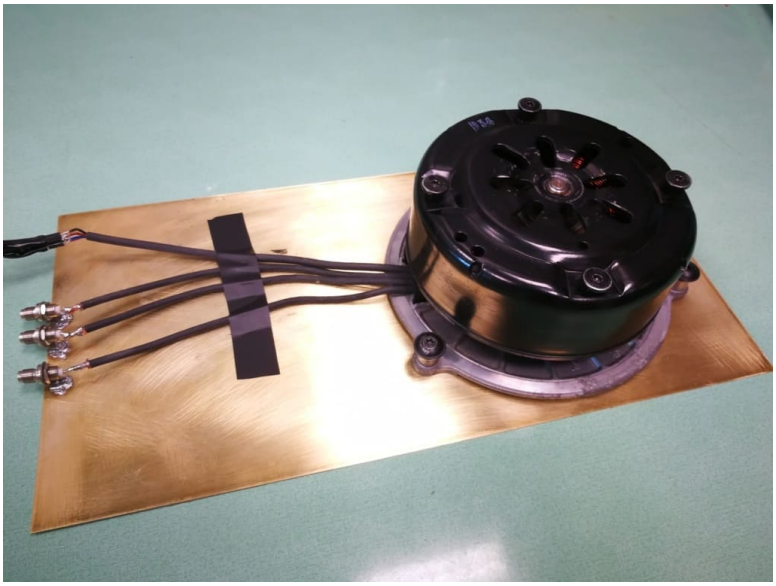

Figure B.1: Motor parasitics measurement test setup.

The load used for the measurements, as presented in Chapter 5, is a 600W BLDC motor, which has been characterized only with its functional parameters. In order to evaluate the effect of the load on the conducted EMI propagation, an high frequency model of the motor is needed. Such a model is obtained from measurements, performed with a Keysight E5080A 4-port network analyzer. In order to perform such a characterization, the motor has been placed on a 170 mm x 330 mm conductive plane, and three 3.5mm SMA connectors have been soldered between each motor phase cable and the plane, as shown in Fig. B.1. Such a test setup aims to evaluate the high frequency phase inductances L_{pw}, their parallel

parasitic capacitances C_{pw}, the parasitic capacitance present between the phases and the chassis, C_{s}, and the cable parasitic inductances L_{c}. The schematic of the model is shown in Fig. B.2.

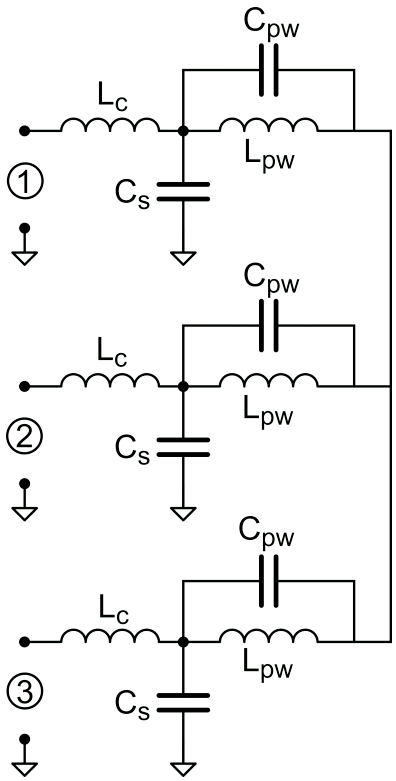

Figure B.2: High frequency motor model for EMC purposes.

Since the network analyzer produces reliable measurement results starting from 100 kHz, the **S**-matrix has been evaluated in the range 100 kHz-100 MHz. The measurement result of the three-port characterization is reported in Fig. B.3. For convenience, the **S**-matrix has been converted into a **Z**-matrix, which is reported in Fig. B.4. The motor shows a symmetric behavior in the low frequency range, while in the high frequency one it is asymmetric.

In order to evaluate the phase inductance, ports 1 and 3 have been loaded with a short circuit, nulling the C_{s} parasitic capacitances effect, and a C_{t} =10 nF capacitor has been placed in series to port 2.

The impedance measured with the VNA is shown in Fig. B.6. The measured capacitance is $C_{\mathrm{t}} = 9.32\,\mathrm{nF}$ and looking at the first series resonance frequency of the measured impedance, $f_{\mathrm{rs1}} = 364\,\mathrm{kHz}$, the total inductance can be evaluated:

$$\frac{3}{2}L_{\mathrm{pw}} = \frac{1}{C_{\mathrm{t}}(2\pi f_{\mathrm{rs1}})^2} \rightarrow L_{\mathrm{pw}} = 13.7\,\mu\mathrm{H}. \tag{B.1}$$

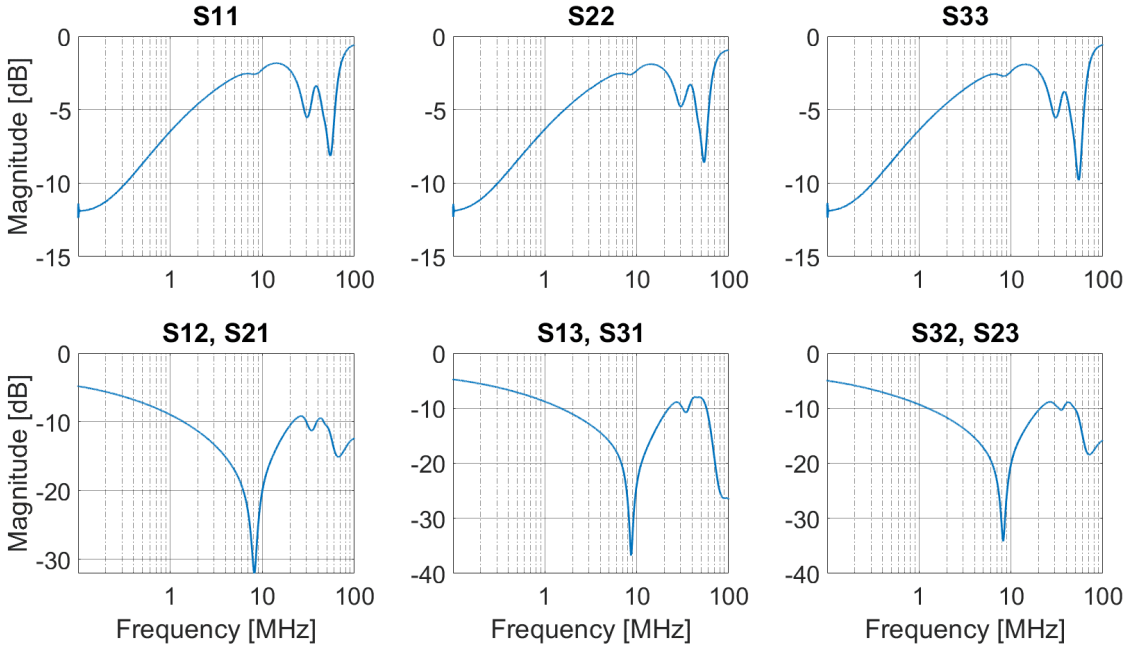

Figure B.3: Measured **S**-matrix.

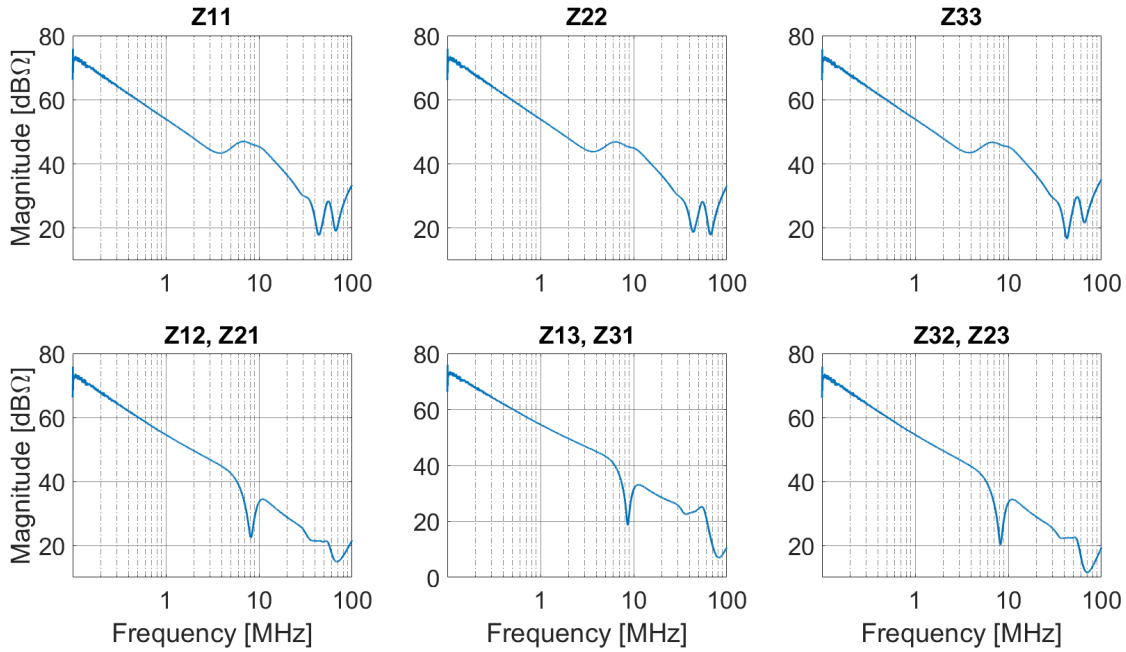

Figure B.4: Measured **Z**-matrix.

From the parasitic inductance, it is possible to evaluate, looking at the first

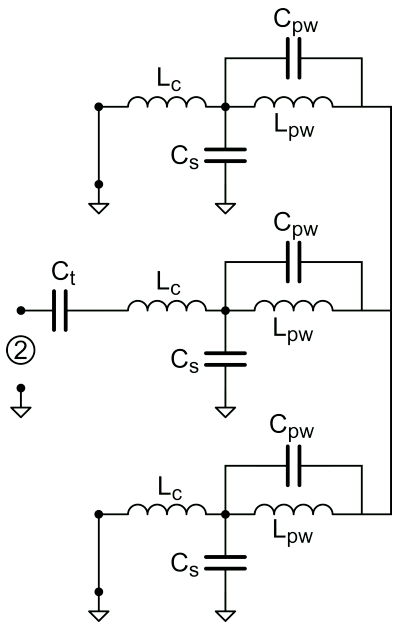

Figure B.5: Test bench.

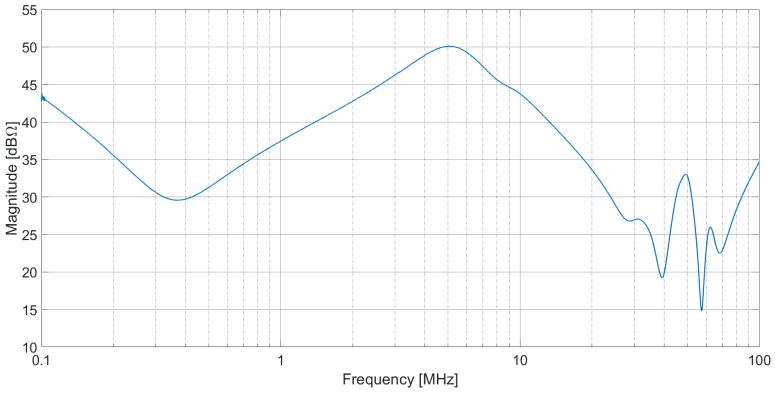

Figure B.6: Port 2 Impedance according to the test bench of Fig. B.5.

parallel resonance peak, $f_{\mathrm{rp1}} = 5\,\mathrm{MHz}$, the total parallel parasitic capacitance C_{tot}:

$$C_{\mathrm{tot}} = \frac{1}{L_{\mathrm{pw}}(2\pi f_{\mathrm{rp1}})^2} \rightarrow C_{\mathrm{tot}} = 49\,\mathrm{pF}. \tag{B.2}$$

The second series resonance, located around $f_{\mathrm{rs2}} = 40\,\mathrm{MHz}$, is due to the cable inductance and the total parasitic capacitance. From this frequency it is possible to evaluate L_{c}:

$$L_{\mathrm{c}} = \frac{1}{C_{\mathrm{tot}}(2\pi f_{\mathrm{rs2}})^2} \rightarrow L_{\mathrm{c}} = 330\,\mathrm{nH}. \tag{B.3}$$

The last evaluation consist in the separation of C_{tot} between its components, C_{s} and C_{pw}. This evaluation has been performed considering two cases: the one seen before, with both port 1 and port 3 short-circuited, and the case in which the differential impedance between port 1 and port 2 is evaluated, while port 3 is grounded. The equivalent circuits for the two cases are shown in Fig. B.7 and the resulting impedances are reported in Fig. B.8.

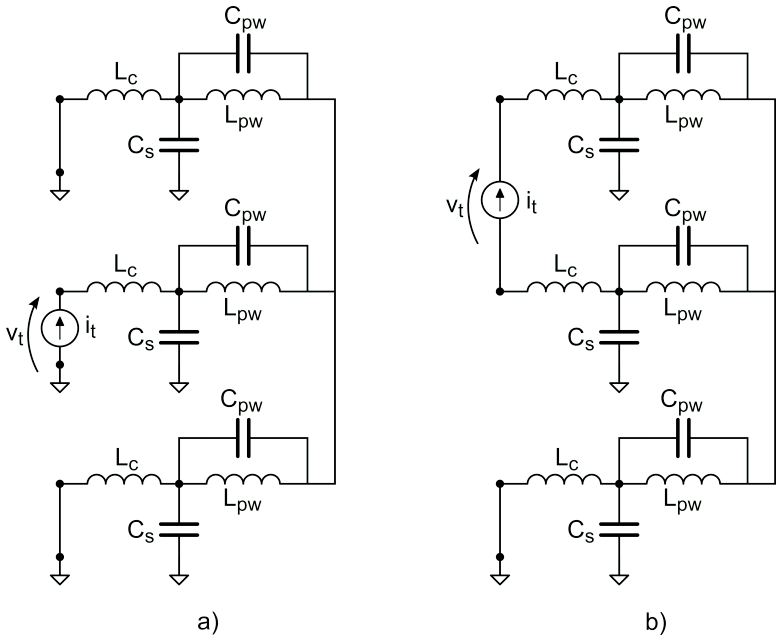

Figure B.7: Test bench for the evaluation of C_{s} and C_{pw}.

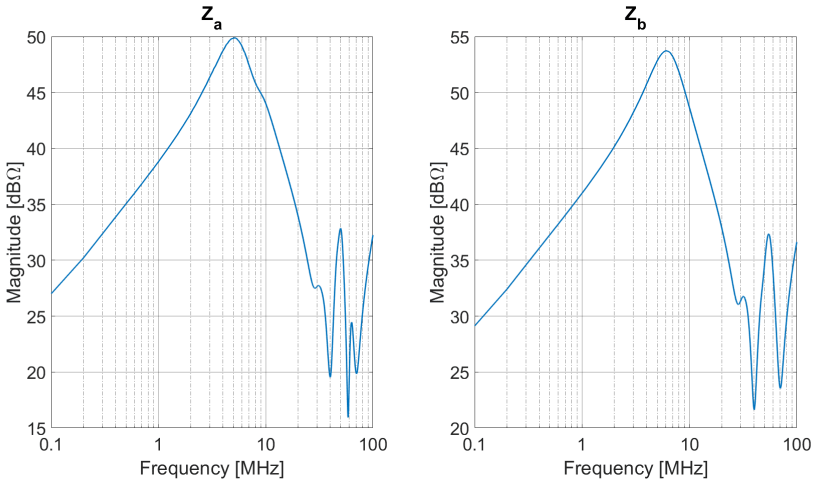

Figure B.8: Resulting impedances for the test benches of Fig. B.7.

Table B.1: Model Parameters

Parameter	Value
L_c	330 nH
L_{pw}	13.7 μH
C_{pw}	9 pF
C_s	43 pF

In the first case, it is possible to evaluate the total parasitic capacitance as seen in Eq. B.2. Therefore, C_{tot} can be expressed as:

$$C_{tot} = \left(C_s + \frac{2}{3}C_{pw}\right) = 49\,\text{pF}. \tag{B.4}$$

For the second case, the parallel resonance frequency moves up to $f'_{rp1} = 6\,\text{MHz}$:

$$C'_{tot} = \frac{1}{2L_{pw}(2\pi f'_{rp1})^2} \rightarrow C'_{tot} = 26\,\text{pF}, \tag{B.5}$$

where:

$$C'_{tot} = \left(\frac{C_s}{2} + \frac{C_{pw}}{2}\right) = 26\,\text{pF}. \tag{B.6}$$

From Eq. B.4 and Eq. B.6 it is possible to derive:

$$C_s = 43\,\text{pF}, \qquad C_{pw} = 9\,\text{pF}. \tag{B.7}$$

The component values of the model presented in Fig. B.2 are summarized in Tab. B.1.

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