POLITECNICO DI TORINO
Repository ISTITUZIONALE

In-Circuit Mitigation Approach of Single Event Transients for 45nm Flip-Flops

Original
In-Circuit Mitigation Approach of Single Event Transients for 45nm Flip-Flops / Azimi, Sarah; De Sio, Corrado; Sterpone, Luca. - ELETTRONICO. - (2020), pp. 1-6. ((Intervento presentato al convegno 26th IEEE International Symposium on On-Line Testing and robust System Design (IOLT 2020).

Availability:
This version is available at: 11583/2842252 since: 2020-08-04T10:25:20Z

Publisher:
IEEE International Symposium on On-Line Testing and robust System Design

Published
DOI:

Terms of use:
openAccess

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

20 October 2021

In-Circuit Mitigation Approach of Single Event Transients for 45nm Flip-Flops

Sarah Azimi, Corrado De Sio, Luca Sterpone

Dipartimento di Automatica e Informatica
Politecnico di Torino
Torino, Italy

***Abstract*— Nowadays, radiation-induced Single Event Transients are a leading cause of critical errors in CMOS nanometric integrated circuits. In this work, we propose a workflow for analyzing and mitigating nanometric CMOS integrated circuits to radiation-induced transient errors. The analysis phase starts with the developed Rad-Ray tool for mimicking the passage of the radiation particles through the silicon matter of the cells to identify the features of the generated transient pulses. The tool is integrated with an electrical simulator to evaluate the dynamic behavior of the transient pulses inserted and propagated in the circuit. A tunable mitigation solution is proposed by inserting the filtering block before the storage element, tuned based on the duration and amplitude of the expected transient pulse, identified in the analysis phase. Experimental results are achieved by applying the proposed approach on the 45 nm Flip-Flop component available in the FreePDK design kit, comparing the Dynamic Error Rate for the original Flip-Flop and the mitigated one which shows a reduction of sensitivity up to 56% with respect of the original version, with negligible degradation of performances.**

***Keywords*— Single Event Transient, Flip-Flop, Circuit Design, Mitigation.**

I. INTRODUCTION

Due to technology scaling, increasing the density of transistors, and reduction of the critical charge of the cells, logic designs are becoming more vulnerable to Soft Errors [1]. When a charged particle interacts with a device, it may cause a voltage pulse known as Single Event Transient (SET). If the generated pulse arrives at the storage element such as Flip-Flops (FFs) during its latching window, incorrect data can be stored resulting in Single Event Upset (SEU). The generated SEU might propagate to the output of the circuit, causing errors and malfunctioning of the system. As today's technology continuously scales down, circuits become increasingly more vulnerable to SET. Due to the reduction of a node capacitance, a radiation particle with lower energy can create a voltage pulse in the circuit. On the other hand, the increasing of the clock frequency of recent circuits leads to a higher probability of SET pulses being captured by the storage elements. However, If the SET pulse does not carry sufficient amplitude and width, it will get attenuated as it propagates, and it will not be sampled by the storage element. This effect is known as Electrical Masking [2]. Though, due to the scaling down of devices, the effect of electrical masking is reduced, and the probability of SET being sampled by storage element increases [3].

Flip-Flops (FFs) are also influenced by the scaling down of technology, optimization of speed and power which lead to an increase of the sensitivity versus soft errors. Therefore, the sensitivity of these components should be studied in detail in order to reach an efficient mitigation technique.

The main contribution of this work is to propose a framework for analyzing the vulnerability of nanometric circuits to radiation-induced transient errors and mitigating the generated transient pulse by adding the filtering block, which is tuned based on features of the pulse, generated and propagated to the storage element. This approach is based on a toolchain composed of our developed tool, Rad-Ray, which is able to mimic the effect of radiation particle interacting within a given device, computing the effectively generated SET pulses with consistent amplitude and duration in relation to the particle strike and the location of the generated pulses. The tool is integrated with commercial electrical simulation tool, HSPICE, that allows to inject SET pulses in the sensitive nodes of the circuit identified by Rad-Ray and evaluate the dynamic behavior of the pulse propagating through the circuit, reporting the dynamic failure rate and the SET pulses which creates the failure of the circuits knowing as critical SETs. A tunable mitigation solution is proposed which acts by inserting the filtering blocks consisting of pass transistors before the storage elements. The size of the pass transistors is tuned with respect to the SET pulse reaching the storage element, identified by the analysis phase. The filtering block acts by reducing the amplitude of the transient pulse, lowering the probability of the pulse being captured by the storage element. Therefore, reducing the Soft Error Rate (SER) while the area and performance overhead are negligible.

This paper is organized as follows: Section II is dedicated to reviewing the related works. Section III describes the developed workflow in detail. Section IV elaborates on the experimental results, applying the workflow to the 45 nm Flip-Flop using FreePDK physical library. Finally, Section V reports the conclusion and future works.

II. RELATED WORKS

Several works studied the sensitivity of different FF designs to radiation-induced soft errors [4][5]. In [6], the authors report the neutron-induced and alpha-particle-induced SER of 14 different Flip-Flops designs fabricated in a 40 nm bulk CMOS technology node. The result shows the increase of the SET in all the FFs with a reduction in the supply voltage and ambient temperature.

The mitigation of Single Event Transients has taken on growing importance as transistor size has decreased. In general, these mitigation techniques act on filtering or vanishing the deposited charge or use some sort of redundancy technique to prevent corrupting data [7]. Researchers have also proposed techniques based on low pass filter characteristics of transmission gates in protecting against radiation transients [8][9]. In [10], researchers used the low pass filtering characteristic of the transmission gate for reducing the SET rate. It was shown that the magnitude of a SET pulse can be reduced before it is passed on the next stage while the main signal passes with little change. In [8], it was claimed that a two stages transmission gate configuration makes the technique the most efficient when the size of the second stage transistors is larger than the first one. The work in [13] proposed a tunable transient filter design that achieved a better filtering characteristic, while [9] demonstrated that a new filter gates scheme with varied gate voltage offered improved SET filtering characteristics when compared to basic filter gates. However, even though these studies [12] provide efficient mitigation techniques, they are not tuned with respect to the radiation profile of the mission and the prediction of SET pulses.

III. The Analysis and Mitigation Workflow

In order to analyze the sensitivity of a circuit to SET and mitigate the propagated SET pulse, we developed a workflow consisting of analysis and mitigation phases. The analysis phase, represented in Figure, 1 starts with developing an electrical model of the circuit under analysis. The electrical netlist and the layout are provided to the developed Rad-Ray tool to perform a radiation analysis and compute the characterization of expected SET pulses with respect to the radiation profile and layout of the circuit under the test. The core of this stage is related to the Monte Carlo based radiation analysis tool which is able to generate the radiation-induced SET effect on the basis of the technology and layout of the analyzed circuit. The estimated SET distribution is used in the electrical fault injection environment. The commercial electrical simulation tool, HSPICE, is used to inject SET pulses generated by Rad-Ray in a sensitive node of the netlist identified and to evaluate the impact of the SET pulses on the functionality of the circuit in terms of Dynamic Error Rate. The mitigation phase acts by inserting a filtering block consisting of a pair of pass transistors before the sensitive storage elements. The filtering block reduces the amplitude of the transient pulses. The amount of reduction is dependent on the size of the transistors. Therefore, by tuning the size of the pass transistors, it is possible to filter SET pulses with different amplitudes. This workflow has been applied to a Flip-Flop as an important component of data path design. However, it is possible to apply the workflow to any circuits with different technology. When the FF is used for circuits applied in space applications, as an effect of radiation particle interaction, SET pulses can be generated in the internal transistors composing a FF. The generated SET pulse is propagating until the output of the FF and it can temporarily alter its logic value that can be sampled by the consequent FFs at the sampling window triggered by the clock signal. Even if the generated pulse is not happening during the device clocking period, it appears in the output of the FF along with the main signal. The pulse in the output of the FF may propagate to the output of the circuit and generate an error in the functionality of the circuit.

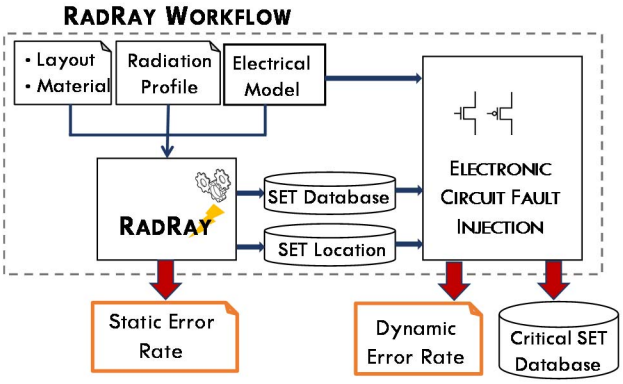

Figure 1. The scheme of developed radiation effect analysis workflow.

A. Rad-Ray Radiation Analysis

As a first stage, we considered the electrical HSPICE model of the FF type D included in the FreePDK 45 nm design library. The layout description of the circuit has been extracted in terms of Graphic Data System-II (GDS-II). The GDS file is the result of the circuit design and it is the file provided to the foundries for the fabrication of the IC. Rad-Ray is an in-house developed tool for simulating the passage of radiation particles through the silicon matter of modern integrated circuits and generating the transient voltage pulse response. The tool receives the netlist and layout of the circuit under the study, together with the layer material and depth of each layer and the radiation profile of the mission as inputs.

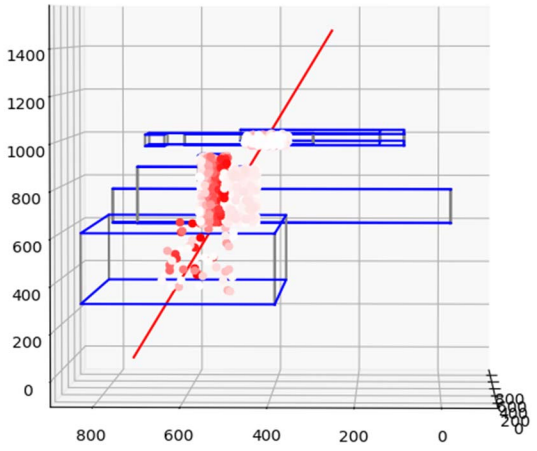

Figure 2. A Heavy-Ion track releasing charge during its propagation. Colored spots provide the value of the corresponding released charge distributed for each cell volume. The unit of all axes is Å.

Rad-Ray starts with the GDS-II of the circuit and generates the 3D mesh structure of the layout of the circuit. Based on the size and shape of metallization and volumes of the cells with respect to the radiation profile of the mission which includes the type of the ions existing in the environment under the study, the energy and the flux of the particles, the tool simulates the effects

of highly charged particles traversing the silicon junction of the device.

The produced free mobile carriers are concentrated within the depletion region of a p-n junction in the transistor sensitive parts individuated by the Rad-Ray algorithm. The eV transmitted by the particles, depending on the traversed section of the cell, can cause a voltage glitch that is propagated to the output of the transistor and finally to the output of the cell, generating a SET effect into the circuit. Rad-Ray mimics the track passage of ion ray by generating a list of starting and ending coordinates of each particle and calculates the amount of energy loss during this passage in each node.

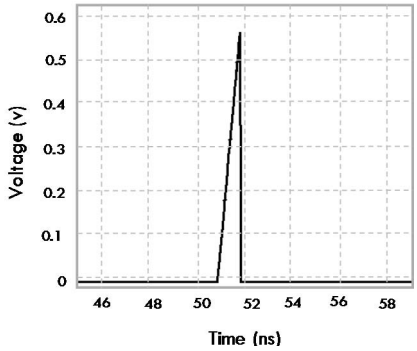

Figure 3. The outcome of Rad-Ray method visualized thanks to the H-Spice simulation and related to a single particle strike within the cell under the analysis.

Figure 2 shows the heavy ion releasing its energy during the propagation in the cells. The propagation of particles terminates by reaching to the final coordinates. Finally, the Rad-Ray tool converts the transmitted energy in Volts and plots the Voltage value of each cell. Figure 3 represents the generated SET pulse within the cell under the analysis. The result is a report which elaborates the generated transient pulse in terms of duration and amplitude of the voltage pulse at the output of the analyzed cell. More details about Rad-Ray algorithm are provided in [11]. As a next step, Rad-Ray is linking the affected cell to the netlist of the circuit and identifying the affected transistor node in the circuit netlist. At the end of the Rad-Ray elaboration, all the affected transistors nodes and the features of the generated SET pulse affecting the transistors are identified.

B. Electrical Fault Injection

The generated SET database has been provided to the next stage of the workflow to develop an electrical SET fault injection environment. As has been mentioned, as a result of Rad-Ray analysis, the generated SET pulses, in terms of duration and amplitude, and the locations where the pulses have been generated are characterized. This information has been used for the electrical fault injection environment to evaluate the effect of the SET pulse on the dynamic behavior of the FF.

To emulate the SET pulse, the original netlist of the FF has been modified automatically, inserting a transient voltage source connected to the affected node of the transistor in the netlist corresponding to the physical location identified by the Rad-Ray tool in the previous stage. The inserted transient voltage source has the same duration and amplitude of the SET pulse generated by the Rad-Ray physical analysis. Figure 4 represents a sensitive transistor identified by Rad-Ray. A radiation particle hits the source terminal of the transistor and generates a SET pulse with the duration of 550 ps and amplitude of 0.8 V. The electrical model has been modified and the SET pulse has been added to the source terminal of the transistor in terms of a transient voltage source. The same flow has been followed for each SET pulse reported by Rad-Ray. The netlist has been modified by adding the voltage source in the transistor node affected by the radiation particle.

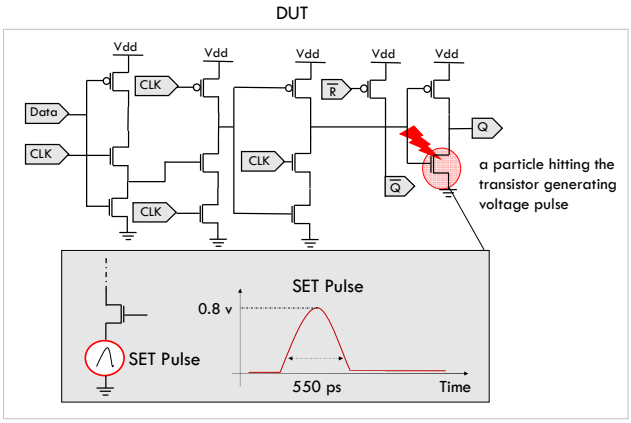

Figure 4. An example of emulation of a transient pulse with a duration of 550 ps and amplitude of 0.8 V in the source of the transistor identified by the Rad-Ray tool.

The inserted SET pulse may propagate to the output of DUT. In order to verify whether the propagated SET in the output of the DUT is sufficient to propagate until the output of the circuit and create an error, we designed a setup represented in Figure 5.

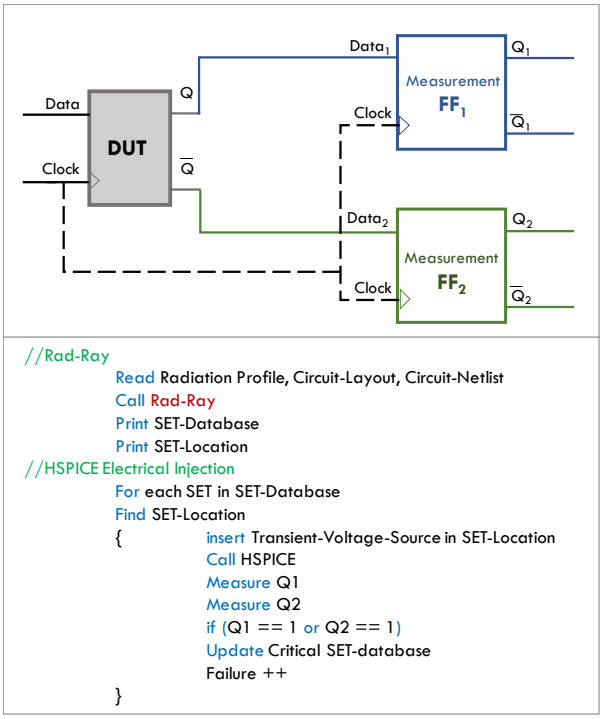

Figure 5. A developed setup to evaluate whether the generated SET pulse inside DUT is propagated and sampled by the following storage element.

When a SET pulse is generated inside the DUT (i.e. FF), it propagates to its outputs. However, depending on the location

of the incident and internal transistor that has been affected, the pulse might appear either in one or both the outputs of the FF. In the case that the SET appears in the positive output of the DUT (Q), it will propagate toward the *Data₁* signal of the first sampling Flip-Flop (*FF₁*). If the duration and amplitude of the pulse are fulfilling the requirements of the technology under the study, it will be sampled by the *FF₁*. Similarly, for the negative output of DUT, the SET pulse which arrives at the negative output of DUT propagates to the *Data₂* signal of the second Flip-Flop (*FF₂*) and it might be sufficient to be sampled by the FF_2. If the inserted SET pulse reaches at least one of the measurements FF and is sampled by them, it is considered as a failure case of the system and the source SET pulse is considered as a critical SET pulse which creates failure. Using this measurement setup, it is possible to classify the SETs which becomes SEU and report the dynamic error rate of the FF under evaluation.

C. The SET mitigation solution

Thanks to the Rad-Ray tool, we can identify the characteristics of the expected SET pulse in terms of duration and amplitude with respect to radiation profile and technology under the study. As a result of the fault injection analysis, the set of transient pulses which can create errors in the output of the FF, known as the critical SET database, have been defined. Based on the features of the critical SETs, a tunable mitigation technique is proposed.

The main idea of the proposed method is to insert a filtering block consisting of a pair of pass transistors connected in series at the output of the FF under evaluation, as represented in Figure 6.

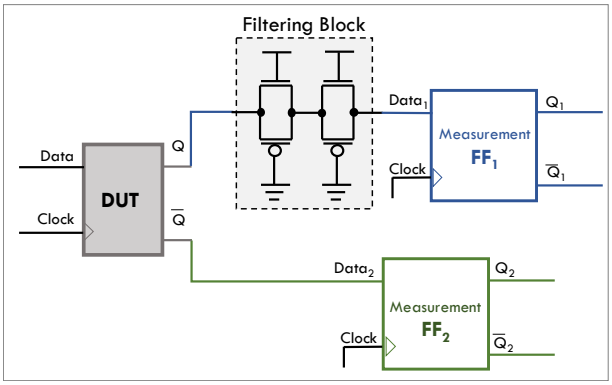

Figure 6. The insertion of the tunable filtering block (at the netlist level) to mitigate SET pulses generated within the DUT Flip-Flop.

The pass transistor reduces the amplitude of the transient pulses while the data signal can pass through the circuit with little change. The pass transistors are always conducting. The gates of the PMOS and NMOS transistors in the pass transistors are permanently connected to ground and VDD, respectively. Setting the size of the former transistor bigger than the latter is more effective to reduce the amplitude of the transient pulse. For example, setting the size of the second transistor 4 times bigger than the first one can reduce the amplitude of the pulse to about 40% [8]. However, it has been mentioned in [11] that increasing the length (L) of the transistor is more effective than increasing the width (W). Therefore, we insert a Filtering Block in which the length of the first pass transistor is greater than the length of the second one.

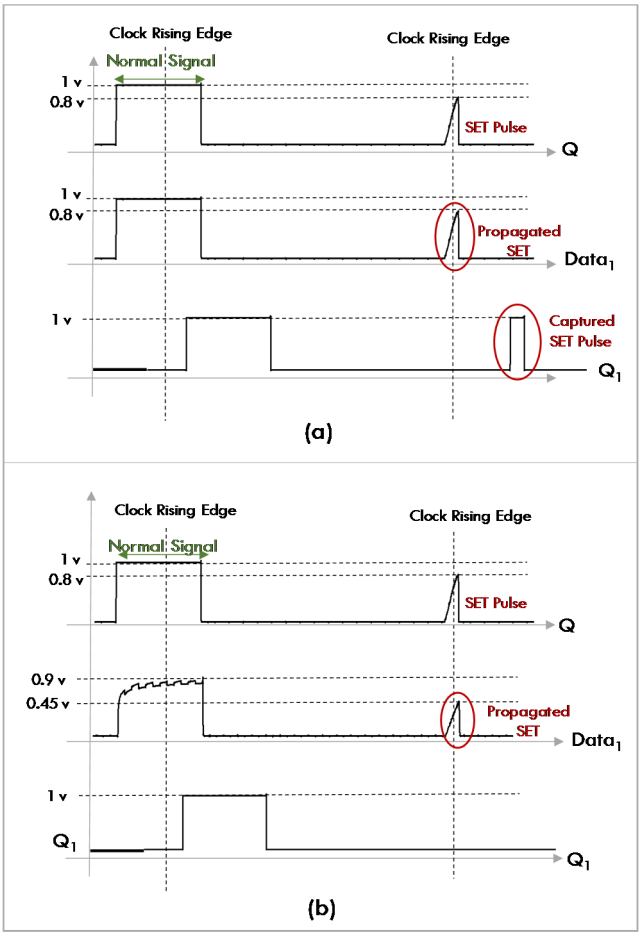

Figure 7. Inserting SET pulse with the duration of 2.1 ns and amplitude of 0.8 V in the DUT internally, propagating toward the input of the measurement FF Data$_1$) (a) the pulse being captured in the output of FF_1 without filtering block (b) the pulse not being captured in the output of the FF_1 with filtering block.

The increase in the length of the back transistor is dependent on the amplitude of the transient pulse to be masked. To elaborate more, as a result of the radiation analysis of a circuit, the sensitivity of the circuit and the features of critical SET pulses that create failure in the system have been defined. To mitigate the SET effect, a filtering block is inserted before the sensitive storage element to mitigate the SET effect. The size of the pass transistor in the filtering block is tuned with respect to the critical SET pulse amplitude, propagated to the storage element. by increasing the size of the transistor, it is possible to increase the filtering capability of the filtering block.

Figure 7 shows the SET pulse with the amplitude of 0.8 V and a duration of 2.1 ns generated in the FF and propagated to the output (Q) of the FF under the test (DUT). Figure 7 (a) represents the SET pulse that arrived at the input of the measurement FF (Data$_1$). The pulse has been captured by FF_1 and it is presented as a normal signal in the output of FF1 (Q_1). On the other side, Figure 7 (b) represents the same SET pulse while the filtering block consisting of two pass transistors is applied to the output of DUT. In this example, the length of the first transistor is four-time bigger than the front one. As can be

observed, the SET pulse is passing through pass transistors and the amplitude of the pule is reducing becoming smaller than the sampling threshold of the technology while the main signal in changing slightly. As a result of the reduction of the amplitude, the measurement FF (FF_1) is not sampling the pulse and just the main signal is appearing in the output of FF_1.

IV. Experimental Results

In order to evaluate the sensitivity of Flip-Flop, the electrical design of the FF has been realized using the FreePDK physical library at 45 nm and adopting the electrical Predictive Technology Model (PTM) of 45 nm for bulk CMOS. Using the commercial K-layout tool, the layout description of the circuit has been extracted in terms of Graphic Data System-II (GDS-II). The netlist and the layout of the circuit have been provided to the Rad-Ray tool together with the radiation mission profile to perform the radiation analysis.

TABLE I. Particles Analyzed by the RadRay Analysis tool

Ion	DUT Energy [MeV]	Range [µm Si]	LET [MeV/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{27}Al^{18+}$	250	131.2	5.7
$^{40}Ar^{12+}$	379	120.5	10.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{124}Xe^{35+}$	995	73	62.5

The radiation analysis has been performed applying the Heavy Ion profile related to the UCL facility [14]. The characteristics of the analyzed particles are reported in Table I where the type of Ions, energy, range, and Linear Energy Transfer (LET) values are reported.

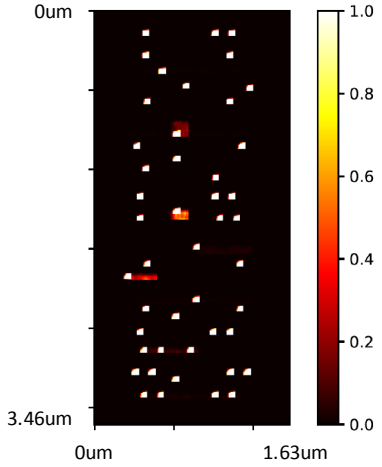

Figure 8. The Single Event Transient (SET) sensitivity heat-map from the top view of the 45nm Flip-Flop.

We performed a simulation of 10,000 particles for each Ion affecting the physical description of the FF under evaluation. The Rad-Ray analysis individuates different volumes distributed among 32 layers. Please consider that we used the material type associated with each layer, as defined in the FreePDK design kit for 45 nm. The Rad-Ray radiation analysis result is reported in Figure 8 and 9. Figure 8 provides an accurate heat-map of the most sensitive volumes of the cell in which the voltage values are normalized between 0 to 1 Volts. Furthermore, Figure 9 represents the cross-section of the FF for different Heavy Ion is shown. As can be seen, the particles with lower energy such as *C* result in lower cross-section, vice versa, by increasing the LET of the particle, the cross-section is increasing such as *Xe* with the highest energy and LET.

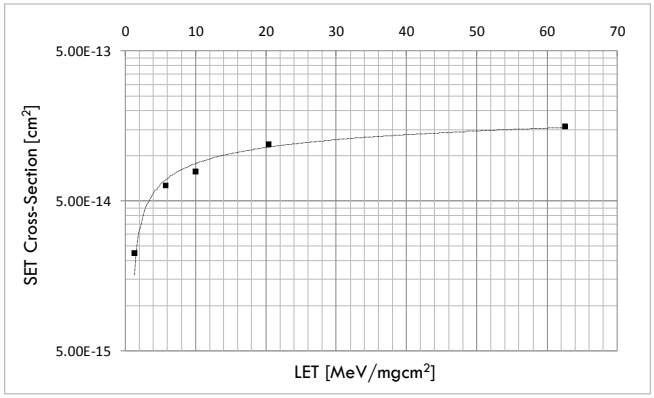

Figure 9. Single Event Transient Cross-Section [cm^2] for static radiation analysis of 45 nm original Flip-Flop.

Figure 10 represents the SET distributions in terms of amplitude of the pulses reported from Rad-Ray analysis. Small Pulse represents the pulses with the amplitude less than 0.45 V while medium pulses having the amplitude between 0.45 V to 0.85 V and large pulse are with the amplitude bigger than 0.85 V. The duration of the pulses is calculated between 100 ps to 520 ps obtained by the Rad-Ray tool for the mentioned radiation profile.

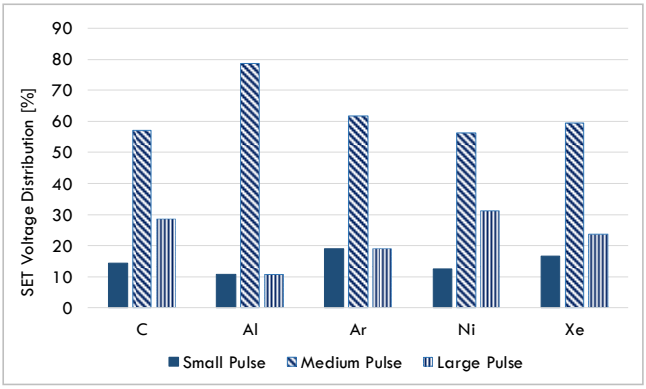

Figure 10. SET distribution generated by 10,000 *Xe* particle injection calculated from Rad-Ray static radiation analysis.

The SET collection is provided to an electrical fault injection environment to evaluate the dynamic failure rate of the 45 nm FF. Please notice that using the Rad-Ray radiation analysis tool, it is possible to calculate both the expected SET pulse characteristic and the sensitive nodes of the transistor that has been affected by the SET pulse are identified too. This information has been provided to the electrical injection environment. The netlist of the circuit has been modified inserting a voltage pulse according to each SET with the duration and amplitude equal to the SET pulse (between 100 ps to 520 ps). For each SET pulse, a random time during the simulation time is chosen to insert the SET pulse and execute the electrical simulation for each single SET pulse. The SET

pulse has been inserted in the sensitive node of the transistor of the DUT, represented in Figure 4. If the pulse propagates to one of the measurement FFs and if it is sufficient in terms of amplitude and duration to be captured by measurement FF, it has been considered that the SET pulse causes a failure in the system.

Figure 11 represents the Dynamic Error Rate *Xe,* the particles with the highest energy. Dynamic Error Rate represents the percentage of the failures with respect to the number of the injected SET pulse. We evaluate the Dynamic Error Rate for different Clock frequency starting with 100 MHz increasing to 1 GHz which is the highest working frequency of the FF in 45 nm technology.

The Dynamic Error Rate is calculated for three different versions of the circuit, represented in Figure 11. As a first version, the original circuit has been evaluated. We increase the clock frequency of the circuit and as it is expected, it is observed that by increasing the frequency, the probability of sampling of SETs is increasing. Therefore, a higher value of Error Rate is observed.

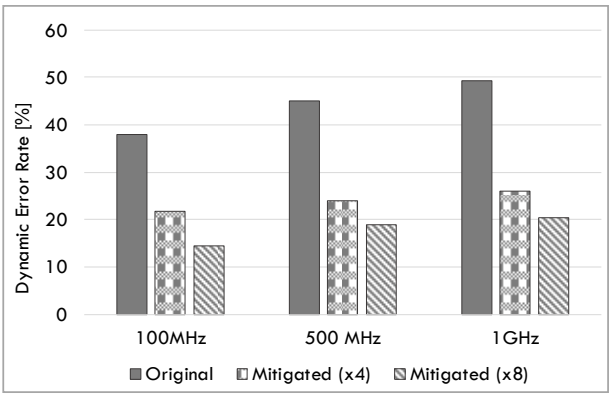

Figure 11. Dynamic Error Rate comparison between original FF 45-nm FF, and mitigated version with the size of the mitigation pass transistor 4 and 8 times larger.

As a next step, we applied a filtering block consisting of two pass transistors in series with the FF under the study. For our analysis, as a first mitigated version, we set the length of the back transistor 4-times bigger than the front one and we report the Dynamic Error Rate. We continue the investigation by increasing the size of the pass transistor 8-times bigger and performing the analysis to report the Dynamic Error Rate. As can be seen in Figure 11, by applying the filtering block with the size of x4, there is a reduction of Dynamic Error Rate of 45%, while the remaining 30% of captured SETs are having lower amplitude. By increasing the size of the pass transistor to x8, the Dynamic Error Rate reduced for 56%, as can be seen in Figure 11. However, inserting and increasing the size of the pass transistors result in area and delay overhead.

Table II reports the area and performance overhead of different versions of the mitigated circuits.

TABLE II. Introduced Area and Performance Overhead by Inserting filtering Block.

Circuit Version	Time overhead [ps]	Area Overhead [%]	Power Consumption Overhead [W]
Mitigated x4	10	1.86	7.843e-06
Mitigated x8	17	3.35	10.59e-06

V. Conclusion and Future Works

The propagation of SET in the circuit has different behavior depending on the generated SET pulse and the propagation path. Therefore, the SET pulses reaching the storage elements have different shapes. In this paper, we proposed a workflow for estimating the shape of the generated SET pulse with respect to the layout of the circuit and the radiation profile, propagating the generated pulse to identify the features of the SET pulses reaching to the storage element by instrumenting the HSPICE circuit electrical stimulation and applying a mitigation solution tuned based on the shape of the pulse reaching to the storage element. The workflow is applied to analyze and mitigate the 45 nm FF. The results show a reduction of Dynamic Error Rate up to 56% with negligible area and performance overhead.

References

[1] D. Tang, C. He, Y. Li, H. Zang, C. Xiong, J. Zhang, “Soft error reliability in advanced CMOS technologies trends and challenges”, Science China Technological Science, vol. 57, n. 9, Sep 2014, pp. 1846-1857.

[2] S. Azimi, B, Du, L. Sterpone, “A new CAD tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs”, Integration, the VLSI journal, ISSN 0167-9260, 2019.

[3] V. F. Cavrois, L. W. Massengil, P. Gouker, “Single Event Transients in digital CMOS- A review”, IEEE Transaction on Nuclear Science, 2013.

[4] Loveless, S. Jagannathan, T. Reece, J. Chetia, B. L. Bhuva, L. W. Massengill, S. J. Wen, R. Wong, D. Rennie, “Neutron and proton induced SET error rates for D and DICE Flip Flop designs at a 40 nm technology node”, IEE Transaction on Nuclear Science, 2011.

[5] N. Seifert, V. Ambrose, B. Gil, Q, Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, A. Balsubramanian, “On the Radiation-induced Soft Error Performance of Hardened Sequential Elements in Advanced bulk CMOS technologies”, IEEE international Reliability Symposium, 2010.

[6] S. Jagannathan, T.D. Loveless, Z. Diggins, B. L. Bhuva, S. J. Wen, R. Wong, L. W. Massengill, “Neutron- and alpha-particle induced soft-error rates for flip flops at a 40 nm technology node”, IEEE International Reliability Physics Symposium, Apr 2011, pp. SE.5.1-SE.5.5.

[7] S. Sayil, “A Survey of Circuit-Level soft error mitigation methodologies”, in Analog Integrated Circuits and Signal Processing, 2019.

[8] Y. Sasaki, K. Namba, H. ITO, “Soft Error Masking Circuit and Latch Using Schmitt Trigger Circuit”, IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2006.

[9] S. Sayil, A. H. Shah, M. A. Zaman, M. A. Islam, “Soft Error Mitigation Using Transmission Gate with Varying Gate and Body Bias”, IEEE Design & Test, 2017.

[10] Kumar, J., & Tahoori, M. B. (2005). Use of pass-transistor logic to minimize the impact of soft errors in combinational circuits. In WKSP on SELSE, pp. 67–74.

[11] L. Sterpone, F. Luoni, S. Azimi, B. Du, “Rad-Ray: A new simulation tool for the analysis of heavy ions-induced SETs on ICs”, IEEE Radiation Effect on Components & Systems Conference, 2019.

[12] Q. Zhou, K. Mohanram, “Gate Sizing to Radiation Harden Combinational Logic”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006.

[13] Q. Zhou, M. R. Choudhury, K. Mohanram, “Tunable Transient Filters for Soft Error Rate reduction in Combinational Circuits”, In IEEE European Test Symposium, 2008.

[14] A. O. Akhmetov et al., "IC SEE Comparative Studies at UCL and JINR Heavy Ion Accelerators," 2016 IEEE Radiation Effects Data Workshop (REDW), Portland, OR, USA, 2016, pp. 1-4.