Test Solution for Heatsinks in Power Electronics Applications

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Test Solution for Heatsinks in Power Electronics Applications

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Abstract: Power electronics technology is widely used in several areas, such as in the railways, automotive, electric vehicles, and renewable energy sectors. Some of these applications are safety critical, e.g., in the automotive domain. The heat produced by power devices must be efficiently dissipated to allow them to work within their operational thermal limits. Moreover, numerous ageing effects are due to thermal stress, which causes mechanical issues. Therefore, the reliability of a circuit depends on its dissipation system, even if it consists of a simple passive heatsink mounted on the power device. During the Printed Circuit Board (PCB) production, an incorrect assembly of the heatsink can cause a worse heat dissipation with a significant increase of the junction temperatures (T_j). In this paper, three possible test strategies are compared for testing the correct assembling of heatsinks. The considered strategies are used at the PCB end-manufacturing. The effectiveness of the different test methods considered is assessed on a case study corresponding to a Power Supply Unit (PSU).

Keywords: power electronics; heatsink test; in-circuit test; functional test

1. Introduction

A relevant issue in power electronics applications is the management of the thermal aspects, i.e., the dissipation of the heat produced by any power device. The high voltages and currents related to these devices may cause an unwanted increase of their junction temperatures (T_j). Many of the electrical features of the power devices depend also on the junction temperature, e.g., the drain-source resistance ($R_{ds,on}$) of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) depends on the T_j [1]. This involves numerous issues in terms of the power efficiency of power applications [2] and in terms of the reliability of power systems.

The increase of the junction temperature in power devices leads to numerous mechanical stresses [3] inside the device itself, which increases the probability of malfunction and breakage of the power device. The materials used in the power devices (e.g., silicon, copper, iron, oxides, plastic) have different thermal expansion coefficients. When the temperature increases, these materials have different thermal dilatation causing considerable physical stress inside the device [3]. In addition to mechanical stress, there are also numerous device ageing phenomena associated with the temperature increase [4]. Due to ageing, the electrical parameters of the devices may change, reducing their average life [5,6]. The mechanical stress and the ageing phenomena of the device are the main cause of the breakdown of power devices [7].

Several cooling strategies [8] have been introduced to dissipate the excess of heat produced by the electronic devices and to avoid an undesired temperature increase. Passive heatsinks are the most commonly adopted approach. These heatsinks are implemented with different copper or aluminum cooling fins arranged to ease the dispersion of heat by convection. Typically, a passive heatsink is considered as efficient, reliable, and inexpensive. However, it normally has a significant physical volume and a considerable weight.

As an alternative to passive heatsinks, active heatsinks can be used. By means of a fan, it is possible to force a constant airflow between the fins of the heatsink to facilitate the heat dispersion. In more complex systems, it is possible to use the same principle for forcing a constant liquid flow within the heatsink. The active heatsinks have a smaller physical volume and allow a greater dispersion of the heat produced by the power devices. However, they are ineffective if the cooling fan or of the circulation pump do not work correctly. However, the cooling systems used in power systems require adequate levels of reliability; their malfunction can cause temperature increases in power devices causing malfunction or breakage.

The main contribution of this paper is to propose a methodology for assessing the effectiveness of different test strategies used to verify the correct operation of the cooling systems. The test procedures considered have the target of checking the correct assembly of the heatsinks on the power devices, as discussed in [9,10]. A bad assembly of the heatsink propagates the heat to the surrounding environment to a lesser degree, resulting in a junction temperature rise. The test strategies considered are applied as an end-of-line stage during the production on the final Printed Circuit Board (PCB). In the final PCB, all electrical components are assembled, including the heatsinks.

The tests strategies considered are based on the *in-circuit test* approach and *functional test* approach. Moreover, a further hybrid approach realized combining the previous two strategies was considered. The hybrid approach (called *observability enhanced functional test*) represents an improvement of the *functional test* approach. The strategies were evaluated on different devices assembled on a private heatsink or sharing the same heatsink, i.e., the heatsink was assembled on the same power devices. The evaluation of the test procedures was performed using a thermal model of the dissipation system. The thermal model was used to perform a thermal simulation together with the electrical one; in other words, an electrothermal simulation of the system was performed using a circuit simulator. Some thermal faults were considered in the thermal model of the system. This paper uses the concept of thermal fault associated with an incorrect heatsink assembly [9]. In this work, some typical power devices were considered, such as Insulated Gate Bipolar Transistors (IGBTs) and power diodes.

This work shows that the effectiveness of the considered test strategies strongly depends on the circuit on which they are used; in other words, some electrical components can hide the effects of the faults during the tests. Therefore, the effectiveness of the test is inhibited. In general, the *observability enhanced functional test* approach is particularly effective for testing the heatsink's assembly, as discussed in this paper. The three test strategies considered in this paper were evaluated on a real case study corresponding to a Power Supply Unit (PSU) for industrial applications.

This work extends two previous works [9,10]. In Reference [9], a test procedure applicable to MOSFET devices was discussed. In that work, the MOSFETs were mounted on a passive heatsink. In Reference [9], the effects of different thermal faults on power devices are considered and analyzed. Furthermore, in Reference [9], some possible thermal faults are experimentally reproduced in the laboratory in order to understand the real impact of the incorrect heatsink assembly on power devices. The second work [10] developed a thermal model of the heat dissipation system. The model discussed in [10] considers a single power device assembled on the heatsink. This model is useful for identifying the maximum mechanical tolerances associated with the heatsink assembly, e.g., the maximum possible distance between the device and the heatsink or the minimum contact surfaces between the device and the heatsink. For the purpose of the work reported in [10], the power device was not yet assembled on the PCB.

In the current work, the heatsink was assembled on the PCB and the effectiveness of the test procedures considered can be influenced or inhibited by the PCB circuit, as discussed in this paper.

The paper is organized in different sections; Section 2 provides the reader with some useful information on the end-of-manufacturing test and about the thermal models. Section 3 introduces the concept of thermal faults and illustrates the three test strategies considered in this paper. Section 4 presents the selected case study and the thermal model of the dissipation system used. Section 5 presents and elaborates on the experimental results obtained. Finally, Section 6 draws some conclusions.

2. Background

In this section, different concepts related to the typical end-of-manufacturing tests performed on PCBs in an industrial environment are shown. Furthermore, some aspects of the thermal models are discussed. Finally, the Temperature-Sensitive Electrical Parameters (TSEP) of the IGBT and the diode devices are discussed.

2.1. End-of-Manufacturing Tests

The purpose of this section is to provide the reader with some basic information about the main test strategies implemented at the end-of-manufacturing in an industrial environment. The purpose of these tests is to verify the correct assembly of the final PCB. As indicated in [11], 75% of manufacturing defects occur during the assembly of the PCBs, while the remaining 25% depend on electronic devices already defective before the assembly phase. The main test strategies used at the end-of-line phase are the *in-circuit test* and the *functional test* [11,12].

The *in-circuit test* is performed through Automatic Test Equipment (ATE); the ATE is able to directly contact some pins of any electronic devices soldered on the PCB. Different thin and precise probes of the ATE are used to contact the interest points of the circuit. The electrical contact operation can be performed in two ways, with the *bed of nails* [11] approach or with the *flying probes* [11] approach. In the first one, different needles exist in the ATE test compartment, and the board is placed over the needles to implement the electrical contacts. In the second one, a robotic arm with some needles performs the electrical contacts moving around over the PCB. In this paper, the *flying probes* approach was considered. The electrical contact can be performed on the welding of the component to be tested, or by a *test point*. As discussed in [11], a *test point* is a location on a PCB used to measure an electrical value or to apply a test signal. The *test points* are placed during the PCB design phase for facilitating the test procedures. Through the different probes positioned on the PCB, the ATE imposes some voltages or currents in the circuit and simultaneously measures different voltages or currents. In this way, some electrical stimuli are applied to the device under test to verify its correct operation after the PCB assembly phase. For example, consider a resistor; it is possible to test it by imposing a voltage (V_{test}) at its pins and measuring the current (I_M) that passes through the device, as shown in Figure 1. The probes are automatically moved on the component to be tested; the ATE forces the test stimuli and performs the necessary electrical measurements. Electrical measurements are processed by the ATE and the results compared to the expected ones.

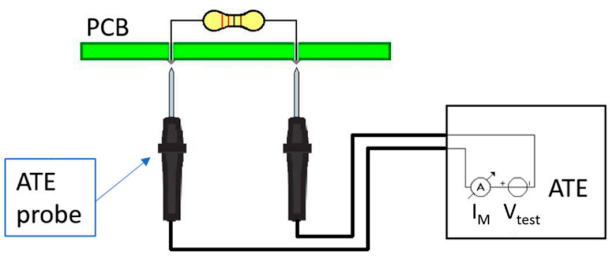

Figure 1. In-circuit test approach.

The stimuli applied to the circuit can propagate in an undesired way; this phenomenon can inhibit the test or damage other devices present in the PCB. Therefore, it is often necessary to place additional *guard probes* [12–14] on the PCB. These *guard probes* are ground connections used for isolating the device under test; the usage of these probes is well known in the industrial field, as it is widely discussed in [13]. The guard probes can also be used for the power circuits [14].

The *functional test* is performed by applying some electrical stimuli to the PCB input ports and observing the PCB behavior on the PCB output ports. A *functional test* is performed considering only the design specifications of the PCB. The stimuli applied to the PCB are compliant with the technical specifications of the PCB defined during the design phase of the circuit. The values observed on the PCB output signals must be compliant with the PCB design specifications. If there is a fault, the measurement performed is different from the expected one. This first functional approach based only on the observation of the PCB output ports is called the *base functional test*. Moreover, it is possible to increase the observability of the *base functional test* by using the *observability enhanced functional test* approach [15], where ATE is used. During this test, some electrical measurements are performed in different points of the PCB resorting to some ATE probes; the measurements are performed while the PCB is functionally stimulated. The signals measured by the test equipment during the *observability enhanced functional test* must be compliant with the PCB design specifications.

2.2. Thermal Model Concept

As discussed in [10,16–18], it is possible to develop *thermal* models by exploiting the analogies between thermal and electrical models. In such models, the electrical quantities of voltages and currents assume different physical meanings. In particular, in thermal networks, the voltage represents the temperature, while the current has the meaning of heat flow. A thermal resistance identifies an obstacle to the propagation of heat in a material, while a thermal capacitance identifies the amount of heat stored by a physical object. Therefore, it is possible to develop thermal circuit models using the *Cauer* or *Foster* networks, as discussed in [4,10,19]. Figure 2 shows the two possible network topologies. *Cauer's* network is usually derived from the physical analysis of the system, while the *Foster* network is obtained experimentally. With both approaches, some R-C cells are used to model the thermal behavior of the different materials that constitute the physical system modelled.

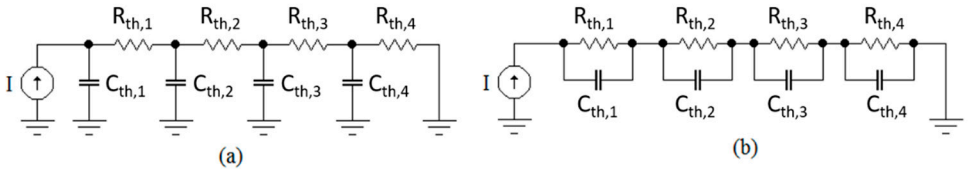

Figure 2. (**a**) Cauer thermal network; (**b**) Foster thermal network.

2.3. Temperature-Sensitive Electrical Parameters (TSEPs)

The measurement of the junction temperature in a semiconductor device is possible resorting to the device electrical parameters sensitive of the junction temperature. These parameters are called *Temperature-Sensitive Electrical Parameters* (TSEPs) [20]. In Reference [8,9], the most frequently used TSEP for measuring the T_j in the MOSFET device is considered, i.e., the relationship between the R_{on} of the IGBT and the T_j is discussed. In this paper, a diode and an IGBT device are considered. Among the possible TSEPs for these devices, the forward voltage (V_F) of the diode and the dependence on the V_{ce} and I_c of the IGBT are considered.

For the diode device, the relationship between V_F and T_j is typically used, as discussed in [19]. In particular, there is a threshold voltage decrease as a consequence of the junction temperature increases in the diode device. Typically, the relationship V_F (T_j) is provided by the diode manufacturer, or it can be obtained experimentally, as discussed in [21].

On the other side, for the IGBT device, there is a relationship that involves multiple TSEPs, as discussed in [20,22]. In particular, it is possible to estimate T_j by resorting to a relationship involving the collector–emitter voltage drop (V_{ce}) and the I_c current that flows in the IGBT device. The relationship V_{ce} (I_c, T_j) can be estimated with the procedure described in [22] by means of numerous electrical measurements at different I_c and V_{ce}.

3. Proposed Approach

This section defines first the concept of *thermal faults* proposed by us and discusses the *in-circuit test* and *functional test* strategies considered. It then outlines the proposed approach to assess the quality of a test solution for the heatsink assembly test.

3.1. Thermal Faults

In accordance with the definition of thermal resistance provided in Section 2.2, we define the concept of *thermal fault* as an increase in the thermal resistance value in the thermal model of the cooling system. In the thermal model of the dissipation system, some additional thermal resistances are added in series with the thermal resistance of the model.

In this paper, we consider the thermal faults associated with the heatsink assembling; in other words, further thermal fault resistances are added in the thermal model between the portion of the model which describes the internal physical structure of the power device and the portion of the model that identifies the heatsink. Usually, as described in [23], there is a *thermal contact resistance* that models the difficulty that the heat encounters for propagating from the power device to the heatsink. The thermal fault resistance considered is added in series with this *thermal contact resistance*. From a physical perspective, the added thermal fault resistance represents a further obstacle to the propagation of the heat generated by the power device.

3.2. Thermal Faults Simulation

The effectiveness of the considered test procedures can now be assessed by means of electro-thermal simulations using a thermal model of the cooling system. The thermal model of the devices and the thermal model of the overall dissipation system can be obtained as described in [18,24,25]. The considered test methods perform voltage or current measurements on power devices; these measurements can be performed by ATE. Different thermal faults simulations are performed in a fault-free scenario and with a single thermal fault injected in the cooling system thermal model. The value of the thermal fault resistances injected is calculated as discussed in [10], i.e., the value of the thermal resistance of the fault is chosen in order to maximize the junction temperature of the power device to bring it to the maximum junction temperature supported ($T_j = T_{j,MAX}$). The value of the maximum junction temperature supported is usually provided by the power device manufacturer. As discussed in [10], a thermal resistance value equal to or greater than the thermal fault resistance brings the junction temperature of the device out of the device operating parameters defined by the device manufacturer. Values of thermal resistance lower than the thermal fault resistance cause an increase in T_j; however, the T_j remains within the thermal limits defined by the manufacturer.

3.3. TSEP Test Characterization

The evaluation of the junction temperature in the diode and IGBT devices requires an initial characterization procedure. The aim of the characterization procedure is to obtain the relationship between T_j and the electrical parameters sensitive to the T_j for the diode and the IGBT devices, as discussed in Section 2.3. Figure 3 shows the calibration circuits used for the diode and the IGBT. For the diode device, the characterization procedure was performed in two phases, a heating phase and a cooling one. In the heating phase, the switch (SW) was configured in position A.

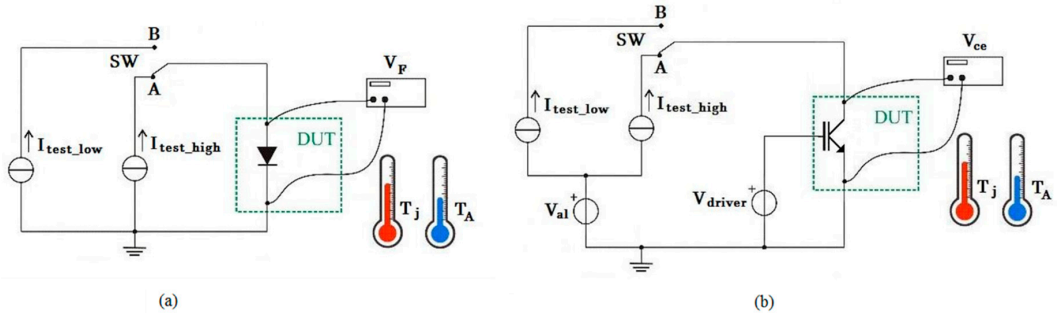

Figure 3. Diode (**a**) and Insulated Gate Bipolar Transistor (IGBT) (**b**) characterization circuits.

A high current flowed through the diode in order to dissipate a high power and increase the T_j. The junction temperature reached was about the maximum junction temperature supported by the device. However, in the cooling phase, the switch was commutated in position B; a low test current was forced in the diode. During the cooling phase, the V_F and T_j were continuously measured; T_j was measured on the cathode of the device, e.g., by means of a thermocouple as discussed in [26]. The power dissipated by the diode during the cooling phase was negligible; therefore, the temperature measured on the cathode was about T_j, as discussed in [26]. Figure 4a shows the trend of V_F as a function of T_j for different test currents. These curves are useful for estimating the T_j during the test of the device assembled on the PCB.

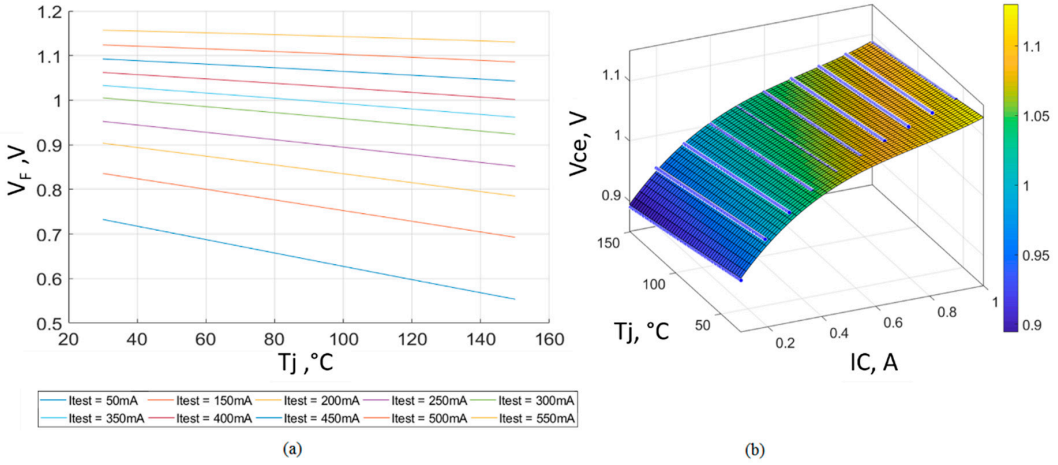

Figure 4. (**a**) Diode Temperature-Sensitive Electrical Parameters (TSEP), (**b**) IGBT TSEP.

Moreover, the characterization procedure for the IGBT device was performed with the circuit shown in Figure 3. The characterization procedure was similar to the diode one. However, a drive voltage higher than V_{th} and a voltage V_{al} able to maintain the IGBT in conduction were imposed. In the heating phase, a high current flowed in the IGBT, while in the cooling phase, a low current was forced. Moreover, the V_{ce} and T_j were continuously monitored in the IGBT cooling phase. The T_j was measured on the IGBT collector pin as previously discussed for the diode. Figure 4b shows the different measurements performed at different test currents during the cooling phase. The TSEP characteristic of the IGBT can be obtained by interpolating the different curves measured.

3.4. In-Circuit Thermal Test

Two different in-circuit tests procedures were considered. In this paper, we extended the methodology discussed in [9,10] to the IGBT device, while in [27], a test strategy for the diodes is shown. Both strategies consist of contacting the pins of a single power device to perform the test. Figure 5 shows the considered test procedure for a power IGBT and a diode. The circuit implemented by the ATE is indicated in green. During the *in-circuit test*, the PCB was not powered, and there were

no further electrical stimuli applied to the PCB except those forced by the ATE. Moreover, the input and output ports of the PCB were disconnected.

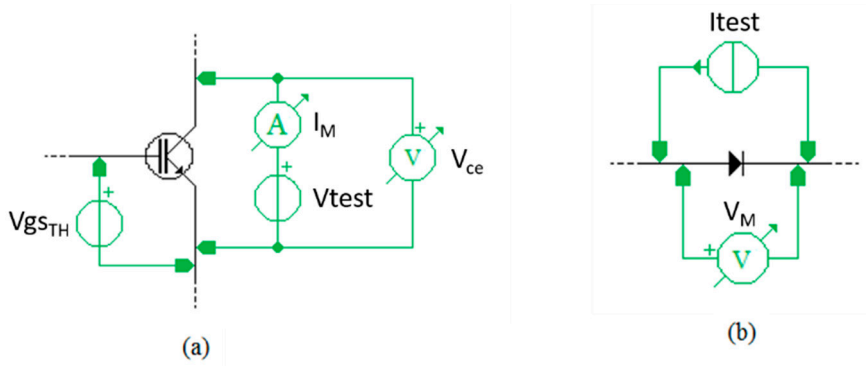

Figure 5. (**a**) In-circuit thermal test for IGBT device; (**b**) in-circuit thermal test for diode device.

For the IGBT device, two voltages were applied to turn on the device. At the same time, the ATE measured the current (I_M) that flowed through the device and the voltage (V_{ce}) between the collector and the emitter terminals. The test voltage imposed on the device was chosen considering the device specifications using Equation (1). The test voltage (V_{test}) was chosen in a conservative manner in order not to damage the power device, i.e., considering 50% of the maximum power (Pmax) managed by the device. The I_{test} current was chosen considering the maximum current that can be delivered by the ATE during the test.

$$\text{Vtest} = \frac{\text{Pmax}}{2} \cdot \frac{1}{\text{Itest}}; \text{ with Itest} \leq \frac{\text{Imax}_{\text{ATE}}}{2} \quad (1)$$

With the I_M and V_{ce} values measured by the ATE, it is possible to estimate the T_j using the TSEP characterization test discussed in Section 3.3. In the presence of a thermal fault on the heatsink assembly, the T_j of the device was higher than expected; therefore, the measured I_M was different from the expected one, as discussed in Section 2.3.

On the other side, for the power diode, a test current (I_{test}) was forced in the diode by the ATE. At the same time, the voltage drop across the diode was measured (V_M). The I_{test} current imposed by the ATE was chosen in a conservative manner considering the device specifications. The I_{test} current value was chosen with Equation (2).

$$\text{Itest} = \frac{\text{Pmax}}{2} \cdot \frac{1}{\text{V}_{\text{F}_{nominal}}} \quad (2)$$

With the V_M value measured by the ATE, it is possible to estimate the T_j by means of the TSEP characterization test of the diode performed in Section 3.3. As discussed in Section 2.3 and in [27], the increase of the junction temperature in the diode device caused a decrease in the forward voltage (V_F). Therefore, in the presence of a thermal fault, the voltage drop measured on the diode was lower than the expected one.

3.5. Functional Thermal Test

The functional test was performed by applying different electrical stimuli on the input ports of the power converter and observing the trend of the voltages or currents at the output ports. The proposed approach is based on the *observability enhanced functional test* in which the voltage drop on the power device is also measured. All measured electrical quantities must comply with the PCB specifications and must be equal (except for a defined tolerance) to the expected ones. The voltage drop on the power device is measured because it depends on the junction temperature (T_j) of the device, as discussed in Section 2.3. An excessive variation of the electrical quantities measured during the functional test indicates the presence of a thermal fault in the heatsink.

4. Case Study

In this section, the case study and the thermal model of the cooling system used are presented. In particular, a Power Supply Unit (PSU) for industrial applications was considered. The heat produced by the PSU power devices is dissipated resorting to a passive heatsink assembled on the power devices. The PCB considered was developed by the Politecnico di Torino as part of an industrial project performed by the Power Electronic Innovation Center (PEIC). The PSU considered is used to power household appliances or industrial compressors.

4.1. The Power Supply Unit

The PSU we considered consists of three boost cells; each cell is composed of an inductor, a diode (STTH12S06), and an IGBT (STGF19NC60), as shown in Figure 6. Figure 6 also shows the FAN9673 analog controller [28], which drives the three IGBTs of the PSU. The FAN9673 measures the currents in the three boost cells, the PSU output voltage, and the PSU input voltage in order to supply a continuous stabilized voltage in output. The currents are measured by means of appropriate sense resistances (Rs1, Rs2, Rs3). The PSU provides a DC output voltage of 400 V with a 12 A of maximum current delivered to the electrical load. The PSU works with AC sinusoidal input voltages between 110 V RMS and 220 V RMS at 50 Hz or 60 Hz. The PSU is used to power a three-phase inverter for electric motors.

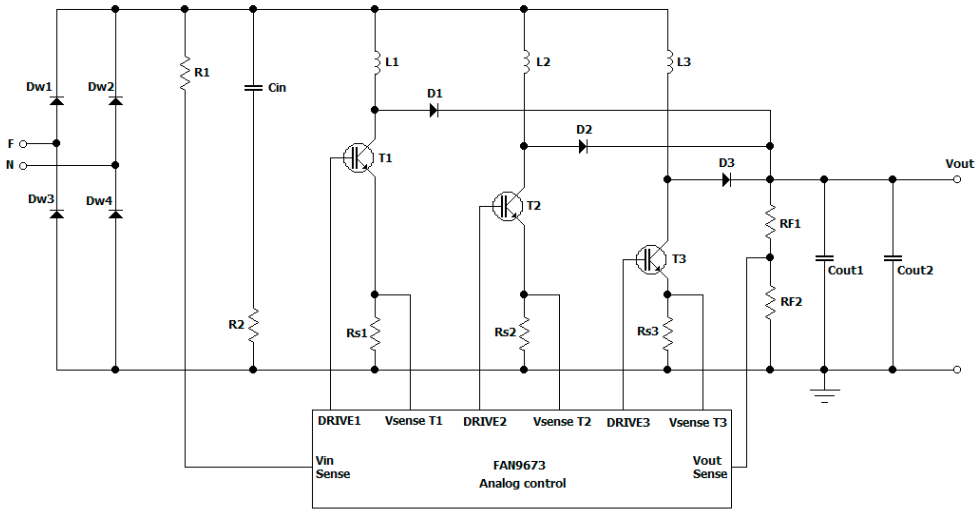

Figure 6. The Power Supply Unit (PSU).

The STTH12S06 diode [29] is a power device assembled in a TO-220FPAC package. It has a forward voltage (V_F) of 1.5 V, and it can manage a current up to 12 A. The maximum junction temperature (T_{jMAX}) supported is 175 °C, and it has a case junction thermal resistance ($R_{th,JC}$) of 4.6 °C/W. The IGBT STGF19NC60 [30] is a power device assembled in a TO-220FP package. The device manages voltages up to 600 V and currents up to 19 A. The maximum managed junction temperature is 150 °C with a junction-case thermal resistance ($R_{th,JC}$) of 3.9 °C/W. The STTH12S06 diode and the STGF19NC60 IGBT are produced by STMicroelectronics, while the FAN9673 analog controller is produced by ON Semiconductor.

The PSU cooling system is built using the passive SK56 heatsink produced by Fischer Elektronik [31]. The heatsink is composed of aluminum, it is equipped with numerous cooling fins able to disperse the heat. The thermal resistance of the heatsink (R_{th,H_A}) is 0.35 K/W. From Figure 7, it is possible to see that the heatsink completely covers the PCB of the PSU (L × W × H: 150 mm × 300 mm × 40 mm). The heatsink is connected to the three power diodes (D1, D2, D3) and to the three IGBTs (T1, T2, T3) by means of through screws. As shown in Figure 7, the PSU power diodes and IGBTs are assembled on the back side of the PCB. This configuration allows a better physical contact between the power devices and the heatsink.

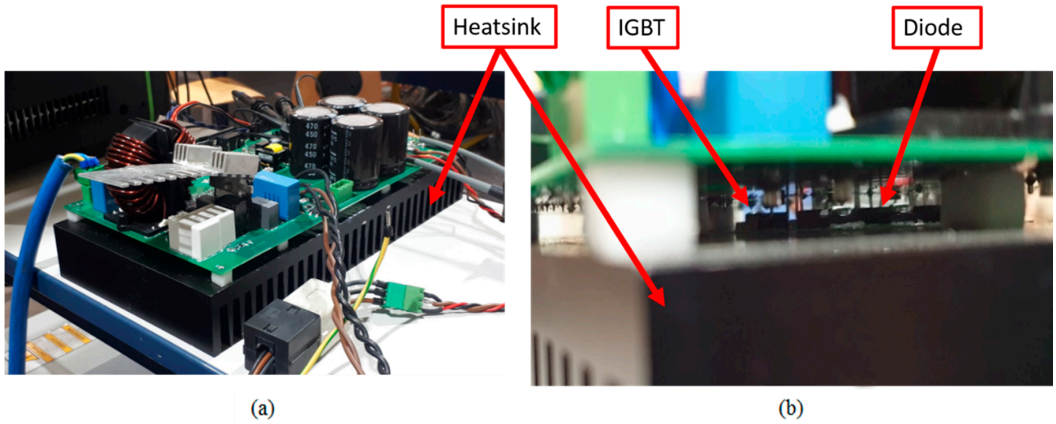

Figure 7. (**a**) Printed Circuit Board (PCB) overview; (**b**) power devices assembled between the PCB and the heatsink.

4.2. Thermal Model of the PSU Cooling System

In this sub-section, the electro-thermal models of the power devices and the cooling system of the PSU are discussed. The whole thermal model is shown in Figure 8 [18,24,25]; the three diodes and the three IGBTs that constitute the three boost cells of the PSU that share the same passive heatsink are considered, as shown in Figures 6 and 7. As discussed in Reference [25], the thermal model of each device can be combined with the thermal model of the heatsink. In Figure 8, the thermal models of the power devices are shown in blue, while the thermal model of the heatsink is shown in green. Moreover, the thermal resistances ($R_{th,D1\_H}$; $R_{th,T1\_H}$; $R_{th,D2\_H}$; $R_{th,T2\_H}$; $R_{th,D3\_H}$; $R_{th,T3\_H}$) model the assembly of the power devices on the heatsink.

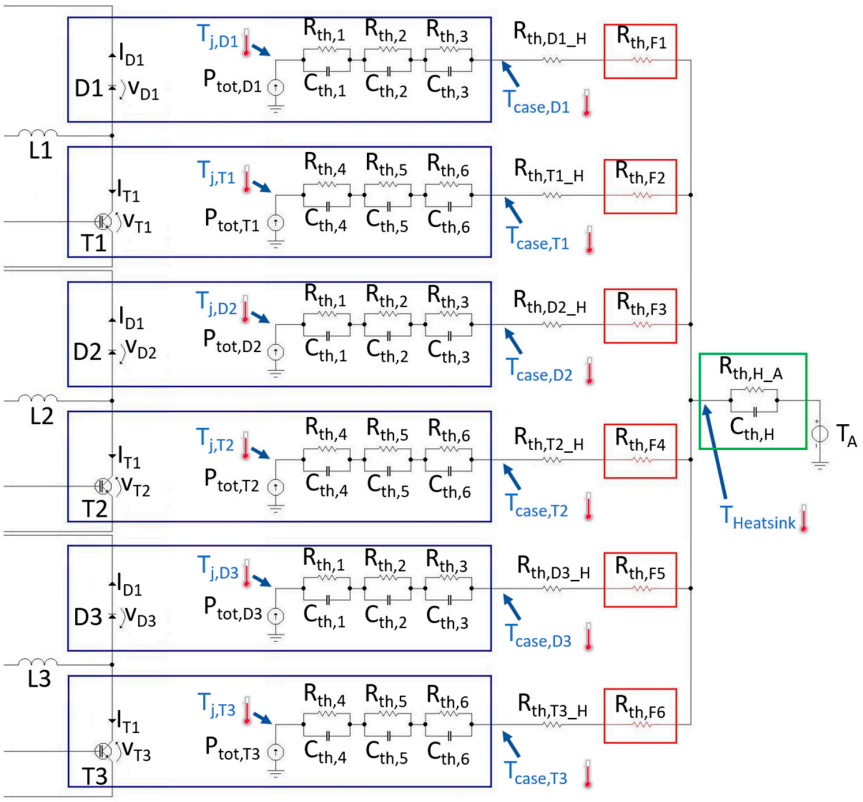

Figure 8. Thermal model of the cooling system.

For each power device, there is a current source, called P_{tot}, that models the total power dissipated by the device. The power dissipated by each device is given by Equation (3) for the diode device and Equation (4) for the IGBT device, as discussed in [18]. The P_{tot} current generator models the heat flow produced by the power device. The thermal models of the IGBT and the diode are completed by three R-C *Foster* cells that model the different layers of silicon, metal, and plastic of which each device is composed. The thermal model of the single power device can be provided by the device manufacturer (an example in [17]) or obtained as proposed in [32]. An additional *thermal contact resistance* ($R_{th,D1\_H}$; $R_{th,T1\_H}$; $R_{th,D2\_H}$; $R_{th,T2\_H}$; $R_{th,D3\_H}$; $R_{th,T3\_H}$) was added between the heatsink and the case of each power device, as discussed in Section 3.1. The heatsink was modelled by an additional R-C cell (R_{th,H_A}; $C_{th,H,}$). Figure 8 also shows the points where the different temperatures were observed during thermal simulations; for example, the junction temperature was measured on the P_{tot} generator in each device. The T_A voltage source was used for modelling the ambient temperature, as discussed in [17]. The six thermal fault resistances discussed in Section 3.1 are indicated in red in the thermal model ($R_{th,F1}$; $R_{th,F2}$; $R_{th,F3}$; $R_{th,F4}$; $R_{th,F5}$; $R_{th,F6}$). Each thermal fault resistance is associated with the heatsink assembled on each power device concerned. The value of the thermal fault resistances is calculated as discussed in Section 3.2.

$$P_{tot} = V_D \cdot I_D \quad (3)$$

$$P_{tot} = V_T \cdot I_T \quad (4)$$

5. Results Analysis

This section shows the results obtained by means of simulations. The effectiveness of the *in-circuit thermal test* and *functional thermal test* strategies outlined in Section 3 were assessed. The test strategies were evaluated on the case study discussed in Section 4, focusing on their ability to detect possible defects affecting the heatsink assembly. In particular, the diodes and IGBTs that share the same heatsink of the PSU were considered. The last section draws some conclusions about the obtained results.

5.1. In-Circuit Thermal Test

The *in-circuit thermal test* was applied to the IGBTs (T1, T2, T3) and to the diodes (D1, D2, D3) of the PSU, with reference to Figure 6. The *in-circuit thermal test* was performed with the converter off and with the load disconnected. For the IGBT devices, the test was performed by imposing a Vtest = 1.5 V and a Vgs = 4 V on the IGBT; at the same time, the current I_M that flows through the device was measured, as discussed in Section 3.3. During the test, the thermal faults ($R_{th,F2}$; $R_{th,F4}$; $R_{th,F6}$) relating to the assembling of the heatsink on the IGBTs were injected; a single fault was considered in each simulation. Table 1 shows the results obtained for the IGBT T1. Similar results were obtained on the other two IGBTs. The measurements were performed with the circuit in the steady state, i.e., when the I_M current reached a stable steady-state value. An ambient temperature of 25 °C was considered during the simulation (T_A = 25 V).

Table 1. In-circuit IGBT results.

	$R_{th,F2}$ (°C/W)	I_M (A)	$Vce_{,T1}$ (V)	$T_{j,T1}$ (°C)	$T_{CASE,T1}$ (°C)	$T_{HEATSINK}$ (°C)
Fault-free	0	1.04	1.41	72	42	26
With fault	10.3	1.27	1.43	148	117	25

The considered *in-circuit thermal test* was able to detect the thermal fault of the heatsink assembled on the IGBT observing the I_M current; in the presence of the thermal fault, the I_M was larger by about 0.23 A with respect to the I_M in the fault-free scenario. The value of the thermal fault resistance was chosen as discussed in Section 3.1; the value that brings the $T_{j,T1}$ of the IGBT device to the maximum junction temperature supported by the device was chosen. In this case, a thermal resistance of 10.3 °C/W was enough to bring the $T_{j,T1}$ to 150 °C.

Table 1 shows also the temperature present on the TAB transistor package ($T_{CASE,T1}$) and the heatsink temperature ($T_{HEATSINK}$). Note that the thermal fault can also be observed resorting to the $T_{CASE,T1}$ temperature of the IGBT; the $T_{CASE,T1}$ temperature cannot be directly measured due to the presence of the heatsink above the power device. There is no particular variation of the heatsink temperature in presence of a fault.

Figure 9 shows the *in-circuit thermal test* related to the power diode D1. Similar results were obtained for the other diodes. In Figure 9, the circuit created by the ATE is shown in green. In this case, a test current of I_{test} = 0.5 A was forced. Table 2 shows the results obtained with the *in-circuit thermal test* on the diode. In presence of the fault, there was no significant V_M variation from the fault-free scenario. In the case study, the *in-circuit thermal test* on the diodes was ineffective. It was impossible to test each diode separately due to the connection of the diodes in this circuit. The test current forced on one of the diodes by the ATE flowed on the other diodes as well. A portion of the test current forced flows through the inductances (L1, L2, L3); then the voltage drop across the three inductors was zero. Therefore, the three diodes (D1, D2, D3) were parallel; hence, they have the same voltage drop. In the presence of a thermal fault on a diode, the diode voltage drop is similar to the diode voltage drop in the fault-free scenario. The effect of the thermal fault on a diode is masked by the other diodes placed in parallel. The *in-circuit thermal test* is ineffective in this specific circuit due to the D1, D2, and D3 diodes placed in parallel.

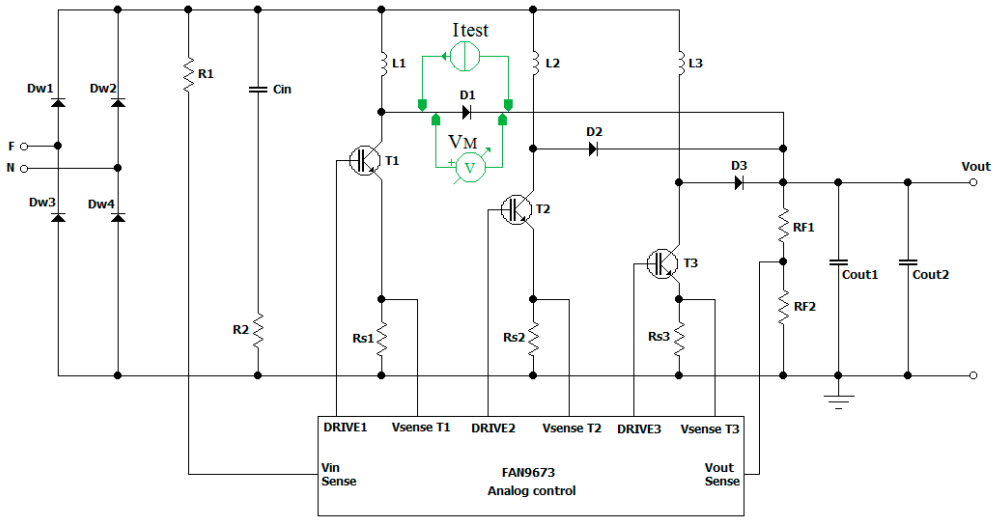

Figure 9. In-circuit thermal test for diode device.

Table 2. In-circuit diode results.

	$R_{th,F1}$ (°C/W)	V_M (V)	$T_{j,D}$ (°C)	$T_{CASE,D1}$ (°C)	$T_{HEATSINK}$ (°C)
Fault-free	0	1.46	31.2	27.2	25.4
With fault	16.7	1.45	176.3	51.7	25.5

5.2. Functional Thermal Test

The *functional thermal test* was performed by applying an AC sinusoidal voltage of 220 V RMS at 50 Hz to the input port of the power converter. A resistor was connected to the output port as an electrical load. The test was performed using the *observability enhanced functional test* strategy discussed in Section 3.4; therefore, during the test, it was possible to measure other electrical quantities by placing additional probes on the PCB. Typically, voltage measurements are performed on the PCB. During the test, different electrical quantities were measured, such as the I_L current that flows through the RL load, the current I_A absorbed by the PSU, the output voltage V_{out} of the PSU, the IGBT voltage V_{ce} when the IGBT was saturated, and V_F on the diode when the diode was directly polarized. Table 3 shows

the measured values in the fault-free scenario and in presence of the heatsink thermal fault for the IGBT device, while Table 4 shows the measured values for the diode device. The electrical quantities I_L, I_A, V_{out}, V_{ce}, and V_{ak} were measurable by ATE during the test, while the other measurements were obtained only in simulation. Furthermore, Tables 3 and 4 show the junction temperature reached in the power device, the device case temperature, and the heatsink temperature. The values shown in Tables 3 and 4 refer to the IGBT T1 and the diode D1, while similar values were also measured for the other devices.

Table 3. Results for the functional test of the IGBT.

	$R_{th,F2}$ (°C/W)	I_L (A)	I_A (A)	V_{out} (V)	$V_{ce,T1}$ (V)	$T_{j,T1}$ (°C)	$T_{CASE,T1}$ (°C)	$T_{HEATSINK}$ (°C)
Fault-free	0	8.5	16.1	400	0.75	71.1	33.7	28.3
With fault	10.3	8.5	16.1	400	1.21	151.2	86.3	28.5

Table 4. Results for the functional test of the diode.

	$R_{th,F1}$ (°C/W)	I_L (A)	I_A (A)	V_{out} (V)	$V_{F,D1}$ (V)	$T_{j,D1}$ (°C)	$T_{CASE,D1}$ (°C)	$T_{HEATSINK}$ (°C)
Fault-free	0	8.5	16.1	400	1.3	82.9	38.4	28.2
With fault	16.7	8.5	16.1	400	1.1	181.1	95.6	28.4

The *base functional test* approach was performed observing only the signals at the PCB input/output ports; in the case study, the I_L current on the electrical load, the I_A current absorbed by the PSU from the electrical grid, and the V_{out} voltage provided by the PSU were considered. With the *base functional test* approach, no thermal faults were detected, as shown in Tables 3 and 4. With the *observability enhanced functional test* approach, it was possible to observe the effect of the thermal fault on the heatsink assembly, as shown in Tables 3 and 4. In particular, it was possible to detect the faults by measuring the voltage drop ($Vce_{,T1}$; $V_{F,D1}$) present on the power devices.

5.3. Tests Results

This last section summarizes the main results obtained with the *in-circuit thermal test* and with the *functional thermal test*. Table 5 shows, for each test strategy, which thermal faults were detected (DT) or not detected (NDT).

Table 5. Test approach comparisons.

Thermal Fault	Power Device	In-Circuit	Base Functional Test	Observability Enhanced Functional Test
$R_{th,F1}$; $R_{th,F3}$; $R_{th,F5}$	Diodes D1, D2, D3	NDT	NDT	DT
$R_{th,F2}$; $R_{th,F4}$; $R_{th,F6}$	IGBTs T1, T2, T3	DT	NDT	DT

The *in-circuit thermal test* is potentially able to detect the thermal faults associated with the heatsink assembly on the power devices, provided that the PCB circuit allows the test, in other words, if the stimuli applied by the ATE on the power device are not influenced by other devices present in the circuit, e.g., the D1, D2, and D3 diodes in the case study. In addition, to perform the *in-circuit thermal test*, the ATE probes must be able to physically reach each device. The physical access to the power device can be inhibited by the power heatsink itself that covers the power device. During the development of the PCB, it was possible to introduce some *test points* that were used by ATE to contact the power devices of interest, as discussed in Section 2.1. This location is specifically designed to be accessible by ATE also in the presence of a heatsink.

The *base functional test* was not sufficient to observe the thermal faults considered. The electrical quantities observed during the *base functional test* were controlled by the FAN9673 controller. The analog controller of the PSU aims to stabilize the PSU output voltage and to maintain a constant absorption from the electrical network. Therefore, the *base functional test* approach may not be sufficient in

closed-loop electric systems. The *Observability enhanced functional test* was able to detect the thermal faults considered, but it had the same problem of physical accessibility to the device already discussed for the *in-circuit thermal test*. Figure 10 shows the pins of the power devices accessible by ATE for the PCB case study.

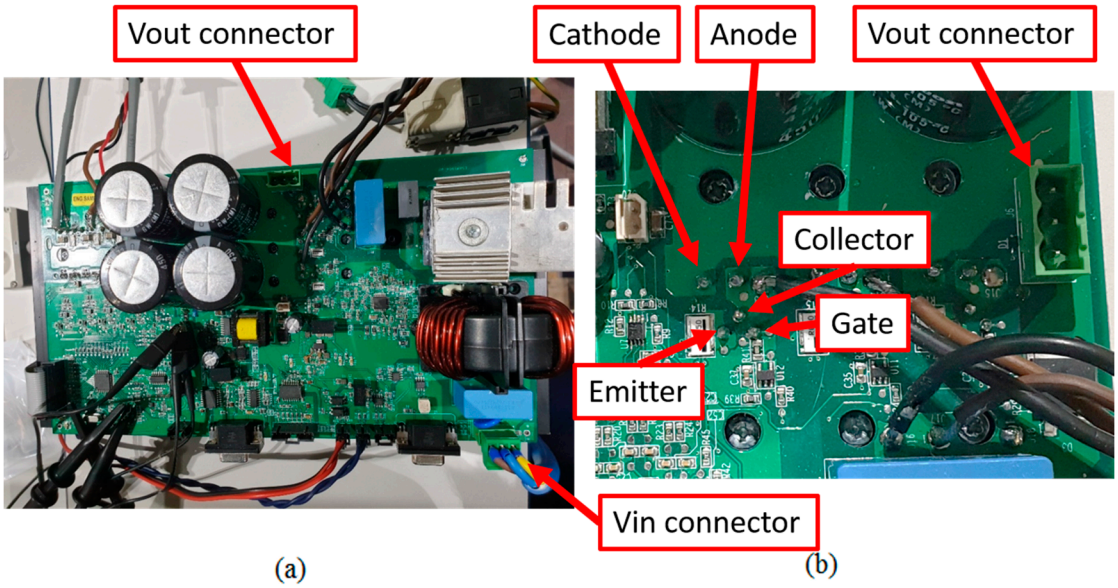

Figure 10. (**a**) PCB surface; (**b**) Contact points accessible from the Automatic Test Equipment (ATE).

The simulations were performed using the PLECS circuit simulator [33]. PLECS is a behavioral simulator specifically designed for simulating power circuits. Each simulation required about 20 min of CPU time on a PC equipped with an 8-core AMD FX-8370 processor operating at 4 GHz and 32 GB of 1333 RAM memory.

6. Conclusions

The growing use of power electronics in safety-critical applications requires accurate test strategies even for those aspects usually not considered, such as the heatsinks assembled on the power devices. The junction temperature increase is the main cause of ageing, mechanical stress, and breakage of the power devices. This paper highlights the importance of testing some aspects normally not considered, such as heatsinks. An incorrect assembly of the heatsink causes an increase of the temperature inside of the power devices. This paper reiterates the concept of thermal fault associated with the heatsink assembly. Some thermal fault resistances were considered in the thermal model of the cooling system. The values of the thermal fault resistances were calculated so as to bring the junction temperature of the power device to the maximum temperature supported, i.e., outside the operating parameters defined by the device manufacturer.

The paper proposes a methodology to assess the effectiveness of different test strategies using a thermal model of the cooling system. Some thermal faults associated with the heatsink assembly were considered in the cooling system thermal model. The results obtained with the different test strategies can be compared for identifying the best test strategy among those considered.

In this paper, we consider three different test strategies to detect the presence of thermal faults associated with the heatsink's assembly. The considered tests strategies are based on the *in-circuit test* and the *functional test*. The tests considered can be easily performed by ATE on the final PCB. The advantages and disadvantages of the three test strategies were evaluated in an industrial case study. In particular, the *in-circuit test* strategy can be used when the circuit allows it, i.e., when the test is not inhibited by any other devices present on the PCB. The *base functional test* approach is not able to detect thermal faults; it is necessary to use an improved version of the *basic functional test* approach as

the *observability enhanced functional test*. The *observability enhanced functional test* strategy allows for the identification of the thermal faults when it is possible to perform further measurements on the PCB during the functional test. Moreover, it is possible to introduce additional *test points* on the PCB during the PCB design phase. These *test points* allow the ATE to perform measurements in points normally inaccessible on the PCB. It should be remembered that the addition of *test points* increases the PCB complexity because it introduces additional traces on the PCB. As a case study, a PSU composed of different power devices was considered.

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