Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers

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Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers †

Pedro Toledo [1,2,*], Paolo Crovetti [1], Hamilton Klimach [2] and Sergio Bampi [2]

[1] Department of Electronics and Telecommunications (DET), Politecnico di Torino, 10129 Turin, Italy; paolo.crovetti@polito.it

[2] Graduate Program in Microelectronics (PGMICRO), Federal University of Rio Grande do Sul, 91501-970 Porto Alegre, Brazil; hklimach@gmail.com (H.K.); Bampi@inf.ufrgs.br (S.B.)

* Correspondence: pedro.leitecorreia@polito.it

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Abstract: The calibration of the effects of process variations and device mismatch in Ultra Low Voltage (ULV) Digital-Based Operational Transconductance Amplifiers (DB-OTAs) is addressed in this paper. For this purpose, two dynamic calibration techniques, intended to dynamically vary the effective strength of critical gates by different modulation strategies, i.e., Digital Pulse Width Modulation (DPWM) and Dyadic Digital Pulse Modulation (DDPM), are explored and compared to classic static calibration. The effectiveness of the calibration approaches as a mean to recover acceptable performance in non-functional samples is verified by Monte-Carlo (MC) post-layout simulations performed on a 300 mV power supply, nW-power DB-OTA in 180 nm CMOS. Based on the same MC post-layout simulations, the impact of each calibration strategy on silicon area, power consumption, and OTA performance is discussed.

Keywords: ultra-low-voltage; operational transconductance amplifier (OTA); digital-based OTA (DB-OTA); fully-digital design; dynamic calibration; static calibration

1. Introduction

Small dimensions and low power consumption are critical requirements of pervasive, (nearly) energy autonomous sensor nodes for the Internet of Things (IoT) [1–4], Figure 1a. While digital circuits can be extremely power- and area-efficient thanks to geometry, voltage and frequency scaling [5], analog circuits are still lagging behind and their performance can be severely degraded in new CMOS technologies nodes due to the limited voltage headroom, high process variability and poor analog characteristics of nanoscale transistors [6].

Focusing on the Operational Transconductance Amplifier (OTA), which is a key building block in most analog sub-systems, several new topologies and design techniques (Figure 1b–g) have been recently devised to enable efficient operation in nanoscale technologies and/or under Ultra-Low-Voltage (ULV) supply [7–16].

In general, ULV OTAs can be classified as: gate-driven , bulk-driven , inverter-based , VCO-based and digital-based [15,16] topologies.

In [8,9] gate-driven MOS transistors working in subthreshold regime are exploited (Figure 1b) and the minimum power supply and common mode input range (CMIR) are limited to $V_{DD} = 3V_{sat} \approx$

300 mV and $V_{CM} = V_{DD} - 2V_{sat} - V_{TH}$, respectively, being V_{sat} the minimum drain-source voltage required to operate an MOS device in saturation voltage and V_{TH} is the threshold voltage.

In [10] (Figure 1c), bulk-driven input devices are exploited to mitigate the CMIR limitation, at the cost of reduced efficiency due to the lower values of the bulk transconductance g_{mb} compared to the gate transconductance g_{mg} under the same bias. Inverter-based amplifiers [11,12] (Figure 1d–e) have been proposed to achieve a large equivalent transconductance ($g_{m_{TOTAL}} = g_{m_{PMOS}} + g_{m_{NMOS}}$) under low V_{DD} and voltage headroom. However, they suffer of limited intrinsic gain and common-mode rejection in nanometer-scale technologies.

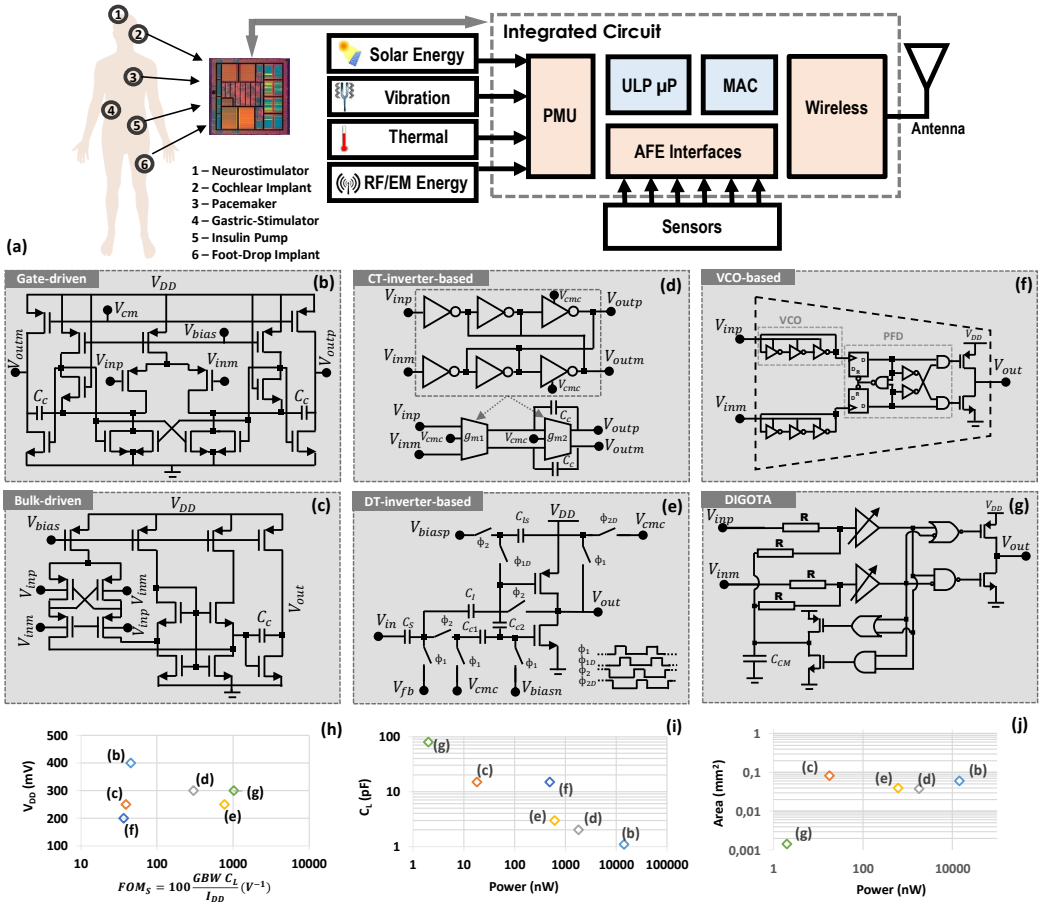

Figure 1. (**a**) General block diagram of an IoT energy-harvesting-enabled device, including its Power Management Unit (PMU), Analog Front-End (AFE) interfaces, ULP microprocessor (μP), Media Access Control (MAC) unit, Wireless unit. (**b**) Gate-driven [8,9], (**c**) Bulk-driven [10] (**d**,**e**) Inverter-based [11,12] (**f**) VCO-based [13,14] (**g**) Digital-based [16] topologies. ULV OTA state-of-art comparison plots: (**h**) V_{DD} (mV) versus $FOM_S = 100\frac{GBWC_L}{I_{DD}}$ (V^{-1}) (**i**) C_L (pF) versus Power (nW) (**j**) Area (mm^2) versus Power (nW).

An alternative approach [17–27] aims at the implementation of analog functions by digital means. Leveraging this concept, a VCO-based OTA [28] and a digital-based [15] OTA (DB-OTA), Figure 1f,g, have been recently proposed [13,16]. Both OTAs are based on time-domain information processing and prove to be very good candidates for efficient ULV operation. Their operation, however, can be impaired by process variations and mismatch, so that an ad-hoc calibration is required for acceptable yield [16,29]. The design of a calibration network for DB-OTAs is critical since it can possibly impair the versatility and limit the power and area advantage of these solutions. The design of a traditional calibration network, in particular, can be not compatible with DB-OTA implementations by small standard cell libraries and by Field Programmable Gate Arrays (FPGAs), in which a limited set of gates

is available and the geometrical dimensions of the calibration transistors cannot be finely tuned by the designer. At the same time, the dynamic calibration approach proposed in [29] to address these limitations results in increased power.

In this paper, the dynamic digital calibration (DDC) and static digital calibration (SDC) of DB-OTAs are addressed. In particular, the trade-off between area/power overhead and performance in post-calibrated Digital-Based OTAs [16,29], is deeply investigated on a 300 mV-power-supply 180 nm CMOS standard-cell DB-OTA by extensive post-layout simulations. Moreover, the possibility of replacing the Digital Pulse-Width Modulation (DPWM) adopted in [29] for DDC by Digital Dyadic Pulse Modulation (DDPM) [30], which shows better spectral properties for dithering purposes [31], is explored for the first time.

The paper is organized as follows: in Section 2, the DB-OTA operation and its limitations are described along with the classical SDC approach. Then, DPWM and DDPM modulations are introduced in Section 3, as well as their application in digital calibration to dynamically compensate the effects of process variations and device mismatch on DB-OTA offset. The effectiveness of the proposed calibration strategies and their impact on DB-OTA performance is then verified in Section 4 by Monte-Carlo (MC) post-layout simulation. In Section 5, some concluding remarks are drawn.

2. Digital-Based OTA

In this section, the operation of a DB-OTA [15,16] is revised highlighting the effects of process variations and mismatch that will be addressed by the calibration techniques considered in this paper.

2.1. Basic Operation

The schematic of the DB-OTA considered in this work is shown in Figure 2a. The circuit is intended to implement the functionality of an OTA by digital means, i.e. to amplify the differential component of the input signal $v_{\mathrm{d}} = V_{\mathrm{in}+} - V_{\mathrm{in}-}$ while rejecting the common mode component $v_{\mathrm{cm}} = \frac{V_{\mathrm{in}+}+V_{\mathrm{in}-}}{2}$.

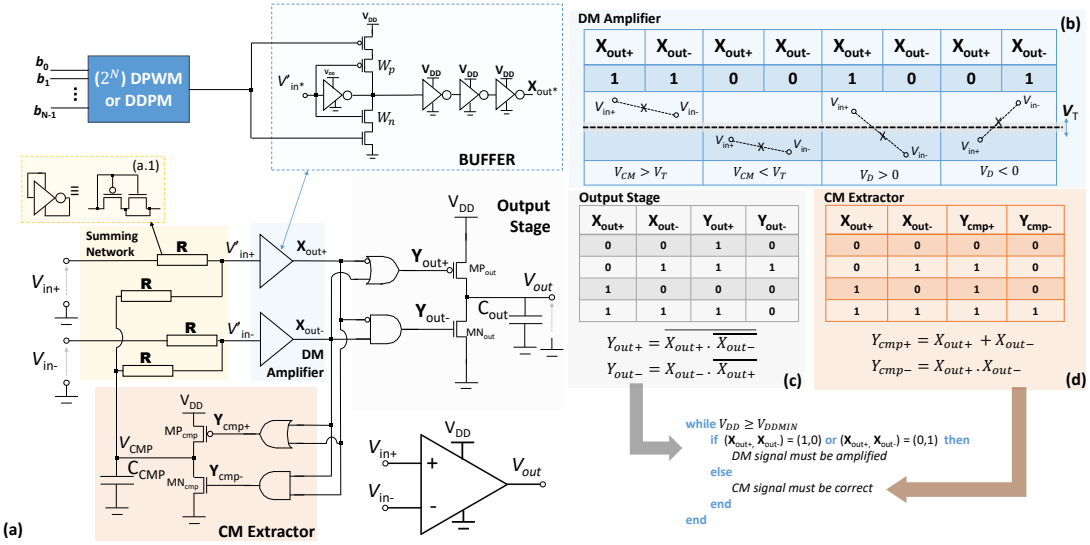

Figure 2. (**a**) ULV DB-OTA schematic (**b**) *DM Amplifier* analog input voltage tracking (**c**) *output stage* Boolean equations (**d**) *CM extractor* Boolean equations.

For this purpose, the DB-OTA includes a *Differential-Mode (DM) amplifier*, a *Common-Mode (CM) extractor* block, a *summing network*, and an *output stage*, as detailed in [16].

The *DM Amplifier* consists of two digital buffers which provide two logical outputs $X_{\text{out}+}$ and $X_{\text{out}-}$ depending on the level of the input voltages with respect to the trip points (V_{T}) of the voltage buffers, resulting in four possible cases:

$$(X_{\text{out}+}, X_{\text{out}-}) = (0,0), (1,1), (1,0), (0,1) \tag{1}$$

As shown in Figure 2b, whenever $(X_{\text{out}+}, X_{\text{out}-}) = (1,0), (0,1)$, it follows that $v_{\text{d}} > 0$ or $v_{\text{d}} < 0$ respectively, so the *output stage* needs to be activated to increase or decrease V_{out}, accordingly. For this purpose the gate signals given by the Boolean equations in Figure 2c are applied to the *output stage*.

When $(X_{\text{out}+}, X_{\text{out}-}) = (0,0), (1,1)$, the transistors MN_{cmp} (MP_{cmp}) of the *CM Extractor* are operated according to the Boolean equations in Figure 2d, to increase (decrease) the capacitor C_{CMP} voltage, V_{CMP}, which is added to the external inputs $V_{\text{in}+(-)}$ through the *summing network*:

$$V'_{\text{in}+(-)} = \frac{V_{\text{CMP}} + V_{\text{in}+(-)}}{2} \tag{2}$$

so that to compensate the CM input signal variations in the inputs $V'_{\text{in}+(-)}$ of the *DM Amplifier*. As described in [15], this behavior of the *CM Extractor* results in dynamic common mode tracking.

When the CM input component is within the CM input range, the transistors MP_{out} and MN_{out} are operated by digital pulses with a duration proportional to v_{d} so that to charge or discharge C_{OUT}. A more detailed analysis of the circuit can be found in [15].

2.2. Process Variations and Mismatch

The ULV DB-OTA operation can be severely impaired by process variations and mismatch in the trip points V_{T} [32] of the first inverters of the *DM amplifier*, which result in an input offset voltage [15]:

$$V_{\text{OFF}} = \Delta V_{\text{T}} + \frac{I_{\text{OUT}}}{C_{\text{OUT}}} \Delta t_{\text{D}} \tag{3}$$

where

$$\Delta V_{\text{T}} = V_{\text{T1}} - V_{\text{T2}} \tag{4}$$

is the difference of the trip points V_{T1} and V_{T2} of the first inverters, both expressed in terms of technology and geometrical parameters as:

$$V_{\text{T}} = \frac{\frac{\kappa T}{q} \log\left(\frac{I_{\text{D0}_{\text{P}}} \left(\frac{W}{L}\right)_{\text{P}}}{I_{\text{D0}_{\text{N}}} \left(\frac{W}{L}\right)_{\text{N}}} \right) + \frac{V_{\text{DD}}}{n_{\text{P}}}}{\frac{1}{n_{\text{P}}} + \frac{1}{n_{\text{N}}}}, \tag{5}$$

Δt_D is the difference in the propagation delays of the two branches of the OTA, I_{OUT} is the output stage current (assumed to be fixed for the sake of simplicity), $I_{\text{D0}_{\text{N(P)}}}$ is the zero-v_{GS} drain current of nMOS (pMOS) in weak inversion and it is process parameter dependent, $n_{N(P)}$ is the subthreshold slope factor of the nMOS (pMOS) device. All the other symbols have their usual meaning [32].

For minimum-size devices, the offset predicted by Equation (3) can be easily large enough to saturate the DB-OTA, thus fully impairing the DB-OTA operation, and needs to be compensated.

For this purpose, the dependence of the trip points of a CMOS inverter on the aspect ratios of the pull-up and pull-down devices, given by Equation (5), is leveraged in the post-fabrication SDC (Figure 3a) procedure proposed in [16], which makes it possible to tune the effective aspect ratio of either the pull-up or the pull-down branch by enabling/disabling binary weighted $2^i W_{\text{min}}$ transistors in parallel to first inverters of the DM amplifier, based on a 8-bit calibration code $b_{i,n}$ with $i = 0 \ldots N-1$.

This calibration procedure, however, is not compatible with a pure digital flow and requires extra area and analog design effort. In view of these limitations, all-Digital Dynamic Calibration (DDC)

based on DPWM has been first explored in [29] and will be further investigated in this work, together with an alternative DDC approach based on the DDPM modulation.

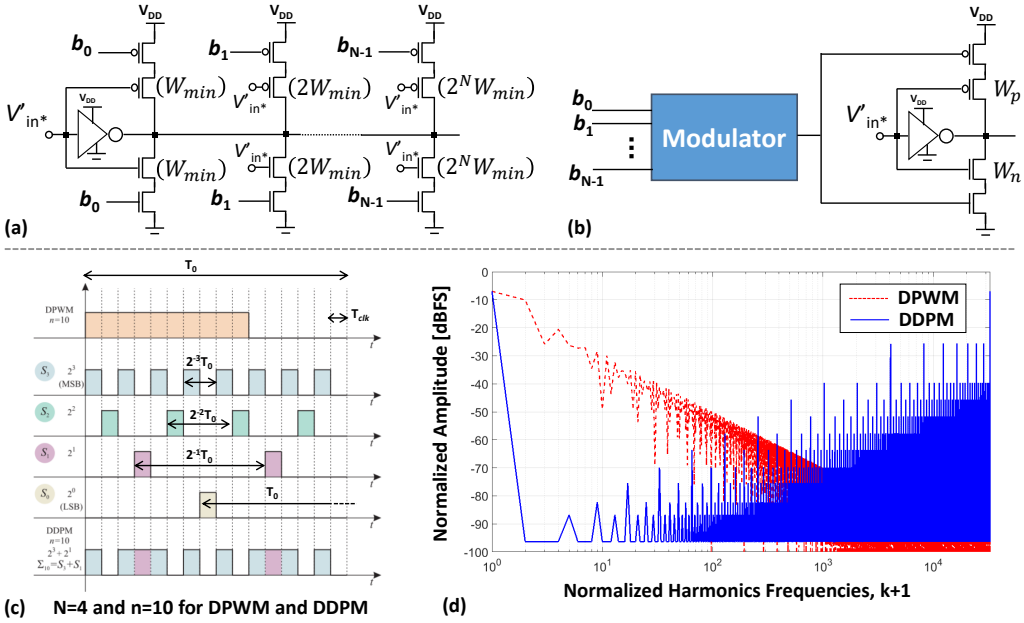

Figure 3. (**a**) N-bit static calibration (**b**) N-bit dynamic calibration (**c**) DDPM and DPPM waveforms for $N = 4$ and $n = 10$ (**d**) Normalized DPWM and DPPM spectrum for $N = 16$ and n = 29,365.

3. Dynamic Digital Calibration

In this section, the digital pulse width modulation (DPWM) and the dyadic digital pulse modulation (DDPM) are first introduced and then their application to DDC of a DB-OTA is proposed in Section 3.2.

3.1. Digital PWM (DPWM) Modulation

Pulse Width Modulation (PWM) is a technique intended to generate a low-frequency output by extracting the DC component $D \cdot V_{\mathrm{DD}}$ of a square wave with high level V_{DD}, low level 0 V, duty cycle D, and frequency $f_0 = \frac{1}{T_0}$ high enough to be conveniently filtered.

A Digital PWM (DPWM) signal with quantized duty cycle $D = n/2^N$ can be expressed as:

$$v_{\mathrm{DPWM},n}(t) = V_{\mathrm{DD}} \sum_{k=-\infty}^{+\infty} \Pi\left(\frac{t}{nT_{\mathrm{clk}}} - \frac{1}{2} - \frac{2^N}{n}k\right), \tag{6}$$

where

$$\Pi(x) = \begin{cases} 1 & |x| < \frac{1}{2} \\ \frac{1}{2} & |x| = \frac{1}{2} \\ 0 & |x| > \frac{1}{2} \end{cases}, \tag{7}$$

and

$$n = \sum_{i=0}^{N-1} b_{i,n} 2^i \tag{8}$$

in which T_{clk} is the bit period and $b_{i,n}$ are the binary digits of the number n represented by N unsigned bits. Such a signal can be generated as a digital stream at clock frequency $T_{\mathrm{clk}} = \frac{T_0}{2^N}$ consisting of n ones followed by $2^N - n$ zeros, as shown in Figure 3c.

Looking at the spectrum of a DPWM signal, which is plotted in red in Figure 3d for an input word n = 29,365 on $N = 16$ bits, it can be observed that most of the AC spurious spectral energy is

concentrated at low frequencies. As a consequence, a low pass filter with very steep transition from the pass band to the attenuated band is required to extract the DC component while suppressing low-frequency spurious components.

3.2. DDPM Modulation

In view of the limitations of DPWM discussed so far, the Dyadic Digital Pulse Modulation (DDPM) has been introduced in [30] as an alternative to DPWM for digital to analog conversion, so that to relax the low pass filter requirements while keeping the same mean value.

A DDPM stream $v_{\mathrm{DDPM},n}(t)$ for a given digital code n on N bits is defined as:

$$v_{\mathrm{DDPM},n}(t) = V_{\mathrm{DD}} \sum_{k=-\infty}^{+\infty} x_n(t - 2^N k T_{\mathrm{clk}}) \tag{9}$$

where

$$x_n(t) = \sum_{i=0}^{N-1} \sum_{h=0}^{2^i-1} b_{i,n} \Pi \left(\frac{t}{T_{\mathrm{clk}}} - 2^{N-i} h - 2^{N-i-1} - \frac{1}{2} \right) \tag{10}$$

and can be regarded as the linear superposition of N orthogonal dyadic basis functions consisting of 2^i non-overlapped T_{clk} pulses with $i = 1 \ldots N-1$ arranged so that to have more switching activities along the same T_0, as illustrated in the bottom waveform of Figure 3c, where a DDPM modulated signal for the same N and n chosen for the DPWM stream in the top waveform is shown.

The higher switching activity of a DDPM signal results in more spectral energy at high frequencies and less at low frequency harmonics, thus releasing the requirements of the low pass filter intended to extract its DC component. This as can be clearly observed in the DDPM spectrum plotted in blue in Figure 3d for the same input word (n = 29,365) and resolution (N = 16 bits) of the DPWM signal (spectrum in red curve).

3.3. Static and Dynamic Calibration Networks

The SDC and DDC based on DPWM and DDPM, which are considered and compared in this paper, are introduced in this Section.

3.3.1. Static Digital Calibration (SDC) Network

In Figure 3a, the post-fabrication SDC network adopted in [16] is depicted. Such a network comprises N inverters - in parallel with the DB-OTA input stage-with a strength scaled by $2^i W_{\mathrm{min}}$. Each of such inverters includes an MOS switch in series with the pull-up branch and one in series with the pull-down branch, which can be turned on/off so that to enable/disable more pull-up and pull-down branches in parallel to the DB-OTA input stage based on a digital calibration word, so that to achieve minimum input offset voltage by compensating process- and mismatch-related variations, as described by Equations (3)–(5).

3.3.2. Dynamic Digital Calibration (DDC)

The proposed Dynamic Digital Calibration (DDC) network, which consists of only one enabled-inverter driven by the input signals ($V_{\mathrm{in}-(+)}$) and also connected in parallel to the first stage of each branch in the *DM amplifier*, is depicted in Figure 3b. A DPWM or a DDPM modulator are then connected to the DDC network to modulate the input signal in the two proposed DDC implementations.

The operation of the calibration network can be described as follows. The pull-up (pull-down) network of the calibration inverter can be connected to the supply (to ground) through a pMOS (nMOS) power gating switch. When the pMOS (nMOS) gating switch is on, the pMOS (nMOS) of the calibration inverter, with width W_{n} (W_{p}) is enabled and connected in parallel to the nMOS (pMOS)

device in the first stage of the *DM amplifier*, thus effectively increasing its width and significantly reducing (increasing) its trip point according to Equation (5).

When the gating switches are periodically operated with frequency $f = \frac{1}{T_0}$ larger than the DB-OTA GBW, it is observed that periodically enabling the gates has the same net effect on the trip points of the DM amplifier gates as increasing the width of the DM amplifier devices by a fraction DW_n (DW_p) of the calibration inverter width W_n (W_p), being $D = \frac{T_{EN}}{T_0}$ the effective enabling duty cycle, where T_{EN} is the overall time the calibration inverter is enabled over the period T_0. This approach is adopted in what follows for dynamic offset calibration of the OTA, considering both DPWM and DDPM streams as gating signals for the calibration inverter.

4. Simulation Results

To compare the calibration approaches (SDC and DDC using DPWM and DDPM modulations), a DB-OTA designed in CMOS 180 nm technology has been considered [16,29]. The DB-OTA layout, including the SDC calibration network, occupies less than 1500 µm^2 silicon area, as shown in Figure 4a.

In [16], the proposed DB-OTA performs amplification at $V_{DD} = 300$ mV power supply driving up to 80 pF C_{LOAD} and its nominal performance, verified by post-layout simulations, are summarized in the next subsection. Then, the feasibility to replace the SDC network introduced in [16] by the DDCs described above is verified by post-layout MonteCarlo simulations.

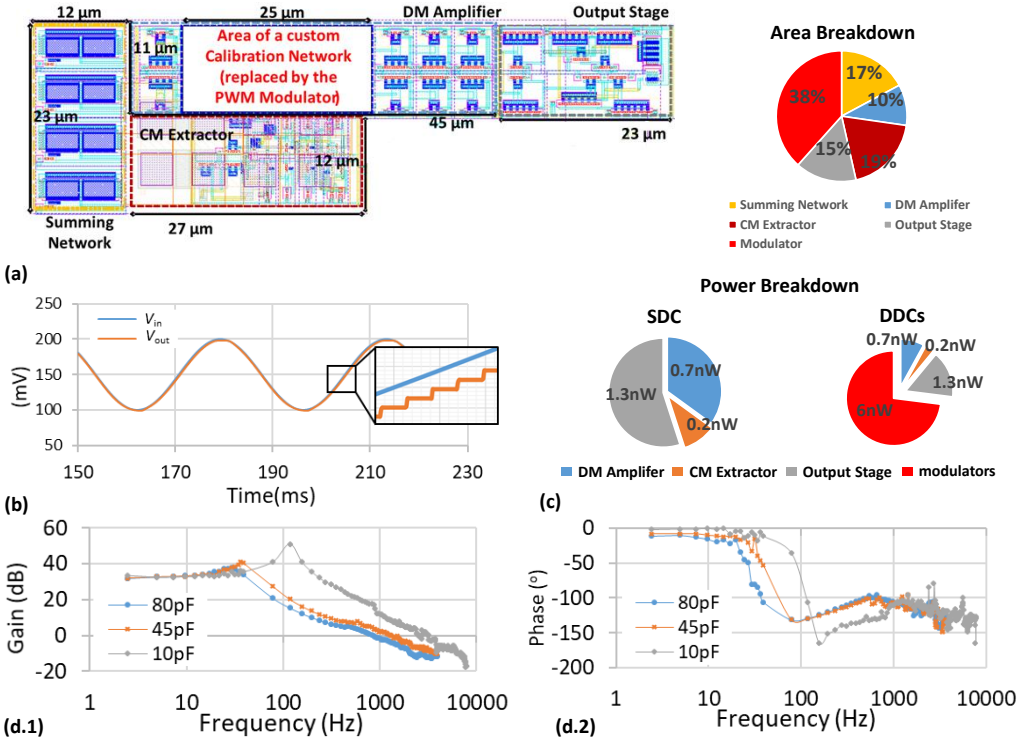

Figure 4. (**a**) DB-OTA layout and Area breakdown (**b**) V_{in} and V_{out} at 30 Hz frequency, 50 mV peak amplitude and $C_{out} = 80$ pF (**c**) Power breakdown (**d.1**,**d.2**) ULV DB-OTA frequency response.

4.1. Performance under Nominal Conditions

The input and output waveforms of the ULV DB-OTA operated at $V_{DD} = 300$ mV and connected in the voltage follower configuration, with a sine wave input at 30 Hz frequency, 50 mV peak amplitude and $C_{out} = 80$ pF are reported in Figure 4b. In this configuration, a THD less than 2% and 2 nW power consumption are achieved. In the same figure, a detail of the waveform reveals the step-wise changes in v_{out} related to the intrinsic digital characteristic of the DB-OTA [15]. The ULV DB-OTA frequency response, calculated through Fast Fourier Transform (FFT) analysis of transient simulations, as done in

[16], is reported in Figure 4d for $C_{LOAD} = 10, 45, 80\,\text{pF}$. According to that, the DB-OTA shows 35 dB DC gain and 0.85, 1.3 and 2.48 kHz Gain Bandwidth Product (GBW) with phase margins 76°, 68.5° and 57°, respectively.

4.2. Process Variations, SDC and DDC comparison

The DB-OTA without calibration has been simulated under process variations for the same voltage follower configuration as in Section 4.1 and for $V_{\text{amp}} = 50\,\text{mV}$, $C_{\text{out}} = 80\,\text{pF}$ and $f_{\text{in}} = 30\,\text{Hz}$ by Montecarlo (MC) simulations on 100 samples. The statistical sampling method used within the MC analysis was the low-discrepancy sequence sampling (LDS) to get evenly distributed samples over the statistical space.

The V_{in} and V_{out} simulated waveforms for a bad sample resulting from this analysis are shown in Figure 5a. Mainly due to mismatch in the *DM amplifier* first inverter, the output signal of this sample is pushed towards V_{DD} distorting the signal and increasing the offset voltage.

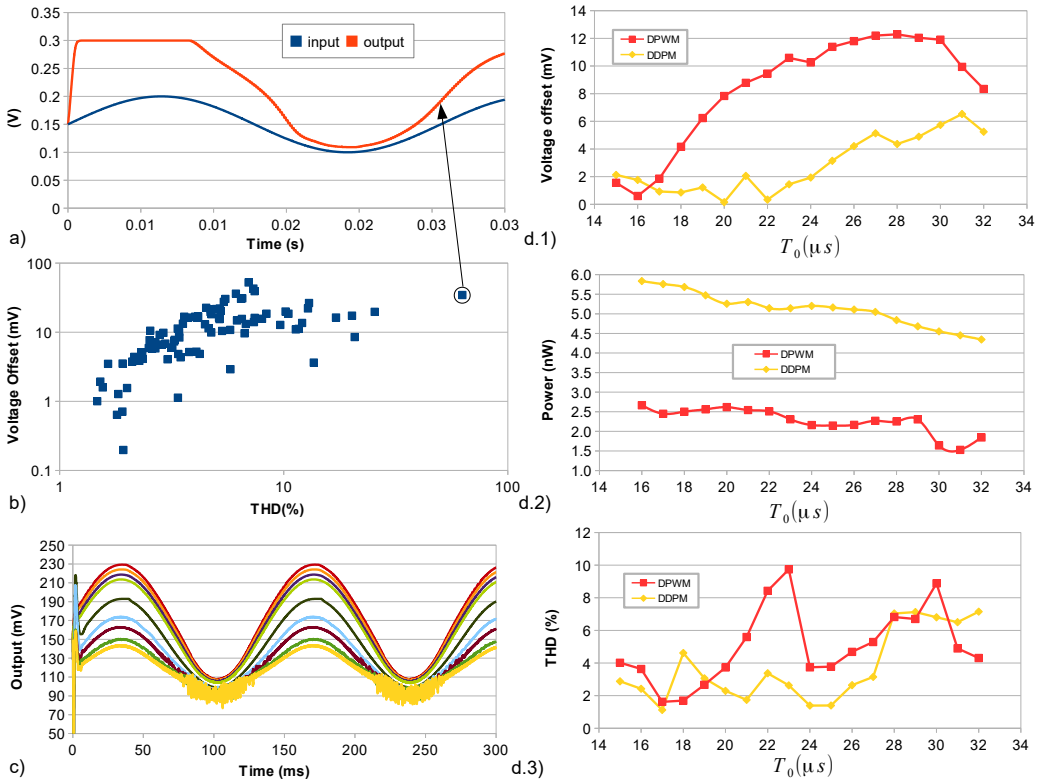

Figure 5. (**a**) V_{in} and V_{out} of a bad sample from the MC analysis with 30 Hz frequency, 50 mV peak amplitude and $C_{\text{out}} = 80\,\text{pF}$ (**b**) Thumbnail plot between THD (%) and Voltage offset (mV)—each point is a sampe of the MC simulation (**c**) Changing the BD-OTA offset through DDC using the DPWM modulator (**d.1**,**d.2**,**d.3**) Trade-off between power and signal integrity (THD) versus T_0.

To gain more insight about the effects of process variations, a scattered plot of the THD (%) and offset voltage (mV) for the 100 MC samples is depicted in Figure 5b. This analysis reveals that more than 50% of the samples show an offset exceeding 10 mV or a THD of more than 5%, confirming the relevant impact of process variations on the DB-OTA performance. The same analysis also reveals a significant correlation between THD and offset (Pearson's correlation coefficient of 40%). As a consequence, if the offset is attenuated by calibration, the THD can be also improved and minimum offset voltage can be conveniently targeted as a global calibration goal.

In view of that, the SDC and DDC have been adopted and compared in the following to tweak the offset the DB-OTA as shown Figure 5c. The calibration simulation flow and the results of the simulations are discussed in what follows.

4.2.1. SDC and DDC Simulation Flow

The high-level simulation flow illustrated in Figure 6 has been adopted to compare the SDC and DDC techniques considered in this paper. After performing a first MC without calibration by LDS statistical sampling method (step #1), statistical corners are created for each sample in the Cadence environment, so that to get direct access to each sample keeping fixed the random number generator seed in MC simulations (step #2). Next (step #3), SDC and DDC techniques are systematically applied to each sample so that to find the 3-bit calibration code (to be applied as an input decoder enabling the calibration network in SDC and as the DPWM/DDPM modulators input words for DDC) which minimizes the simulated input offset voltage. Calibration signals applied just to the non-inverting input branch have been considered to reduce power and area overhead. In step #4, the results are post-processed to evaluate the main DIGOTA performance, which are presented and discussed in what follows.

Figure 6. High-level simulation flow adopted in the assessment of SDC and DDC techniques.

4.2.2. SDC and DDC Statistical Characterization

The calibrated DB-OTA input offset voltage, power (DB-OTA alone) and THD evaluated by the simulation flow in Figure 6 for one representative sample are plotted in Figure 5d versus the period T_0 of DDPM and DPWM calibration patterns applied to the enabling transistors in Figure 3b, revealing that improved offset and THD (both slightly better for DDPM compared to DPWM, as expected in consideration of the better spectral characteristics of the DDPM modulation.) can be achieved at lower T_0 at the cost of an increased power consumption, which is more relevant for DDPM, in view of the higher switching activity. An extra power overhead of around 6 nW and silicon area of 25 µm × 25 µm should be also taken into account for DPWM and DDPM modulators [29]. Trading off power and accuracy, a different period $T_0 = 24$ µs for DPWM and 32 µs for DDPM have been considered as an optimal choice for the two DDC strategies.

To make a fair comparison over different samples, SDC and DDCs have been considered to trim a population of 100 samples keeping the same MC seed used in Figure 5b. Optimal 3-bit calibration words leading to minimum input offset voltage have been first identified for each sample for SDC, and both the DPWM and the DDPM DDC techniques. Then, such optimal calibration words have been applied in simulations, so that to compare the performance statistics of the calibrated samples.

The histogram of the DB-OTA voltage offset is reported in Figure 7a before and after calibration. Without calibration (blue bars), the mean (μ) and standard deviation (σ) are 12.26 mV and 9.29 mV, respectively. Using the SDC (green bars), $\mu = 3.15$ mV and $\sigma = 2.9$ mV have been achieved. As far as DDC is concerned, the simulated mean value and standard deviation are 6.86 mV and 5.8 mV, respectively for DPWM (red bars) and 8.19 mV and 5.34 mV for DDPM (yellow bars). The histograms of THD, Power, GBW and $FOM_S = 100\,\frac{GBW \cdot C_{Load}}{I_{DD}}$ for the calibrated samples are reported in Figure 7b–e.

In Table 1, the mean and standard deviation of each performance parameter before calibration and for the SDC and DDC calibration techniques are compared. The DDC shows an average offset reduction of 1.79X for DPWM and 1.5X for DDPM modulation, increasing the THD yield by 1.3X and 1.2X, respectively, for 5% THD as threshold.

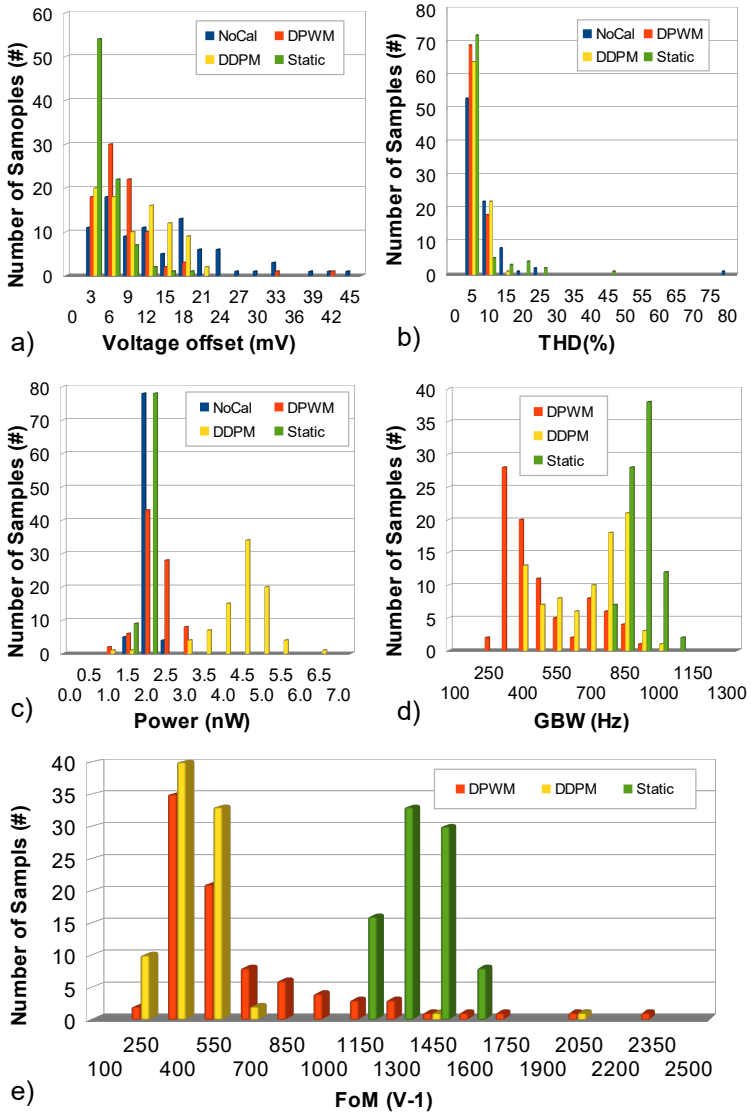

Figure 7. (**a**) Voltage offset (**b**) THD (**c**) Power (**d**) GBW (**e**) and $FOM_S = 100\frac{GBWC_{Load}}{I_{DD}}$ histograms.

Table 1. Monte Carlo simulation results: statistics parameters.

Peformance	No Calibration	Static	DPWM	DDPM
Voltage Offset (mV)	$\mu = 12.26, \sigma = 9.29$	$\mu = 3.15, \sigma = 2.9$	$\mu = 6.86, \sigma = 5.8$	$\mu = 8.19, \sigma = 5.34$
THD (%)	$\mu = 6.17, \sigma = 8.65$	$\mu = 4.6, \sigma = 6.18$	$\mu = 3.61, \sigma = 1.82$	$\mu = 4.16, \sigma = 2.04$
Power (nW)	$\mu = 1.73, \sigma = 0.15$	$\mu = 1.65, \sigma = 0.13$	$\mu = 1.95, \sigma = 0.41$	$\mu = 4.12, \sigma = 0.78$
GBW (nW)	-	$\mu = 865.9, \sigma = 63.3$	$\mu = 434.4, \sigma = 174.28$	$\mu = 643.99, \sigma = 166.65$
FoM (V^{-1})	-	$\mu = 1269.5, \sigma = 127.7$	$\mu = 592.11, \sigma = 385.17$	$\mu = 402.13, \sigma = 227.21$

In Table 2, a comparison with state of the art ULV OTAs reveals competitive performance also for the worst case sample after calibration. It is worth to stress that worst case sample term is used here to define the sample with highest THD and highlighted in Figure 5b.

Table 2. Comparison with the state-of-the-art Ultra-Low-Voltage Operational Transconductance Amplifier.

										This Work *				
										Calibration of the Worst Sample				
Performance	[10] +	[11] *	[13] *	[33]	[34] +	[35]	[36] +	[37] +	[38] +	**Typ.**	**Uncal.**	**Static**	**DPWM**	**DDPM**
Tech. (nm)	130	130	65	65	180	65	350	65	180	180	180	180	180	180
Supply (mV)	250	300	200	350	500	300	600	250	300	300	300	300	300	300
DC Gain (dB)	60	49.8	-	43	52	60	69	70	98.1	35	-	32	27	26
GBW (kHz)	1.88	9100	60	3600	1200	70	11.4	9.5	3.1	0.85	-	0.836	0.67	0.69
Slew Rate ($\frac{V}{ms}$)	0.7	3800	10.5	5600	2890	25	14.6	2	9.1	0.5	-	-		
THD (%)	0.2	-	-	0.6	1	-	0.08	-	0.49	3	77	1.32	2.73	2.35
Phase Margin (°)	52.5	76	-	56	-	53	65	89.9	54	76	-	70	67	68
C_{out} (pF)	15	2	15	3	20	5	15	15	30	80	80	80	80	80
Power (nW)	18	1800	492	17,000	110,000	51	550	26	13	2	1.18	1.81	1.15 ⋆	3.8 ⋆
Area (μm^2)	83,000	-	-	5000	26,000	3000	60,000	2000	9800	1426	1426	1426	1426 ⋆	1426 ⋆
FOM_S (V^{-1})	39.2	303	36.6	22.3	11	205	19	137	215	1020	-	1108	1397 ⋆	434.76 ⋆

+ experimental; * simulation; ⋆ The power and area overhead from the modulators are not included.

4.3. Discussion

Based on the results presented in Figures 3 and 7 and Table 1, both the traditional SDC and the novel DDC techniques considered in this paper have been shown to be effective in mitigating the adverse effects of process variations and mismatch in a DB-OTA circuit, so that to recover proper functionality even for the worst samples.

Moreover, it is observed that in both the proposed DPWM and DDPM DDC techniques, calibration accuracy is related to the period T_0 of the dynamic calibration signal and is traded off with an increased power consumption in the DB-OTA circuit and in the modulator. Comparing DPWM and DDPM, a higher accuracy is observed for DDPM in Figure 3 up to longer periods T_0, in view of the spectral characteristics of the DDPM modulation. By the way, this advantage is offset by the higher switching activity of DDPM, which also results in higher power consumption compared to DPWM.

Comparing DDC and SDC techniques on the same samples in Figure 7 and Table 1, traditional SDC, which requires a semi-custom flow, appears to be preferable to DDC in view of the reduced power overhead and better accuracy. At the same time, DDC, which is fully compatible with a digital flow, provides an effective opportunity to calibrate process and mismatch variations in DB-OTA synthesized by small standard-cell libraries or implemented by FPGAs, where the aspect ratio of calibration devices is not fully under the control of the designer and SDC is therefore not a viable option.

5. Conclusions

The effectiveness of fully digital dynamic calibration techniques based and DPWM and DDPM modulations in compensating the adverse effect of process variations and mismatch in ULV DB-OTAs has been analysed and compared to a classical static calibration approach. In particular, the effectiveness of dynamic calibration techniques on non-functional DB-OTA samples has been demonstrated with reference to an ULV DB-OTA designed in 180 nm CMOS and operating at 300 mV supply. Based on the results of Monte-Carlo (MC) post-layout simulations, a 1.79X and 1.5X offset voltage reduction and a THD yield enhancement by 1.3X and 1.2X have been achieved by DPWM and DDPM DDC, respectively, while keeping reasonable performance compared with the current ULV state-of-the-art OTAs and at the cost of small extra silicon area and power consumption.

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Abbreviations

The following abbreviations are used in this manuscript:

MDPI	Multidisciplinary Digital Publishing Institute
ULV	Ultra Low Voltage
DB-OTAs	Digital-Based Operational Transconductance Amplifiers
DPWM	Digital Pulse Width Modulation
DDPM	Dyadic Digital Pulse5Modulation
MC	Monte-Carlo
IoT	Internet of Things
CMOS	Complementary Metal-Oxide Semiconductor
MOS	Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifier
VCO	Voltage Controlled Oscillator
CMIR	Common Mode Input Range

PMU	Power Management Unit
AFE	Analog Front-End
ULP	Ultra Low Power
μP	microprocessor
MAC	Media Access Control
SDC	Static Digital Calibration
DDC	Dynamic Digital Calibrations
DM	Differential-Mode
CM	Common-Mode
GBW	Gain Bandwidth Product
THD	Total Harmonic Distortion
FFT	Fast Fourier Transform

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