

Fully Depleted MAPS in 110-nm CMOS Process With 100–300-m Active Substrate

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Fully Depleted MAPS in 110-nm CMOS Process With 100–300-m Active Substrate / Pancheri, Lucio; Giampaolo, Raffaele A.; Salvo, Andrea Di; Mattiazzo, Serena; Corradino, Thomas; Giubilato, Piero; Santoro, Romualdo; Caccia, Massimo; Margutti, Giovanni; Olave, Jonhatan Elias; Rolo, Manuel; Rivetti, Angelo. - In: IEEE TRANSACTIONS ON ELECTRON DEVICES. - ISSN 0018-9383. - 67:6(2020), pp. 2393-2399. [10.1109/TED.2020.2985639]

*Availability:*

This version is available at: 11583/2828873 since: 2020-05-23T17:21:32Z

*Publisher:*

IEEE

*Published*

DOI:10.1109/TED.2020.2985639

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# Fully Depleted MAPS in 110-nm CMOS Process With 100–300- $\mu\text{m}$ Active Substrate

Lucio Pancheri<sup>1</sup>, Member, IEEE, Raffaele A. Giampaolo, Andrea Di Salvo, Serena Mattiazzo<sup>2</sup>, Thomas Corradino, Piero Giubilato, Romualdo Santoro<sup>3</sup>, Massimo Caccia<sup>4</sup>, Giovanni Margutti, Jonhatan E. Olave, Manuel Rolo, and Angelo Rivetti

**Abstract**—This article presents a fully depleted monolithic active pixel sensor technology compatible with a standard deep submicrometer 110-nm CMOS process. Passive test pixels structures, produced in various flavors, have proved the feasibility of 100- and 300- $\mu\text{m}$ -thick active substrates. Active pixel sensors with monolithically integrated analog and digital electronics, consisting of a  $24 \times 24$  array of pixels with 50- $\mu\text{m}$  pitch, have been shown to be fully functional when operating in the full depletion mode. Characterization results obtained with a proton microbeam and a  $^{55}\text{Fe}$  radiation source are presented and discussed.

**Index Terms**—CMOS, monolithic active pixel sensor (MAPS), radiation detector, silicon.

## I. INTRODUCTION

MONOLITHIC active pixel sensors (MAPSs) are emerging as a viable alternative to hybrid pixels in charged-particles' detection and high-energy photons imaging, showing advantages in both performance and overall costs per unit area [1]–[3].

The reconstruction with the highest precision of the perigee parameters of charged-particle trajectories in a dense

environment calls for pixel pitches of tens of micrometers, low material budget, a high signal-over-noise ratio, and limited diffusion of the charge carriers originated by the impinging particle. These specifications can be obtained with a monolithic design implemented on a fully depleted (FD) high-resistivity substrate. As a consequence, FD-MAPSs are raising a significant interest in the high-energy physics community [4], [5].

FD-MAPSs have also been proposed for X-ray imaging [6], where an active substrate of 300–500  $\mu\text{m}$  would enable an efficient detection of photon energies up to 15 keV. Other applications, such as medical particle tomography and tracking in space experiments, would benefit from the low material budget, fine pixel pitch, and low power consumption offered by MAPS sensors [7], [8].

As a general trend in the development of pixel sensors, the complexity of on-chip digital functions is increasing, making it easier to integrate and deploy a complete sensor system. Moreover, event-driven readout schemes are frequently adopted to reduce power consumption and, in turn, relax the requirements of the cooling systems, impacting on the overall system material budget. To these purposes, very scaled process nodes should be used to reduce the area and to increase the speed of on-chip digital electronics.

The latest FD-MAPS design efforts in the high-energy physics community are adopting 180- and 150-nm process nodes. Most of the developments, in this respect, have been devoted to the implementation of devices with a depletion region ranging from a few tens of micrometer and hundreds of micrometer [4], [5]. In [4], large depletion regions are obtained by including the electronics inside a deep n-well that is used as a collection node for the electrons generated by the incident charged particles. This approach has demonstrated an excellent radiation hardness and a fast charge collection, but the sensor capacitance is relatively large, and a nonnegligible part of the pixel area cannot be used to accommodate the readout circuits. Scaling to very small pixels is thus very challenging while using such topology.

An alternative approach, arising from an evolution of the pixels designed for the ALICE detector [1], uses small sensing nodes while implanting a low-doped n-type region below the electronics [5]. In this way, most of the generated charges can be collected by drift, while the area and the capacitance of the sensors are maintained small, granting scalability toward

Manuscript received February 7, 2020; revised March 30, 2020; accepted March 30, 2020. This work was supported in part by the Istituto Nazionale di Fisica Nucleare (INFN), CSN5, and in part by the H2020 Project AIDA-2020 under Grant 654168. The review of this article was arranged by Editor J. Huang. (Corresponding author: Lucio Pancheri.)

Lucio Pancheri and Thomas Corradino are with the Dipartimento di Ingegneria Industriale, TIFPA Istituto Nazionale di Fisica Nucleare (INFN), Università di Trento, 38123 Trento, Italy (e-mail: lucio.pancheri@unitn.it).

Raffaele A. Giampaolo and Andrea Di Salvo are with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy, and also with the Istituto Nazionale di Fisica Nucleare (INFN)—Torino, 10125 Turin, Italy (e-mail: raffaeleaaron.giampaolo@to.infn.it; andrea\_disalvo@polito.it).

Serena Mattiazzo and Piero Giubilato are with the Dipartimento di Fisica e Astronomia, Istituto Nazionale di Fisica Nucleare—Sezione di Padova, Università di Padova, 35131 Padua, Italy (e-mail: serena.mattiazzo@unipd.it; piero.giubilato@unipd.it).

Romualdo Santoro and Massimo Caccia are with the Dipartimento di Scienze ed Alta Tecnologia, Università dell'Insubria, 22100 Varese, Italy, and also with the Istituto Nazionale di Fisica Nucleare—Sezione Milano.

Giovanni Margutti is with LFoundry S.r.l., 67051 Avezzano, Italy.

Jonhatan E. Olave, Manuel Rolo, and Angelo Rivetti are with the Istituto Nazionale di Fisica Nucleare—Torino, 10125 Turin, Italy.

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Digital Object Identifier 10.1109/TED.2020.2985639

small pixel sizes. This approach, although excellent for particle tracking, cannot be easily extended to an active thickness in excess of  $100\ \mu\text{m}$  since the space-charge region extends from the top surface of the sensor, thus limiting the applicable voltage at the sensor top side.

The possibility of FD thick substrates in CMOS-integrated sensors has been first explored in [9], demonstrating an FD sensor with p-type substrate and a n-type backside implantation. In the first prototype, the electronics were made entirely of p-type transistors. A similar approach was adopted in [10], using a CMOS process with n-type substrates and implanting a p+ region on the back.

Full depletion can also be obtained using a silicon-on-insulator process. Although the radiation damage of the insulator oxide poses several challenges related to parameter drift in the transistor characteristics, the latest advancements have greatly improved the radiation hardness of the process, and sensors with depletion regions up to  $500\ \mu\text{m}$  thick have been demonstrated [11].

In this article, we present a technology platform for the implementation of FD MAPS based on a modified 110-nm CMOS process. The process node was chosen to enable the in-pixel implementation of complex digital functions while keeping low prototyping and production costs. Backside processing was used to create a junction on the bottom surface that is biased to deplete the whole sensor substrate.

This article is structured as follows. Section II discusses the simulated characteristics with reference to geometry and process parameters. In Section III, the design of pixel test structures and a small array of active pixels with integrated electronics are presented. Section IV presents the results of the characterization of the arrays compared with the expectations according to the simulation. The perspectives for this technology are highlighted in Section V.

## II. SENSOR CONCEPT

The process was developed starting from a 110-nm industrial CMOS with 1.2-V transistors and six metal layers. A few add-ons were necessary to allow for full substrate depletion with electron collection at the sensing electrodes. A concept cross section of the pixel array is shown in Fig. 1 [12].

The standard p-type substrate was replaced with an n-type floating zone material. Wafer thinning and backside lithography were necessary to introduce a junction at the bottom surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side. A shallow boron-doped region was implanted on the rear side of the wafer, and the dopants were activated by laser annealing. Since, at large wafer thicknesses, the voltage needed for sensor full depletion exceeds  $150\ \text{V}$ , a termination structure composed of multiple guard rings was introduced.

A deep p-well scheme was used to prevent the n-wells hosting p-MOSFETs from collecting the charge generated by radiation in the substrate. Care had to be taken to limit the punchthrough current between the back-side junction and the deep p-well at sensor full depletion. A good control of punchthrough could be obtained either by increasing the bias

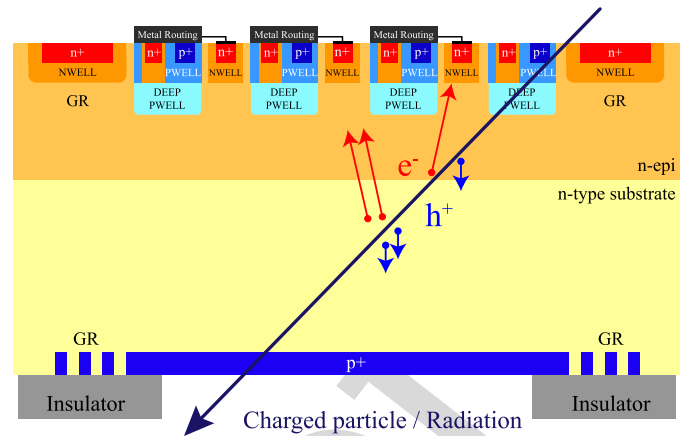


Fig. 1. FD pixel sensor cross section.

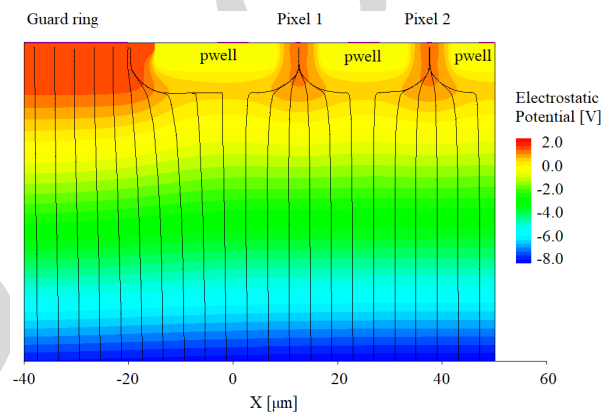
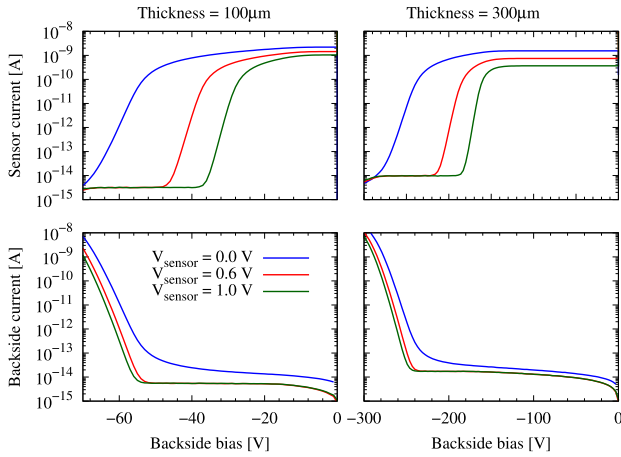


Fig. 2. Simulated 2-D potential profile and electric-field lines at full depletion. The simulation domain includes part of the guard rings and 2 pixels with  $25\text{-}\mu\text{m}$  pitch. Only the sensor surface region is shown.

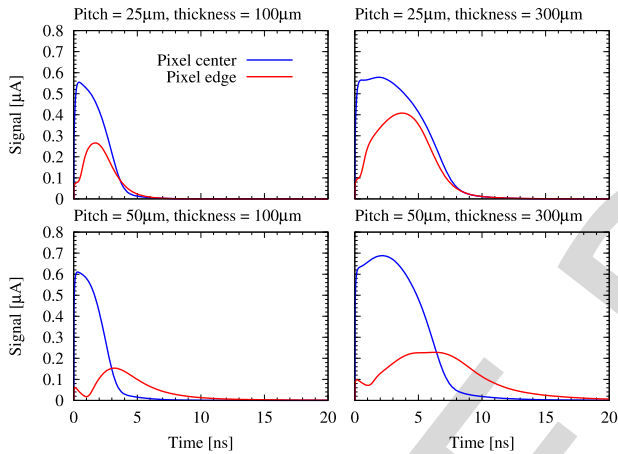
voltage at the pixel sensor nodes or by increasing the n-dopant concentration below the p-wells. Since the sensors had to be directly coupled to the low-voltage electronics, the second solution was adopted, by adding an n-doped epitaxial layer, having a resistivity lower than the substrate, to the process flow.

TCAD simulations were used to tune the process parameters. The simulated potential profile at full depletion for a domain, including 2 pixels and part of the surface guard ring, is shown in Fig. 2. Electric-field lines are orthogonal to the sensor surface up to the bottom of the deep p-wells, and then, they deviate horizontally toward the collection electrodes.

The full depletion and punchthrough voltages were simulated on this domain by introducing a small unbalance ( $10\ \text{mV}$ ) between pixel and guard ring bias voltages. The current flowing at the sensing electrodes and at the backside as a function of applied backside bias is shown in Fig. 3. At low reverse voltage, the substrate is not FD, and resistive paths exist between the pixels and the guard ring, leading to a macroscopic current. As the bias voltage is increased, a sharp current drop is observed, indicating the onset of full depletion. The depletion voltage is reduced by increasing the voltage applied at the front side to the sensor nodes. If the backside voltage is further increased, a punchthrough current starts flowing and



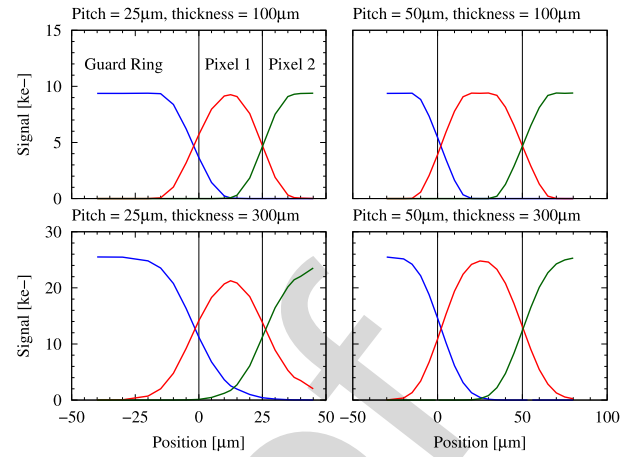
**Fig. 3.** Simulated sensor and backside current as a function of backside voltage for two values of sensor thickness [100  $\mu\text{m}$ , (left) and 300  $\mu\text{m}$  (right)]. Pixel pitch is 25  $\mu\text{m}$ .



**Fig. 4.** Simulated transient current signal with an incident MIP for two different values of sensor thickness [100  $\mu\text{m}$  (left) and 300  $\mu\text{m}$  (right)] and pixel pitch [25  $\mu\text{m}$  (top) and 50  $\mu\text{m}$  (bottom)].

eventually reaches very large values. The voltage difference between breakdown and punchthrough voltages depends on the sensor bias. At a sensor voltage between 0.6 and 1 V that can be applied if the sensor is directly coupled to the electronic readout channels, the difference between full depletion and punchthrough is a fraction of 10%–20% of the applied bias voltage. This value is large enough to reliably accommodate the operation of a pixel array, considered possible doping gradients and nonuniformities between the pixels.

Charge collection dynamics upon the incidence of a minimum ionizing particle (MIP) were also simulated. The MIP was modeled as a continuous charge density of 80 e–h pairs/ $\mu\text{m}$ , orthogonal to the sensor surface and extending throughout the sensor thickness. With reference to the simulation domain shown in Fig. 2, several positions of incidence were considered for the MIP. The current signal generated at the sensor is shown in Fig. 4 for two different MIP incidence positions, two values of pixel pitch (25 and 50  $\mu\text{m}$ ), and two values of sensor thickness (100 and 300  $\mu\text{m}$ ). As expected, complete charge collection is observed in less than 5 and 10 ns,



**Fig. 5.** Simulated collected charge at the sensor periphery as a function of the position of the incident particle for two different values of sensor thickness [100  $\mu\text{m}$  (top) and 300  $\mu\text{m}$  (bottom)] and pixel pitch [25  $\mu\text{m}$  (left) and 50  $\mu\text{m}$  (right)].

respectively, for 100 and 300  $\mu\text{m}$  thickness when the MIP is incident in the center of the pixel. If the MIP is incident at the pixel periphery, the collection speed depends on the pixel pitch; at 50- $\mu\text{m}$  pitch, the collection time approximately doubles since the charge generated in the substrate first reaches the bottom of the deep p-well and then drifts horizontally toward the collection node. Even considering this worst case situation, however, the charge is completely collected within 20 ns. In 25- $\mu\text{m}$  pixels, on the contrary, the collection time is only slightly degraded, as a result of the smaller horizontal distance traveled by electrons generated at the pixel periphery.

The integrated charge as a function of the MIP incidence position is shown in Fig. 5. Charge sharing between the pixels for two values of thickness and pixel pitch can be observed. As expected, sharing slightly increases by increasing the pixel pitch and sensor thickness, but, in all the cases considered here, the effect is confined to the nearest neighboring pixels.

### III. ACTIVE PIXEL ARRAY AND TEST STRUCTURES

A 576-active pixel array was designed as a test bench to validate the performance of the proposed technology [13], [14]. The pixels are organized in four sectors, each one consisting of 6 columns of 24 pixels. An end-of-column (EoC) block manages the column logic, handling pixel configuration and controlling data transmission. In this way, each sector works in parallel with the others. To read out the data for a single sector, two clocks are used. The first controls the shift register in the EoC to select the column, whereas the second one is dedicated to the row shift register. In a typical case, they, respectively, work at 5 and 0.2 MHz. Thus, the whole array can be read in less than 30  $\mu\text{s}$  using a 5-MHz clock.

A single 50- $\mu\text{m}$  pitch pixel hosts both the electrode and the in-pixel electronics. The sensing electrode, together with a surrounding area clear from electronic circuits, occupies a region of 20  $\mu\text{m} \times 20 \mu\text{m}$ , and it is centered in the pixel area. The remaining area is partitioned between the analog front end and the digital logic.

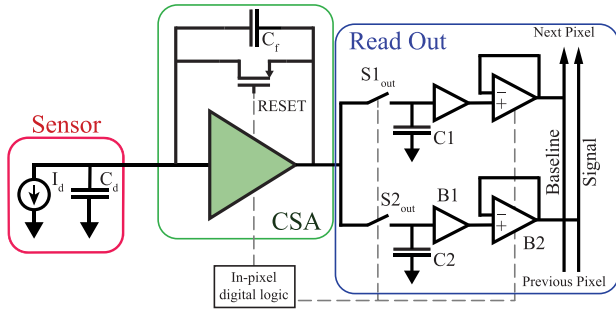


Fig. 6. Pixel readout block scheme.

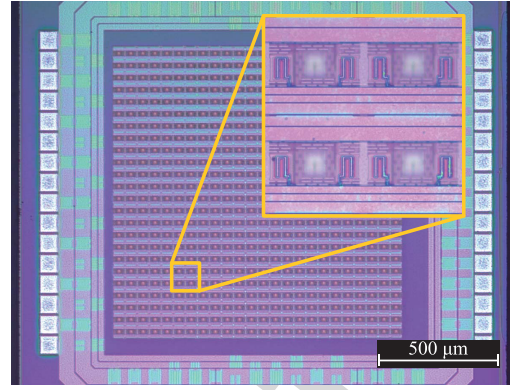


Fig. 7. Micrograph of active pixel array. Inset: close-up of 4 pixels.

201 The readout chain is shown in Fig. 6. The radiation-  
 202 generated current signal is amplified by a charge-sensitive  
 203 amplifier (CSA) circuit. A sample and hold circuitry, designed  
 204 to perform correlated double sampling (CDS) operation,  
 205 follows the CSA. Metal-insulator-metal (MIM) capacitors  
 206 are used to store the signal at this stage. Two analog buffers are  
 207 included to transmit the analog output signal along the column.

208 The charge-integrating amplifier, designed to maximize the  
 209 signal-to-noise ratio (SNR), is based on a telescopic cascode  
 210 architecture with a feedback capacitor  $C_f$  and a minimum-  
 211 size pMOS reset switch.  $C_f$  has been chosen equal to 5.8 fF,  
 212 giving a postlayout simulation gain of 130 mV/fC. The output  
 213 dynamic range of the amplifier is defined by considering the  
 214 expected signal for an MIP in a 300- $\mu\text{m}$ -thick detector. Thus,  
 215 for 3.8 fC (corresponding to 80 e-h pairs/ $\mu\text{m}$  in 300  $\mu\text{m}$   
 216 thickness), the output voltage signal matches the linear output  
 217 range of the amplifier, which is around 500 mV. This gain also  
 218 ensures a good SNR for MIPs in substrates with a thickness  
 219 as low as 50  $\mu\text{m}$ .

220 The pixel unit is also equipped with a digital logic to  
 221 manage data readout and to define the pixel functions. A 3-bit  
 222 in-pixel register allows to switch OFF defective pixels, enable  
 223 the injection of a test pulse for the electrical characterization  
 224 of the readout electronics, and enable the buffer amplifier for  
 225 data transmission. To study digital noise coupling between  
 226 the analog and digital sections of the design, each pixel  
 227 accommodates a digital buffer made by 18 elements, each with  
 228 a bandwidth of 5 GHz, designed to inject digital noise.

229 Fig. 7 shows a micrograph of the active pixel array, with  
 230 a group of 4 pixels in the magnified area. At the center of  
 231 the pixels, an area free from metal is present to allow the  
 232 illumination from the top. This feature was included to carry  
 233 out studies with laser sources.

234 The pixels were designed for a power consumption around  
 235 6  $\mu\text{W}$ . Providing a power supply of 1.2 V, the power consump-  
 236 tion of the pixel array in the static and dynamic conditions  
 237 is, respectively, 3.84 and 6.4 mW, without considering the  
 238 contribution of digital and EoC logic.

239 Small pixel arrays, formed by pixels free from electronic  
 240 readout circuits, were designed to allow additional flexibility  
 241 in the experimental evaluation of sensor and process charac-  
 242 teristics [12]. In these arrays, these are termed pseudomatrixes  
 243 (PMs) since all the sensing electrodes in the pixels are con-  
 244 nected to the same pad, and pixels with both 50- and 25- $\mu\text{m}$   
 245 pitch were included.

TABLE I  
 PRODUCED SENSOR SAMPLES

Sensor type	Thickness [ $\mu\text{m}$ ]	Pixel Pitch [ $\mu\text{m}^2$ ]
Full Sensor	300	50 $\times$ 50
PM	100	25 $\times$ 25, 50 $\times$ 50
PM	300	25 $\times$ 25, 50 $\times$ 50
PM Pixel pitch [ $\mu\text{m}$ ]	Pseudo-pixels	Metal width [ $\mu\text{m}$ ]
25 $\times$ 25	16 $\times$ 18	8
50 $\times$ 50	8 $\times$ 9	15

246 Two fabrication runs, including both pixel arrays and  
 247 PM test structures, were produced on high-resistivity wafers  
 248 ( $\rho > 2 \text{ k}\Omega \cdot \text{cm}$ ) that were thinned to 300 and 100  $\mu\text{m}$  prior  
 249 to backside processing. A summary of the devices presented  
 250 in this article is shown in Table I, highlighting their main  
 251 geometrical characteristics.

#### IV. EXPERIMENTAL RESULTS

252 An extensive experimental test campaign has been carried  
 253 out on both the test structures and the active pixel arrays in  
 254 order to assess their functionality. This section summarizes  
 255 the most meaningful results, discussed with reference to the  
 256 simulated characteristics presented in Section II.  
 257

##### A. Electrical Characterization

258 Static electrical characterizations have been performed at  
 259 room temperature on PM structures in order to evaluate  
 260 full depletion and punchthrough voltages for different pixel  
 261 sizes, thicknesses, and bias conditions. Current-voltage ( $I$ - $V$ )  
 262 curves have been measured using a four-channel semicon-  
 263 ductor parameter analyzer. In the measurements, the same  
 264 conditions used for the simulations described in Section II  
 265 have been applied; the p-wells were biased at 0 V, the sensing  
 266 nodes and the guard ring were biased between 0 and 1 V, and  
 267 a negative bias sweep was applied to the backside contact. The  
 268 measured sensor and backside currents are shown in Fig. 8 as  
 269 a function of the backside bias voltage for PMs with 25- $\mu\text{m}$   
 270 pitch. While the sensor current is plotted for three different  
 271 values of sensor voltage, only one curve is shown for the  
 272 backside current since no dependence on sensor voltage was  
 273 observed.  
 274

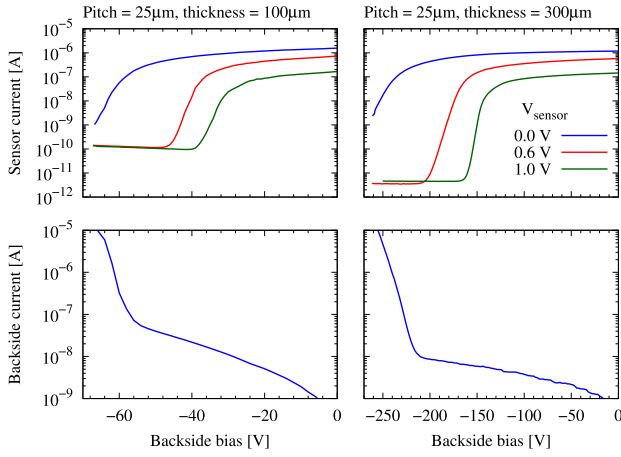


Fig. 8. Measured  $I$ - $V$  curves for 100  $\mu\text{m}$  (left) and 300  $\mu\text{m}$  (right) thick PM sensors. Pixel pitch is 25  $\mu\text{m}$ .

When compared with the simulated curves in Fig. 3, an excellent agreement was found in both the full depletion and the punchthrough voltage for both the device thicknesses and sensor bias voltages. The simulated and measured currents differ by several orders of magnitude due to the different sizes of the simulation domain (single pixel, 25  $\mu\text{m} \times 1 \mu\text{m}$  in 2-D simulations) and PM sensors (400  $\mu\text{m} \times 450 \mu\text{m}$  total active area). In the 300- $\mu\text{m}$ -thick sensors, the measured dark current is more than one order of magnitude smaller than in 100- $\mu\text{m}$ -thick sensors. Further investigations are going on to understand the origin of this difference, probably due to the different processing conditions. The  $I$ - $V$  curves measured on pixels with 50- $\mu\text{m}$  pitch are very similar to the ones shown in Fig. 8.

### B. Microbeam Sensor Characterization

The PMs have been tested at the RBI microbeam facility in Zagreb, Croatia [15]. The microbeam has been generated using a 1-MV Tandatron accelerator capable of delivering protons in the 0.5–2.0-MeV range; 2-MeV proton beams with  $\sigma_{\text{spot}} \approx 2 \mu\text{m}$  have been focused onto PM structures with different pixel sizes and thickness (see Table I). Protons of this energy have been simulated to have a Bragg peak located at a depth  $\lambda \approx 47 \mu\text{m}$  in silicon. As a result, the number of collected carriers and, in turn, the output signal is expected to be independent of the sensor thickness. The proton flux was adjusted to provide a maximum hit rate of 2 kHz.

The DUTs have been wire bonded to a specifically designed PCB equipped with p-i-n connectors to bias the collection electrodes, guard rings, and p-wells. The bias voltages were supplied by a HAMEG HMP2030 power supply, while the high-voltage power supply was an NHQ 202M. As shown in Fig. 9, an ORTEC 142-A bias-T preamplifier with a 20-mV/MeV gain has been connected between the pixel array and the biasing module. An ORTEC 570 voltage amplifier was connected between the preamplifier and a CANBERRA 8075 12-bit 10-V ADC.

Different bidimensional scans were performed by varying the sensor bias voltage to measure the uniformity in the charge

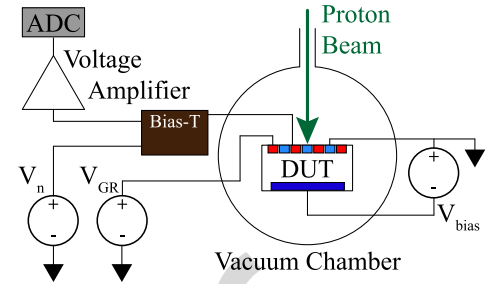


Fig. 9. Schematic of the PM bias and amplification circuits used at the proton microbeam.

collection efficiency (CCE) and characterize the transition at the boundary between the pixels and the guard ring.

The gain of the full readout chain was optimized to maximize the SNR of the output signal. The overall gain, depending on the gain of the different amplification stages, was tuned as follows:

$$G = G_1 \times G_2 = 20 \frac{\text{mV}}{\text{MeV}} \times 1.5 \times 100 \frac{\text{mV}}{\text{mV}} = 3 \frac{\text{V}}{\text{MeV}} \quad (1)$$

where  $G_1$  and  $G_2$  are, respectively, the gain of the preamplifier and the voltage amplifier.

Considering the beam energy,  $E = 2 \text{ MeV}$ , which is fully absorbed within 60  $\mu\text{m}$ , the following theoretical output voltage is expected:

$$V_{\text{th}} = G \times E \approx 6 \text{ V}. \quad (2)$$

In the measurements, the signal output was acquired as a function of the microbeam position. Maps with  $128 \times 128$  points were acquired in different areas of the sensor, both in the center of the pixel array and near the boundary between the pixels and the guard ring. In the former case, the map can be used to calculate uniformity of the CCE along the array, whereas in the latter case, some information on the spatial resolution of the sensor can be inferred.

The sensor output signal, expressed in ADC counts, is shown in Fig. 10 for two PM structures. To better appreciate the variation of the signal with beam position, the maps have been sliced along and across the sensing electrodes. The results are shown in Fig. 11.

The top plots show the CCE variation between the sensor electrodes and the metal lines. In the uniform regions between two metal lines, the mean value was 6.10 V, in good agreement with the expected one.

In the regions under the metal lines, having a width of 15 and 8  $\mu\text{m}$  for the PMs with 50- and 25- $\mu\text{m}$  pitch, respectively, and a thickness of 2.32  $\mu\text{m}$ , a 2% reduction in the collected charge can be estimated, while simulations predict a reduction of 3.5%. This slight discrepancy is due to the limited width of the metal lines, which does not allow observing a region with uniform response due to the finite spot size.

The bottom plots in Fig. 11, showing the signal along the vertical slices, offer information on charge sharing between the pixels and the guard ring. In the 100- $\mu\text{m}$  sensor, the signal rises from 10% to 90% in 22  $\mu\text{m}$  independently of the reverse bias. In the 300- $\mu\text{m}$  sensor, on the other hand, the width of the

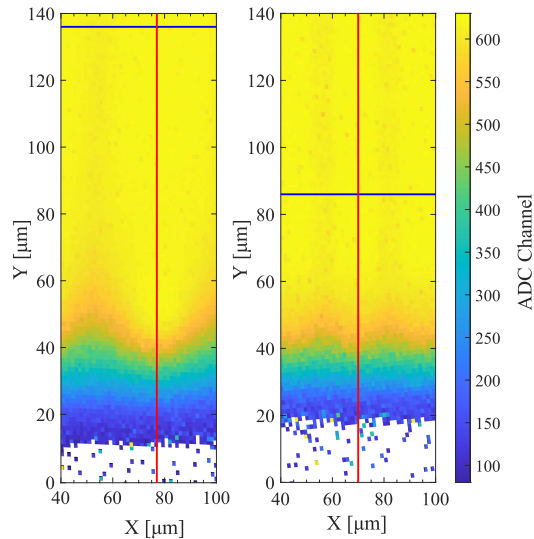


Fig. 10. Microbeam scan of 100  $\mu\text{m}$  sensor with 50- $\mu\text{m}$  pixel pitch (left) and 300- $\mu\text{m}$  sensor with a 25- $\mu\text{m}$  pixel pitch (right). The microbeam scan step is equal to  $\Delta X \approx 1.35 \mu\text{m}$ . The horizontal cut (blue line) is done across the second electrode from the matrix edge, whereas the vertical cut (red line) is performed halfway between the metal lines, i.e., along the collecting electrodes.

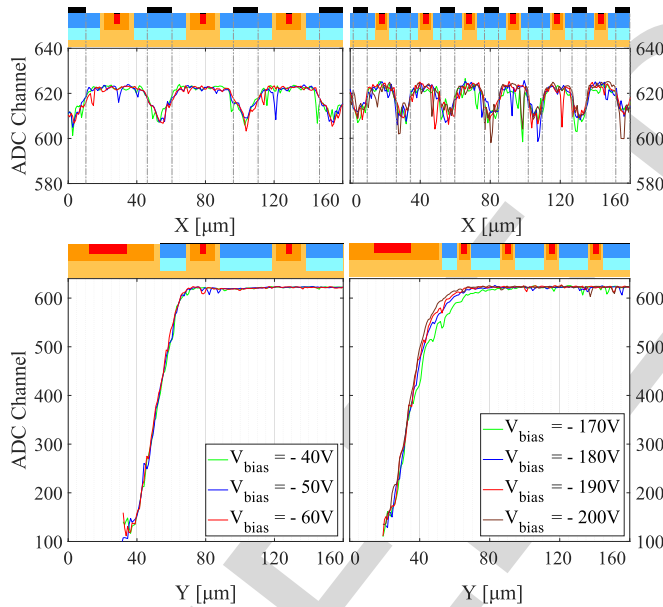


Fig. 11. Signal amplitude profiles at different bias voltages on the 100- $\mu\text{m}$  (left) and 300- $\mu\text{m}$  (right) thick sensors. The profiles are shown along (top) and across (bottom) the sensing electrodes in the same location as in Fig. 10.

355 transition region decreases from 34 to 26  $\mu\text{m}$  as the reverse  
356 bias increases. These results are in good agreement with the  
357 simulations in Fig. 5.

### 358 C. Active Pixel Sensor Characterization With $^{55}\text{Fe}$ 359 Source

360 A test campaign on the active pixel array with a  $^{55}\text{Fe}$   
361 calibration source was carried out in order to characterize both  
362 the sensor and its front-end electronics.

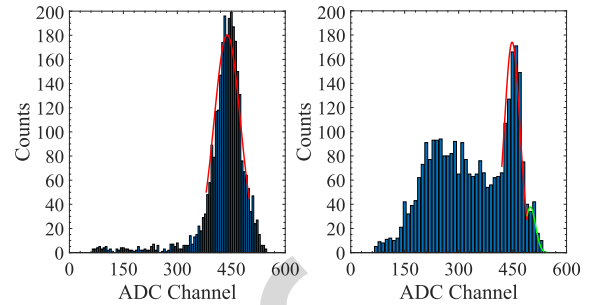


Fig. 12. Reconstructed spectrum of  $^{55}\text{Fe}$  source for all clusters (left) and for seed signals (right) at  $V_{\text{bias}} = -200 \text{ V}$ . The fits are superimposed to the distributions.

The reconstructed spectrum of the absorbed photoelectrons  
was first used to calibrate the pixel response sector by sector.  
In the following discussion, all data refer to one of the  
four sectors at  $V_{\text{bias}} = -200 \text{ V}$  and for an integration time  
of 12.8  $\mu\text{s}$ . This value has been chosen to collect enough  
statistics in a reasonable amount of time, without increas-  
ing the noise contribution, due to the leakage current, too  
much. Cluster signals were reconstructed by applying a double  
threshold method on a matrix of  $5 \times 5$  pixels selected around a  
candidate cluster seed. Clusters were requested to have a seed  
pixel with an SNR, S/N, of at least 6.0 and the neighboring  
pixels an S/N in excess of 4.0.

In Fig. 12, we show the spectrum of the cluster signals  
(left) and the one of the seed pixels only (right). The energy  
peak of the distribution, including all clusters (mean value  
 $\approx 439 \text{ ADC}$ ), was used to calibrate the pixel response.  
The analog gain of the full readout chain was found to be  
 $\approx 124 \text{ mV/fC}$ , in good agreement with simulations  
( $\approx 130 \text{ mV/fC}$ ). The energy resolution [full-width at half-  
maximum (FWHM)] depends on the cluster multiplicity; it is  
 $\approx 1.1 \text{ keV}$  when all clusters are included (regardless of their  
size) and is reduced to  $\approx 0.7 \text{ keV}$  for single-pixel clusters.  
On the seed value distribution, the peak corresponding to  
the full charge collection of the 5.9-keV photoelectrons can  
be recognized at  $\approx 449 \text{ ADC}$ . The charge deficit of  $\approx 1\%$   
with respect to the distribution, including all clusters, puts  
a lower limit to the CCE of the detector. It is interesting  
to note that also the peak of the 6.5-keV photons, centered  
at  $\approx 500 \text{ ADC}$ , can be distinguished. We used the gain  
information to evaluate the noise performance of the prototype  
(sensor and electronics). For each pixel, its noise was measured  
as the rms of the pedestal distribution in dark conditions. The  
noise distribution for the full matrix is  $\approx 12 \text{ ADC}$  (two ADCs  
coming from the readout chain: DAQ and readout boards)  
which, expressed in electrons after the calibration, is shown  
in Fig. 13. The mean noise value is found to be  $\approx 40 \text{ e}^-$  at  
room temperature.

In order to study the charge sharing between the pixels in  
the two configurations, the cluster size and shape were also  
analyzed, applying both front- and back-side irradiation. The  
results are shown in Fig. 14, on the left for front illumination  
and on the right for back illumination. It can be observed,  
in both cases, how the cluster size is limited to 4 pixels  
since clusters with a multiplicity larger than 5 are only a  
small fraction of the total ( $<1\%$ ). This proves how charge

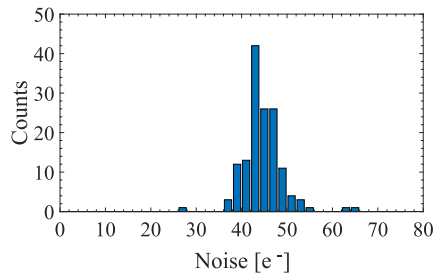


Fig. 13. Noise distribution at room temperature with  $V_{\text{bias}} = -200$  V and an integration time of 12.8  $\mu$ s.

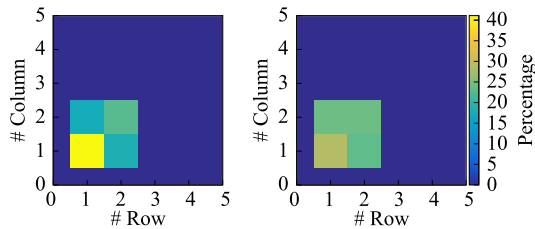


Fig. 14. Cluster size at  $V_{\text{bias}} = -200$  V in front illumination (left) and in back illumination (right).

sharing is small, and the cluster size is mainly affected by the photon conversion position. In addition, the observation that the cluster size in back illumination is comparable with the one in front illumination confirms that, at the selected voltage, the sensor is FD and charge collection is dominated by the drift mechanism.

## V. CONCLUSION

In this article, we have demonstrated the feasibility of FD-MAPS in a 110-nm CMOS process. The first experimental results confirm the expected sensor characteristics for a pixel thickness up to 300  $\mu$ m and a pixel pitch down to 25  $\mu$ m. A large-area active pixel detector is currently under development and will be used to validate the technology in the context of a charged-particle tracking experiment. The interest of the developed process, however, is not limited to charged-particle detection applications. The detection of photons with high penetration depth, i.e., X-ray imaging as well as time-resolved near-infrared imaging, are potentially interesting application scenarios where the proposed technology can be competitive with other state-of-the-art approaches.

## ACKNOWLEDGMENT

The research activity presented in this article has been carried out in the framework of the SEED and ARCADIA

experiments. The authors acknowledge the support from our colleagues at RBI, Zagreb, Croatia, in operating the tandemron experimental setup.

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# Fully Depleted MAPS in 110-nm CMOS Process With 100–300- $\mu\text{m}$ Active Substrate

Lucio Pancheri<sup>1</sup>, Member, IEEE, Raffaele A. Giampaolo, Andrea Di Salvo, Serena Mattiazzo<sup>2</sup>,  
Thomas Corradino, Piero Giubilato, Romualdo Santoro<sup>3</sup>, Massimo Caccia<sup>4</sup>, Giovanni Margutti,  
Jonhatan E. Olave, Manuel Rolo, and Angelo Rivetti

**Abstract**—This article presents a fully depleted monolithic active pixel sensor technology compatible with a standard deep submicrometer 110-nm CMOS process. Passive test pixels structures, produced in various flavors, have proved the feasibility of 100- and 300- $\mu\text{m}$ -thick active substrates. Active pixel sensors with monolithically integrated analog and digital electronics, consisting of a  $24 \times 24$  array of pixels with 50- $\mu\text{m}$  pitch, have been shown to be fully functional when operating in the full depletion mode. Characterization results obtained with a proton microbeam and a  $^{55}\text{Fe}$  radiation source are presented and discussed.

**Index Terms**—CMOS, monolithic active pixel sensor (MAPS), radiation detector, silicon.

## I. INTRODUCTION

MONOLITHIC active pixel sensors (MAPSs) are emerging as a viable alternative to hybrid pixels in charged-particles' detection and high-energy photons imaging, showing advantages in both performance and overall costs per unit area [1]–[3].

The reconstruction with the highest precision of the perigee parameters of charged-particle trajectories in a dense

environment calls for pixel pitches of tens of micrometers, low material budget, a high signal-over-noise ratio, and limited diffusion of the charge carriers originated by the impinging particle. These specifications can be obtained with a monolithic design implemented on a fully depleted (FD) high-resistivity substrate. As a consequence, FD-MAPSs are raising a significant interest in the high-energy physics community [4], [5].

FD-MAPSs have also been proposed for X-ray imaging [6], where an active substrate of 300–500  $\mu\text{m}$  would enable an efficient detection of photon energies up to 15 keV. Other applications, such as medical particle tomography and tracking in space experiments, would benefit from the low material budget, fine pixel pitch, and low power consumption offered by MAPS sensors [7], [8].

As a general trend in the development of pixel sensors, the complexity of on-chip digital functions is increasing, making it easier to integrate and deploy a complete sensor system. Moreover, event-driven readout schemes are frequently adopted to reduce power consumption and, in turn, relax the requirements of the cooling systems, impacting on the overall system material budget. To these purposes, very scaled process nodes should be used to reduce the area and to increase the speed of on-chip digital electronics.

The latest FD-MAPS design efforts in the high-energy physics community are adopting 180- and 150-nm process nodes. Most of the developments, in this respect, have been devoted to the implementation of devices with a depletion region ranging from a few tens of micrometer and hundreds of micrometer [4], [5]. In [4], large depletion regions are obtained by including the electronics inside a deep n-well that is used as a collection node for the electrons generated by the incident charged particles. This approach has demonstrated an excellent radiation hardness and a fast charge collection, but the sensor capacitance is relatively large, and a nonnegligible part of the pixel area cannot be used to accommodate the readout circuits. Scaling to very small pixels is thus very challenging while using such topology.

An alternative approach, arising from an evolution of the pixels designed for the ALICE detector [1], uses small sensing nodes while implanting a low-doped n-type region below the electronics [5]. In this way, most of the generated charges can be collected by drift, while the area and the capacitance of the sensors are maintained small, granting scalability toward

Manuscript received February 7, 2020; revised March 30, 2020; accepted March 30, 2020. This work was supported in part by the Istituto Nazionale di Fisica Nucleare (INFN), CSN5, and in part by the H2020 Project AIDA-2020 under Grant 654168. The review of this article was arranged by Editor J. Huang. (Corresponding author: Lucio Pancheri.)

Lucio Pancheri and Thomas Corradino are with the Dipartimento di Ingegneria Industriale, TIFPA Istituto Nazionale di Fisica Nucleare (INFN), Università di Trento, 38123 Trento, Italy (e-mail: lucio.pancheri@unitn.it).

Raffaele A. Giampaolo and Andrea Di Salvo are with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy, and also with the Istituto Nazionale di Fisica Nucleare (INFN)—Torino, 10125 Turin, Italy (e-mail: raffaeleaaron.giampaolo@to.infn.it; andrea\_disalvo@polito.it).

Serena Mattiazzo and Piero Giubilato are with the Dipartimento di Fisica e Astronomia, Istituto Nazionale di Fisica Nucleare—Sezione di Padova, Università di Padova, 35131 Padua, Italy (e-mail: serena.mattiazzo@unipd.it; piero.giubilato@unipd.it).

Romualdo Santoro and Massimo Caccia are with the Dipartimento di Scienze ed Alta Tecnologia, Università dell'Insubria, 22100 Varese, Italy, and also with the Istituto Nazionale di Fisica Nucleare—Sezione Milano.

Giovanni Margutti is with LFoundry S.r.l., 67051 Avezzano, Italy.  
Jonhatan E. Olave, Manuel Rolo, and Angelo Rivetti are with the Istituto Nazionale di Fisica Nucleare—Torino, 10125 Turin, Italy.

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Digital Object Identifier 10.1109/TED.2020.2985639

65 small pixel sizes. This approach, although excellent for particle  
66 tracking, cannot be easily extended to an active thickness in  
67 excess of  $100\ \mu\text{m}$  since the space-charge region extends from  
68 the top surface of the sensor, thus limiting the applicable  
69 voltage at the sensor top side.

70 The possibility of FD thick substrates in CMOS-integrated  
71 sensors has been first explored in [9], demonstrating an FD  
72 sensor with p-type substrate and a n-type backside implanta-  
73 tion. In the first prototype, the electronics were made entirely  
74 of p-type transistors. A similar approach was adopted in [10],  
75 using a CMOS process with n-type substrates and implanting  
76 a p+ region on the back.

77 Full depletion can also be obtained using a silicon-on-  
78 insulator process. Although the radiation damage of the insula-  
79 tor oxide poses several challenges related to parameter drift  
80 in the transistor characteristics, the latest advancements have  
81 greatly improved the radiation hardness of the process, and  
82 sensors with depletion regions up to  $500\ \mu\text{m}$  thick have been  
83 demonstrated [11].

84 In this article, we present a technology platform for the  
85 implementation of FD MAPS based on a modified 110-nm  
86 CMOS process. The process node was chosen to enable the  
87 in-pixel implementation of complex digital functions while  
88 keeping low prototyping and production costs. Backside  
89 processing was used to create a junction on the bottom  
90 surface that is biased to deplete the whole sensor substrate.

91 This article is structured as follows. Section II discusses  
92 the simulated characteristics with reference to geometry and  
93 process parameters. In Section III, the design of pixel test  
94 structures and a small array of active pixels with integrated  
95 electronics are presented. Section IV presents the results of  
96 the characterization of the arrays compared with the expecta-  
97 tions according to the simulation. The perspectives for this  
98 technology are highlighted in Section V.

## 99 II. SENSOR CONCEPT

100 The process was developed starting from a 110-nm indus-  
101 trial CMOS with 1.2-V transistors and six metal layers. A few  
102 add-ons were necessary to allow for full substrate depletion  
103 with electron collection at the sensing electrodes. A concept  
104 cross section of the pixel array is shown in Fig. 1 [12].

105 The standard p-type substrate was replaced with an n-type  
106 floating zone material. Wafer thinning and backside lithog-  
107 raphy were necessary to introduce a junction at the bottom  
108 surface, used to bias the substrate to full depletion while  
109 maintaining a low voltage at the front side. A shallow boron-  
110 doped region was implanted on the rear side of the wafer, and  
111 the dopants were activated by laser annealing. Since, at large  
112 wafer thicknesses, the voltage needed for sensor full depletion  
113 exceeds  $150\ \text{V}$ , a termination structure composed of multiple  
114 guard rings was introduced.

115 A deep p-well scheme was used to prevent the n-wells  
116 hosting p-MOSFETs from collecting the charge generated  
117 by radiation in the substrate. Care had to be taken to limit  
118 the punchthrough current between the back-side junction and  
119 the deep p-well at sensor full depletion. A good control of  
120 punchthrough could be obtained either by increasing the bias

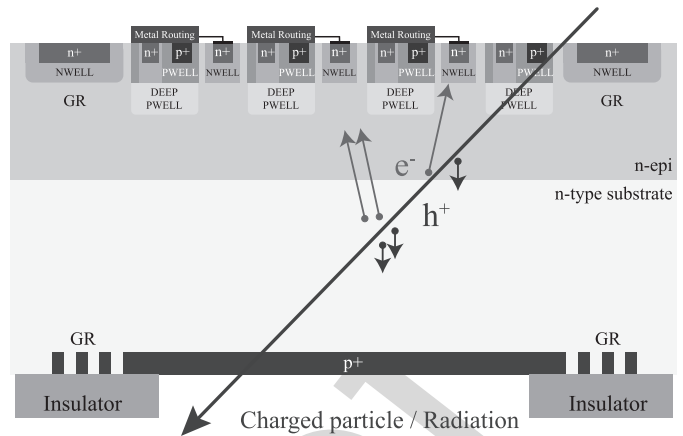


Fig. 1. FD pixel sensor cross section.

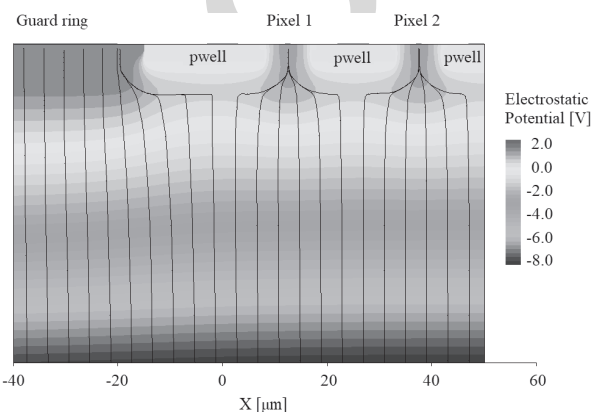


Fig. 2. Simulated 2-D potential profile and electric-field lines at full depletion. The simulation domain includes part of the guard rings and 2 pixels with  $25\text{-}\mu\text{m}$  pitch. Only the sensor surface region is shown.

121 voltage at the pixel sensor nodes or by increasing the n-dopant  
122 concentration below the p-wells. Since the sensors had to be  
123 directly coupled to the low-voltage electronics, the second  
124 solution was adopted, by adding an n-doped epitaxial layer,  
125 having a resistivity lower than the substrate, to the process  
126 flow.

127 TCAD simulations were used to tune the process paramet-  
128 ers. The simulated potential profile at full depletion for a  
129 domain, including 2 pixels and part of the surface guard ring,  
130 is shown in Fig. 2. Electric-field lines are orthogonal to the  
131 sensor surface up to the bottom of the deep p-wells, and then,  
132 they deviate horizontally toward the collection electrodes.

133 The full depletion and punchthrough voltages were simu-  
134 lated on this domain by introducing a small unbalance ( $10\ \text{mV}$ )  
135 between pixel and guard ring bias voltages. The current  
136 flowing at the sensing electrodes and at the backside as a  
137 function of applied backside bias is shown in Fig. 3. At low  
138 reverse voltage, the substrate is not FD, and resistive paths  
139 exist between the pixels and the guard ring, leading to a macro-  
140 scopic current. As the bias voltage is increased, a sharp current  
141 drop is observed, indicating the onset of full depletion. The  
142 depletion voltage is reduced by increasing the voltage applied  
143 at the front side to the sensor nodes. If the backside voltage  
144 is further increased, a punchthrough current starts flowing and

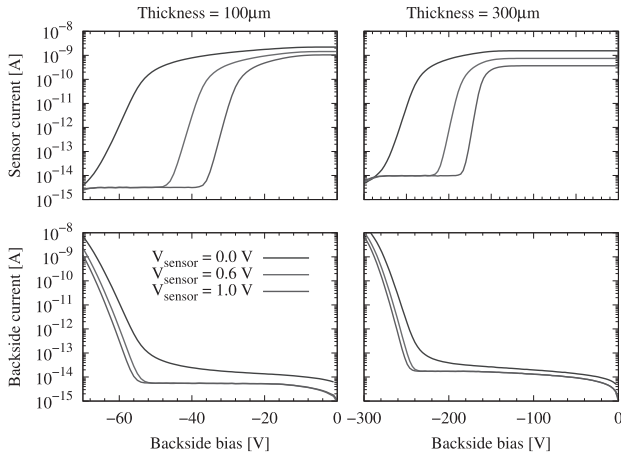


Fig. 3. Simulated sensor and backside current as a function of backside voltage for two values of sensor thickness [100  $\mu\text{m}$ , (left) and 300  $\mu\text{m}$  (right)]. Pixel pitch is 25  $\mu\text{m}$ .

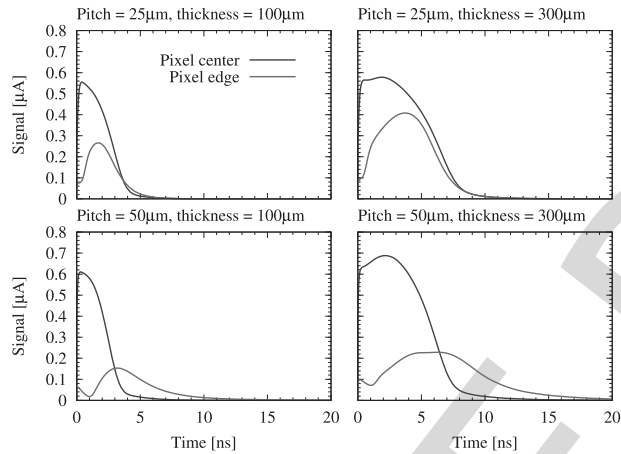


Fig. 4. Simulated transient current signal with an incident MIP for two different values of sensor thickness [100  $\mu\text{m}$  (left) and 300  $\mu\text{m}$  (right)] and pixel pitch [25  $\mu\text{m}$  (top) and 50  $\mu\text{m}$  (bottom)].

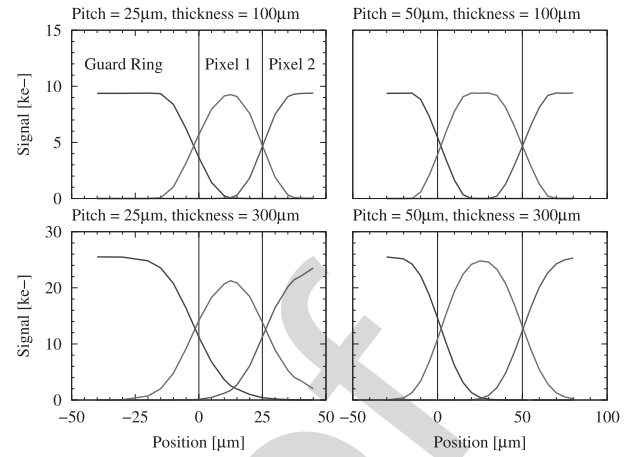


Fig. 5. Simulated collected charge at the sensor periphery as a function of the position of the incident particle for two different values of sensor thickness [100  $\mu\text{m}$  (top) and 300  $\mu\text{m}$  (bottom)] and pixel pitch [25  $\mu\text{m}$  (left) and 50  $\mu\text{m}$  (right)].

respectively, for 100 and 300  $\mu\text{m}$  thickness when the MIP is incident in the center of the pixel. If the MIP is incident at the pixel periphery, the collection speed depends on the pixel pitch; at 50- $\mu\text{m}$  pitch, the collection time approximately doubles since the charge generated in the substrate first reaches the bottom of the deep p-well and then drifts horizontally toward the collection node. Even considering this worst case situation, however, the charge is completely collected within 20 ns. In 25- $\mu\text{m}$  pixels, on the contrary, the collection time is only slightly degraded, as a result of the smaller horizontal distance traveled by electrons generated at the pixel periphery.

The integrated charge as a function of the MIP incidence position is shown in Fig. 5. Charge sharing between the pixels for two values of thickness and pixel pitch can be observed. As expected, sharing slightly increases by increasing the pixel pitch and sensor thickness, but, in all the cases considered here, the effect is confined to the nearest neighboring pixels.

eventually reaches very large values. The voltage difference between breakdown and punchthrough voltages depends on the sensor bias. At a sensor voltage between 0.6 and 1 V that can be applied if the sensor is directly coupled to the electronic readout channels, the difference between full depletion and punchthrough is a fraction of 10%–20% of the applied bias voltage. This value is large enough to reliably accommodate the operation of a pixel array, considered possible doping gradients and nonuniformities between the pixels.

Charge collection dynamics upon the incidence of a minimum ionizing particle (MIP) were also simulated. The MIP was modeled as a continuous charge density of 80 e-h pairs/ $\mu\text{m}$ , orthogonal to the sensor surface and extending throughout the sensor thickness. With reference to the simulation domain shown in Fig. 2, several positions of incidence were considered for the MIP. The current signal generated at the sensor is shown in Fig. 4 for two different MIP incidence positions, two values of pixel pitch (25 and 50  $\mu\text{m}$ ), and two values of sensor thickness (100 and 300  $\mu\text{m}$ ). As expected, complete charge collection is observed in less than 5 and 10 ns,

### III. ACTIVE PIXEL ARRAY AND TEST STRUCTURES

A 576-active pixel array was designed as a test bench to validate the performance of the proposed technology [13], [14]. The pixels are organized in four sectors, each one consisting of 6 columns of 24 pixels. An end-of-column (EoC) block manages the column logic, handling pixel configuration and controlling data transmission. In this way, each sector works in parallel with the others. To read out the data for a single sector, two clocks are used. The first controls the shift register in the EoC to select the column, whereas the second one is dedicated to the row shift register. In a typical case, they, respectively, work at 5 and 0.2 MHz. Thus, the whole array can be read in less than 30  $\mu\text{s}$  using a 5-MHz clock.

A single 50- $\mu\text{m}$  pitch pixel hosts both the electrode and the in-pixel electronics. The sensing electrode, together with a surrounding area clear from electronic circuits, occupies a region of 20  $\mu\text{m} \times 20 \mu\text{m}$ , and it is centered in the pixel area. The remaining area is partitioned between the analog front end and the digital logic.

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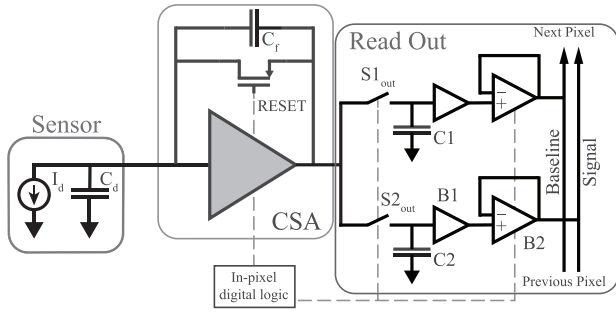


Fig. 6. Pixel readout block scheme.

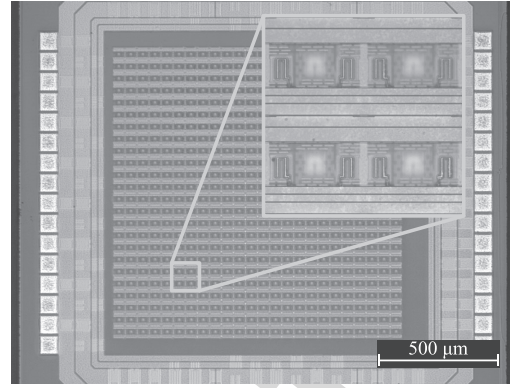


Fig. 7. Micrograph of active pixel array. Inset: close-up of 4 pixels.

201 The readout chain is shown in Fig. 6. The radiation-  
 202 generated current signal is amplified by a charge-sensitive  
 203 amplifier (CSA) circuit. A sample and hold circuitry, designed  
 204 to perform correlated double sampling (CDS) operation,  
 205 follows the CSA. Metal-insulator-metal (MIM) capacitors  
 206 are used to store the signal at this stage. Two analog buffers are  
 207 included to transmit the analog output signal along the column.

208 The charge-integrating amplifier, designed to maximize the  
 209 signal-to-noise ratio (SNR), is based on a telescopic cascode  
 210 architecture with a feedback capacitor  $C_f$  and a minimum-  
 211 size pMOS reset switch.  $C_f$  has been chosen equal to 5.8 fF,  
 212 giving a postlayout simulation gain of 130 mV/fC. The output  
 213 dynamic range of the amplifier is defined by considering the  
 214 expected signal for an MIP in a 300- $\mu\text{m}$ -thick detector. Thus,  
 215 for 3.8 fC (corresponding to 80 e-h pairs/ $\mu\text{m}$  in 300  $\mu\text{m}$   
 216 thickness), the output voltage signal matches the linear output  
 217 range of the amplifier, which is around 500 mV. This gain also  
 218 ensures a good SNR for MIPs in substrates with a thickness  
 219 as low as 50  $\mu\text{m}$ .

220 The pixel unit is also equipped with a digital logic to  
 221 manage data readout and to define the pixel functions. A 3-bit  
 222 in-pixel register allows to switch OFF defective pixels, enable  
 223 the injection of a test pulse for the electrical characterization  
 224 of the readout electronics, and enable the buffer amplifier for  
 225 data transmission. To study digital noise coupling between  
 226 the analog and digital sections of the design, each pixel  
 227 accommodates a digital buffer made by 18 elements, each with  
 228 a bandwidth of 5 GHz, designed to inject digital noise.

229 Fig. 7 shows a micrograph of the active pixel array, with  
 230 a group of 4 pixels in the magnified area. At the center of  
 231 the pixels, an area free from metal is present to allow the  
 232 illumination from the top. This feature was included to carry  
 233 out studies with laser sources.

234 The pixels were designed for a power consumption around  
 235 6  $\mu\text{W}$ . Providing a power supply of 1.2 V, the power consump-  
 236 tion of the pixel array in the static and dynamic conditions  
 237 is, respectively, 3.84 and 6.4 mW, without considering the  
 238 contribution of digital and EoC logic.

239 Small pixel arrays, formed by pixels free from electronic  
 240 readout circuits, were designed to allow additional flexibility  
 241 in the experimental evaluation of sensor and process charac-  
 242 teristics [12]. In these arrays, these are termed pseudomatrices  
 243 (PMs) since all the sensing electrodes in the pixels are con-  
 244 nected to the same pad, and pixels with both 50- and 25- $\mu\text{m}$   
 245 pitch were included.

TABLE I  
 PRODUCED SENSOR SAMPLES

Sensor type	Thickness [ $\mu\text{m}$ ]	Pixel Pitch [ $\mu\text{m}^2$ ]
Full Sensor	300	50 $\times$ 50
PM	100	25 $\times$ 25, 50 $\times$ 50
PM	300	25 $\times$ 25, 50 $\times$ 50
PM Pixel pitch [ $\mu\text{m}$ ]	Pseudo-pixels	Metal width [ $\mu\text{m}$ ]
25 $\times$ 25	16 $\times$ 18	8
50 $\times$ 50	8 $\times$ 9	15

Two fabrication runs, including both pixel arrays and PM test structures, were produced on high-resistivity wafers ( $\rho > 2 \text{ k}\Omega \cdot \text{cm}$ ) that were thinned to 300 and 100  $\mu\text{m}$  prior to backside processing. A summary of the devices presented in this article is shown in Table I, highlighting their main geometrical characteristics.

#### IV. EXPERIMENTAL RESULTS

An extensive experimental test campaign has been carried out on both the test structures and the active pixel arrays in order to assess their functionality. This section summarizes the most meaningful results, discussed with reference to the simulated characteristics presented in Section II.

##### A. Electrical Characterization

Static electrical characterizations have been performed at room temperature on PM structures in order to evaluate full depletion and punchthrough voltages for different pixel sizes, thicknesses, and bias conditions. Current-voltage ( $I$ - $V$ ) curves have been measured using a four-channel semiconductor parameter analyzer. In the measurements, the same conditions used for the simulations described in Section II have been applied; the p-wells were biased at 0 V, the sensing nodes and the guard ring were biased between 0 and 1 V, and a negative bias sweep was applied to the backside contact. The measured sensor and backside currents are shown in Fig. 8 as a function of the backside bias voltage for PMs with 25- $\mu\text{m}$  pitch. While the sensor current is plotted for three different values of sensor voltage, only one curve is shown for the backside current since no dependence on sensor voltage was observed.

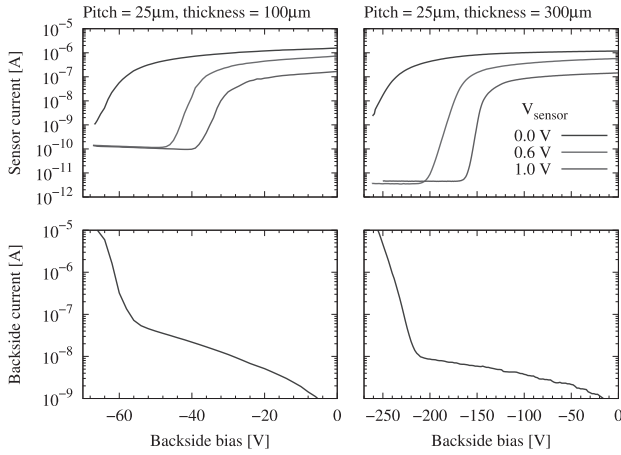


Fig. 8. Measured  $I$ - $V$  curves for 100  $\mu\text{m}$  (left) and 300  $\mu\text{m}$  (right) thick PM sensors. Pixel pitch is 25  $\mu\text{m}$ .

275 When compared with the simulated curves in Fig. 3,  
 276 an excellent agreement was found in both the full depletion  
 277 and the punchthrough voltage for both the device thicknesses  
 278 and sensor bias voltages. The simulated and measured currents  
 279 differ by several orders of magnitude due to the different  
 280 sizes of the simulation domain (single pixel, 25  $\mu\text{m} \times 1 \mu\text{m}$   
 281 in 2-D simulations) and PM sensors (400  $\mu\text{m} \times 450 \mu\text{m}$  total  
 282 active area). In the 300- $\mu\text{m}$ -thick sensors, the measured dark  
 283 current is more than one order of magnitude smaller than in  
 284 100- $\mu\text{m}$ -thick sensors. Further investigations are going on to  
 285 understand the origin of this difference, probably due to the  
 286 different processing conditions. The  $I$ - $V$  curves measured on  
 287 pixels with 50- $\mu\text{m}$  pitch are very similar to the ones shown  
 288 in Fig. 8.

### 289 B. Microbeam Sensor Characterization

290 The PMs have been tested at the RBI microbeam facility  
 291 in Zagreb, Croatia [15]. The microbeam has been generated  
 292 using a 1-MV Tandatron accelerator capable of delivering  
 293 protons in the 0.5–2.0-MeV range; 2-MeV proton beams with  
 294  $\sigma_{\text{spot}} \approx 2 \mu\text{m}$  have been focused onto PM structures with  
 295 different pixel sizes and thickness (see Table I). Protons of  
 296 this energy have been simulated to have a Bragg peak located  
 297 at a depth  $\lambda \approx 47 \mu\text{m}$  in silicon. As a result, the number of  
 298 collected carriers and, in turn, the output signal is expected to  
 299 be independent of the sensor thickness. The proton flux was  
 300 adjusted to provide a maximum hit rate of 2 kHz.

301 The DUTs have been wire bonded to a specifically designed  
 302 PCB equipped with p-i-n connectors to bias the collection  
 303 electrodes, guard rings, and p-wells. The bias voltages were  
 304 supplied by a HAMEG HMP2030 power supply, while the  
 305 high-voltage power supply was an NHQ 202M. As shown  
 306 in Fig. 9, an ORTEC 142-A bias-T preamplifier with a  
 307 20-mV/MeV gain has been connected between the pixel  
 308 array and the biasing module. An ORTEC 570 voltage  
 309 amplifier was connected between the preamplifier and a  
 310 CANBERRA 8075 12-bit 10-V ADC.

311 Different bidimensional scans were performed by varying  
 312 the sensor bias voltage to measure the uniformity in the charge

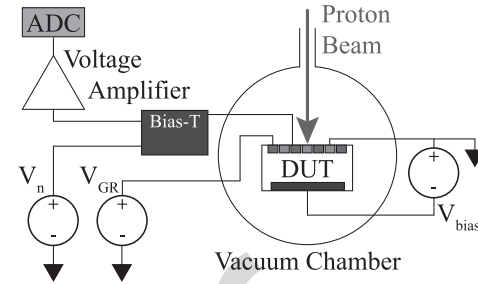


Fig. 9. Schematic of the PM bias and amplification circuits used at the proton microbeam.

313 collection efficiency (CCE) and characterize the transition at  
 314 the boundary between the pixels and the guard ring.

315 The gain of the full readout chain was optimized to maxi-  
 316 mize the SNR of the output signal. The overall gain, depending  
 317 on the gain of the different amplification stages, was tuned as  
 318 follows:

$$319 \quad G = G_1 \times G_2 = 20 \frac{\text{mV}}{\text{MeV}} \times 1.5 \times 100 \frac{\text{mV}}{\text{mV}} = 3 \frac{\text{V}}{\text{MeV}} \quad (1)$$

320 where  $G_1$  and  $G_2$  are, respectively, the gain of the preamplifier  
 321 and the voltage amplifier.

322 Considering the beam energy,  $E = 2 \text{ MeV}$ , which is  
 323 fully absorbed within 60  $\mu\text{m}$ , the following theoretical output  
 324 voltage is expected:

$$325 \quad V_{\text{th}} = G \times E \approx 6 \text{ V}. \quad (2)$$

326 In the measurements, the signal output was acquired as  
 327 a function of the microbeam position. Maps with  $128 \times$   
 328 128 points were acquired in different areas of the sensor, both  
 329 in the center of the pixel array and near the boundary  
 330 between the pixels and the guard ring. In the former case, the map can  
 331 be used to calculate uniformity of the CCE along the array,  
 332 whereas in the latter case, some information on the spatial  
 333 resolution of the sensor can be inferred.

334 The sensor output signal, expressed in ADC counts,  
 335 is shown in Fig. 10 for two PM structures. To better appreciate  
 336 the variation of the signal with beam position, the maps have  
 337 been sliced along and across the sensing electrodes. The results  
 338 are shown in Fig. 11.

339 The top plots show the CCE variation between the sensor  
 340 electrodes and the metal lines. In the uniform regions between  
 341 two metal lines, the mean value was 6.10 V, in good agreement  
 342 with the expected one.

343 In the regions under the metal lines, having a width  
 344 of 15 and 8  $\mu\text{m}$  for the PMs with 50- and 25- $\mu\text{m}$  pitch,  
 345 respectively, and a thickness of 2.32  $\mu\text{m}$ , a 2% reduction in the  
 346 collected charge can be estimated, while simulations predict a  
 347 reduction of 3.5%. This slight discrepancy is due to the limited  
 348 width of the metal lines, which does not allow observing a  
 349 region with uniform response due to the finite spot size.

350 The bottom plots in Fig. 11, showing the signal along the  
 351 vertical slices, offer information on charge sharing between  
 352 the pixels and the guard ring. In the 100- $\mu\text{m}$  sensor, the signal  
 353 rises from 10% to 90% in 22  $\mu\text{m}$  independently of the reverse  
 354 bias. In the 300- $\mu\text{m}$  sensor, on the other hand, the width of the

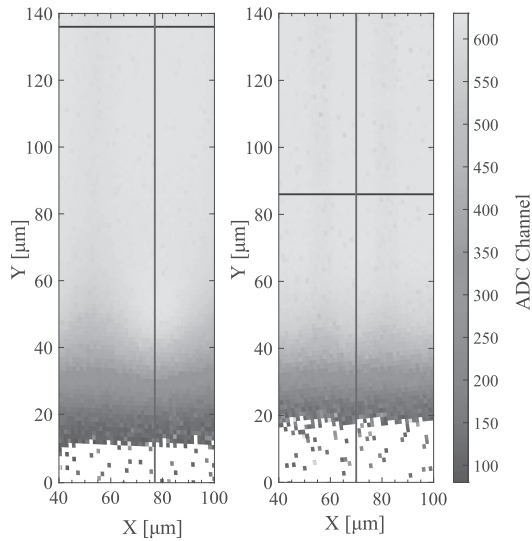


Fig. 10. Microbeam scan of 100  $\mu\text{m}$  sensor with 50- $\mu\text{m}$  pixel pitch (left) and 300- $\mu\text{m}$  sensor with a 25- $\mu\text{m}$  pixel pitch (right). The microbeam scan step is equal to  $\Delta X \approx 1.35 \mu\text{m}$ . The horizontal cut (blue line) is done across the second electrode from the matrix edge, whereas the vertical cut (red line) is performed halfway between the metal lines, i.e., along the collecting electrodes.

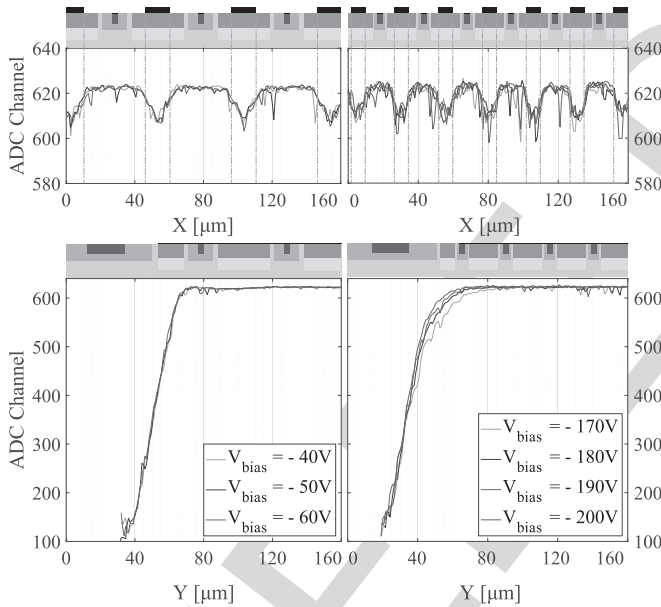


Fig. 11. Signal amplitude profiles at different bias voltages on the 100- $\mu\text{m}$  (left) and 300- $\mu\text{m}$  (right) thick sensors. The profiles are shown along (top) and across (bottom) the sensing electrodes in the same location as in Fig. 10.

355 transition region decreases from 34 to 26  $\mu\text{m}$  as the reverse  
356 bias increases. These results are in good agreement with the  
357 simulations in Fig. 5.

### 358 C. Active Pixel Sensor Characterization With $^{55}\text{Fe}$ 359 Source

360 A test campaign on the active pixel array with a  $^{55}\text{Fe}$   
361 calibration source was carried out in order to characterize both  
362 the sensor and its front-end electronics.

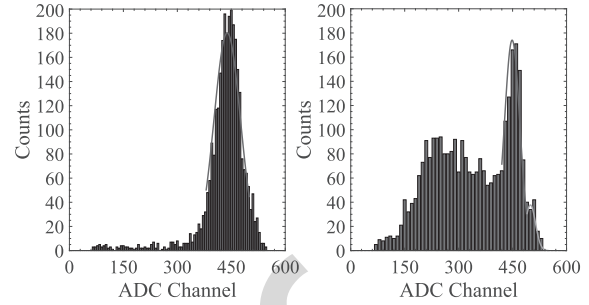


Fig. 12. Reconstructed spectrum of  $^{55}\text{Fe}$  source for all clusters (left) and for seed signals (right) at  $V_{\text{bias}} = -200 \text{ V}$ . The fits are superimposed to the distributions.

363 The reconstructed spectrum of the absorbed photoelectrons  
364 was first used to calibrate the pixel response sector by sector.  
365 In the following discussion, all data refer to one of the  
366 four sectors at  $V_{\text{bias}} = -200 \text{ V}$  and for an integration time  
367 of 12.8  $\mu\text{s}$ . This value has been chosen to collect enough  
368 statistics in a reasonable amount of time, without increasing  
369 the noise contribution, due to the leakage current, too  
370 much. Cluster signals were reconstructed by applying a double  
371 threshold method on a matrix of  $5 \times 5$  pixels selected around a  
372 candidate cluster seed. Clusters were requested to have a seed  
373 pixel with an SNR, S/N, of at least 6.0 and the neighboring  
374 pixels an S/N in excess of 4.0.

375 In Fig. 12, we show the spectrum of the cluster signals  
376 (left) and the one of the seed pixels only (right). The energy  
377 peak of the distribution, including all clusters (mean value  
378  $\approx 439 \text{ ADC}$ ), was used to calibrate the pixel response.  
379 The analog gain of the full readout chain was found to  
380 be  $\approx 124 \text{ mV/fC}$ , in good agreement with simulations  
381 ( $\approx 130 \text{ mV/fC}$ ). The energy resolution [full-width at half-  
382 maximum (FWHM)] depends on the cluster multiplicity; it is  
383  $\approx 1.1 \text{ keV}$  when all clusters are included (regardless of their  
384 size) and is reduced to  $\approx 0.7 \text{ keV}$  for single-pixel clusters.  
385 On the seed value distribution, the peak corresponding to  
386 the full charge collection of the 5.9-keV photoelectrons can  
387 be recognized at  $\approx 449 \text{ ADC}$ . The charge deficit of  $\approx 1\%$   
388 with respect to the distribution, including all clusters, puts  
389 a lower limit to the CCE of the detector. It is interesting  
390 to note that also the peak of the 6.5-keV photons, centered  
391 at  $\approx 500 \text{ ADC}$ , can be distinguished. We used the gain  
392 information to evaluate the noise performance of the prototype  
393 (sensor and electronics). For each pixel, its noise was measured  
394 as the rms of the pedestal distribution in dark conditions. The  
395 noise distribution for the full matrix is  $\approx 12 \text{ ADC}$  (two ADCs  
396 coming from the readout chain: DAQ and readout boards)  
397 which, expressed in electrons after the calibration, is shown  
398 in Fig. 13. The mean noise value is found to be  $\approx 40 \text{ e}^-$  at  
399 room temperature.

400 In order to study the charge sharing between the pixels in  
401 the two configurations, the cluster size and shape were also  
402 analyzed, applying both front- and back-side irradiation. The  
403 results are shown in Fig. 14, on the left for front illumination  
404 and on the right for back illumination. It can be observed,  
405 in both cases, how the cluster size is limited to 4 pixels  
406 since clusters with a multiplicity larger than 5 are only a  
407 small fraction of the total ( $<1\%$ ). This proves how charge

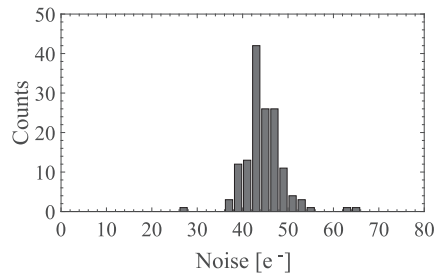


Fig. 13. Noise distribution at room temperature with  $V_{\text{bias}} = -200$  V and an integration time of 12.8  $\mu$ s.

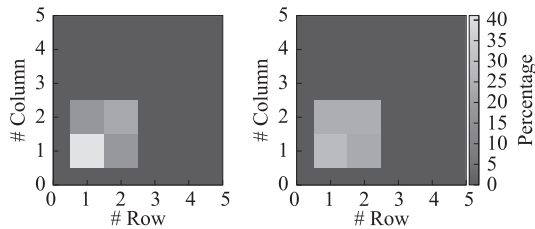


Fig. 14. Cluster size at  $V_{\text{bias}} = -200$  V in front illumination (left) and in back illumination (right).

408 sharing is small, and the cluster size is mainly affected by the  
 409 photon conversion position. In addition, the observation that  
 410 the cluster size in back illumination is comparable with the  
 411 one in front illumination confirms that, at the selected voltage,  
 412 the sensor is FD and charge collection is dominated by the drift  
 413 mechanism.

## 414 V. CONCLUSION

415 In this article, we have demonstrated the feasibility of  
 416 FD-MAPS in a 110-nm CMOS process. The first experimental  
 417 results confirm the expected sensor characteristics for a pixel  
 418 thickness up to 300  $\mu$ m and a pixel pitch down to 25  $\mu$ m.  
 419 A large-area active pixel detector is currently under develop-  
 420 ment and will be used to validate the technology in the context  
 421 of a charged-particle tracking experiment. The interest of the  
 422 developed process, however, is not limited to charged-particle  
 423 detection applications. The detection of photons with high  
 424 penetration depth, i.e., X-ray imaging as well as time-resolved  
 425 near-infrared imaging, are potentially interesting application  
 426 scenarios where the proposed technology can be competitive  
 427 with other state-of-the-art approaches.

## 428 ACKNOWLEDGMENT

429 The research activity presented in this article has been  
 430 carried out in the framework of the SEED and ARCADIA

431 experiments. The authors acknowledge the support from our  
 432 colleagues at RBI, Zagreb, Croatia, in operating the tandetron  
 433 experimental setup.

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