Doctoral Dissertation
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(32.nd cycle)

Enabling Field-Coupled Nanocomputing Multi-Technological Circuits: Design, Simulation and Validation

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The Moore's law defined the trend for digital circuits over the last 50 years. The number of transistors inside a single chip has doubled every year and a half thanks to dimensions scaling. However, this trend is reaching an end due to physical limitations. Dimensions and power density are the main issues. Transistors gate length below 5 nm will be probably the last technology node of the CMOS (complementary metal oxide semiconductor). Furthermore, the power density inside the chip, increasing with the performance of the circuit, is a big limit for the current technology. For these reasons new technologies are being studied in order to find possible alternatives. In particular, the QCA (quantum-dot cellular automata) technology is one of the most promising. Different implementation of this technology are currently studied by the research community. Molecular and magnetic QCA are addressed in this work. These technologies seems promising thanks to a lower power consumption, compatibility with CMOS fabrication process and their non-volatile nature. In fact, the concept of logic-in-memory can be explored using these technologies. However, their performance is not yet comparable with the CMOS technology.

Technologists focus on the design of the single device and its characteristics. However, even at the early stage of development, a circuit level exploration is necessary.

This kind of analysis can be used to verify the behavior of new technologies inside digital circuits. Furthermore, parametric analysis are mandatory to understand the effect of modification of properties of the devices. Another key aspect is the research of architectural optimization specifically designed to take advantages from the technological properties. These kind of explorations need software tools, like CAD (Computer Aided Design) and EDA (Electronic Design Automation), in order to speed up the process.

No commercial tools are available capable of handling these kind of devices. To solve this issue the ToPoliNano framework was developed at the Politecnico di Torino. This framework, comprised of different tools, enables the analysis of emerging technologies giving almost the same flow available for CMOS. In particular two tools are part of the framework. In this work an overview of the entire framework is presented, and a new simulator is introduced. Currently the framework is composed by ToPoliNano and MagCAD.

ToPoliNano is a tool that starts from a HDL (Hardware description Language) description of a circuit and performs the physical place & route based on the technology constraints. Different optimization algorithms are available in the tool and the user can also modify some properties of the technology. It supports hierarchical layout and it is possible to select different approaches in order to handle the hierarchy of the circuits. The tool is not focused on logic synthesis, however VHDL and Verilog are supported. After performing the layout of the circuit it is possible to run simulations to verify the layout thanks to a behavioral simulation engine. At the moment of writing it supports iNML technology.

MagCAD on the contrary is a custom layout editor. Firstly, it is possible to design a new circuit simply placing the technology building blocks inside a drawing area. It is possible also to open a ToPoliNano layout file and modify the circuit. This tool supports hierarchical layouts too. Furthermore, 3D circuits can be designed. After the design phase it is possible to extract a VHDL netlist based on the technological elements. Specifically designed model are embedded in the generated file and are solved during the simulation, which can be performed using commercial HDL simulators. The HDL netlists extraction is performed using the FunCoDe (Function and Connection Detection) algorithm. This tool fully supports two implementations of magnetic QCA (iNML and pNML) and MolQCA. Furthermore, the entire framework is based on general tools and technological plugin. In this way new technology could be easily added.

The main contribution described in this work is FCNS (Field-coupled nanocomputing simulator). This tool, that will become part of ToPoliNano, is a new simulator capable of handling different FCN technologies. A tech-independent core was developed following the idea of the framework. Furthermore, three simulation engines

were added to demonstrate the flexibility of the system. MolQCA and iNML can be simulated using FCN. Another strength of FCN is the possibility to define different simulation engines for the same technology: iNML can be handled with both behavioral or physical engines. In order to verify the simulator capabilities, several circuits based on the different technologies were simulated and the results compared to state of the art simulators. FCNS performance was compared with the other simulators: FCNS is in general faster than the reference simulators giving compliant results.

The ToPoliNano framework can be used to perform circuit level exploration of digital circuits. The results obtained with this kind of analysis can be used to define new trends for the development of those technologies.