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Minimum-Effort Design of Ultra-Low Power Interfaces for the Internet of Things

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***Abstract*—This paper briefly summarized a recent research activity intended to substantially enhance the scalability of analog blocks with technology and voltage by re-thinking analog functions in ICs in digital terms. On the contrary, the implementation of analog functions, which are however essential to acquire data from sensors, is nowadays the real bottleneck and the most serious concern and limiting factor for the further development of IoT applications. In the foreseeable cross-domain approach, design and testing methodologies from the digital world will be extended and frontier design concepts like near-threshold operation further exploited.**

Keywords—Fully-synthesizable, standard cell-based, technology portable, low design effort, low area.

I. Introduction

Internet of Things (IoT), i.e. the vision of a fully interconnected world where pervasive integrated electronic systems embedded in everyday life objects (e.g. automobiles, household appliances, clothes) to collect, process and exchange useful information in a global data network, is one of the main technological challenges for the near future. The idea of IoT along with its practical feasibility and success relies on the possibility to integrate more and more complex functions in extremely compact, low cost, energy autonomous Systems-on-Chip (SoC). The technology scaling described by the Moore's law in Fig. 1 increases density and complexity of the integrated systems. However, feature-size shrinking only improves the performance in terms of speed, power consumption, and cost of digital ICs, while Analog ICs scarcely benefit from scaling. As example, Fig.2 shows how the area of analog fundamental building blocks such as Operational Transconductance Amplifier (OTA) and Bandgap Reference, have been negligibly affected by this trend while digital blocks like SRAM have continuously benefited from technological advances. In ten years, the same analog function is implemented in an area in which the number of digital building blocks that can be placed is more than 5x the number of blocks that were placed a decade before (from 63 kbit of SRAM in 2003 to 352 kbit in 2013).

The design of analog cells in low-voltage, aggressively-scaled, mostly-digital technologies is more and more challenging because of reduced signal swing, worse matching and generally poor "analog" characteristics of nanoscale transistors. Moreover, Fig. 3 shows that, despite the dramatic improvements in data processing, battery capability does not follow the same trend [1]. It means that the limitations of analog cells in terms of energy efficiency and low-voltage operation are getting more and more serious. In addition, the situation is even more critical for energy-autonomous systems intended to operate from energy harvested from the external environment, where operation from a not accurately fixed power supply should be targeted. However, IoT applications require high integration density, low power consumption and low unit cost, as well as analog interfaces for IoT devices typically do not require outstanding performance in term of

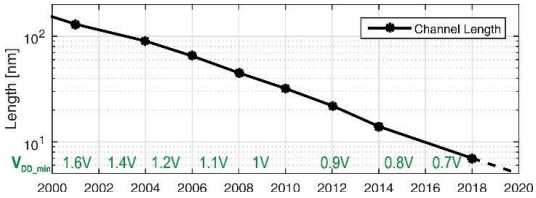

Fig. 1. Moore's Law with Voltage Supply scaling [1]

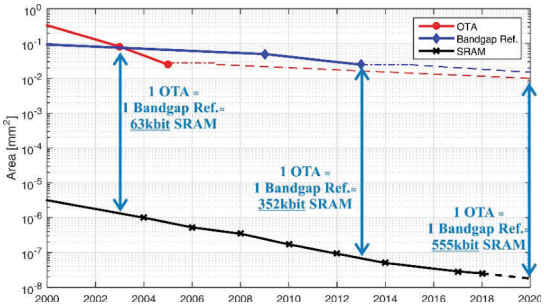

Fig. 2. Scaling of Analog ICs blocks as Operational Transconductance Amplifier (OTA), Bandgap and Digital ICs blocks as bit size of SRAM [2] .

	2009	2014	Yearly changes
Computational Performance (Normalized)	1	57	125%
Tickness	12.5mm	~8mm	-7%
Battery Capability	1500mAh	2800mAh	10%

Fig. 3. Phone's Improvements of Performance/Battery-Capacity/Thickness [3].

signal-to-noise ratio, operation speed and bandwidth of state-of-the-art analog techniques.

This scenario moves researches on architectures and sub-systems that drastically reduce the design effort and are technology scaling-friendly or portable [4] - [5] . In particular, the authors' project ULPIoT [4] is aimed in finding alternative IC design solutions to implement analog functions exploiting a digital (automated) design flow, scaling both dimensions and operating voltages. This allows the low-cost integration of multiple interfaces for different sensors in the same SoC and allows operation from a very low, possibly not accurate power supply as those obtained from harvested energy.

II. DLS Logic

The breakthrough of ULPIoT up-to-date are two: the first pW-range wake-up oscillator for IoT sensor nodes able to operate from 0.3V to 1.8V, avoiding the traditional need of additional power-hungry voltage regulation [7] – [9] and the first fully synthesizable Digital-to-Analog Converters (DACs) able to be designed with a fully automated digital design flow [10] - [11].

A. Dynamic Leakage Suppression (DLS) Logic

Slow oscillators that periodically wake up the sensor nodes are fundamental building blocks in emerging Internet of Things (IoT). Being always on, wake-up oscillators power

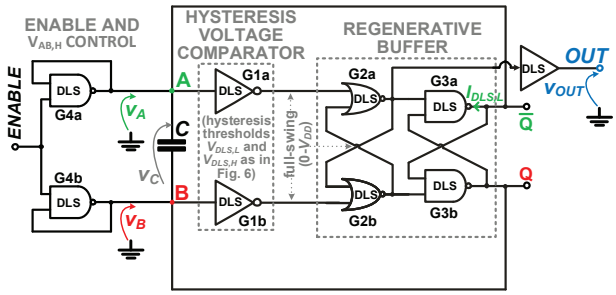

Fig. 4. Gate-level architecture of the proposed wake-up oscillator.

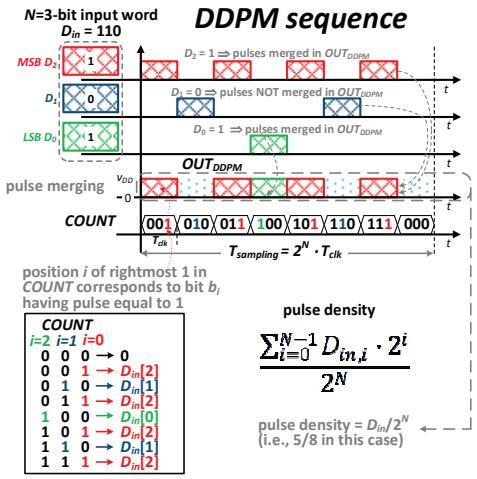

Fig. 5. Main properties of DDPM modulation [7] (example with N=3 bit).

consumption sets the very minimum power consumption of an IoT sensor node under practical duty-cycles. The proposed oscillator is reported in Fig. 4 [7] – [9]. It can work stand-alone, with no further voltage or current reference and with a low frequency sensitivity to the supply voltage. Thus, the actual power consumed by the always-on oscillator, and hence by the entire system is drastically reduced.

B. DAC Architecture

The proposed DACs significantly reduce the design effort compared to conventional analog design styles as they are based on digital standard cells approach [10] - [11]. This enables digital-like shrinkage across CMOS generations and hence low area at down-scaled technologies, as well as operation down to near-threshold voltages. Three different versions have been proposed. The conversion principle is based on a Dyadic Digital Pulse Modulation (DDPM) modulation [12] sketched in Fig. 5 and a first-order RC low-pass filter (Fig. 6). On this basis, the first DAC with a nominal resolution of 12-bit exhibits a graceful degradation under voltage/frequency overscaling [10]; the others are 16-bit and 12-bit versions pointing-out respectively only performance and area reduction [11]. All these characteristics make the proposed solutions highly suitable for the IoT nodes.

C. Other

Another minor ULPIoT outcome [4] is based on the automatized design approach employed to conceive analog comparison using only standard cells (logic gate) [13].

Moreover, as recent result, the first (at the best of authors-knowledge) designed and tested Current-input fully synthesizable Analog-to-Digital Converters (ADCs) has been recently proposed [13] .

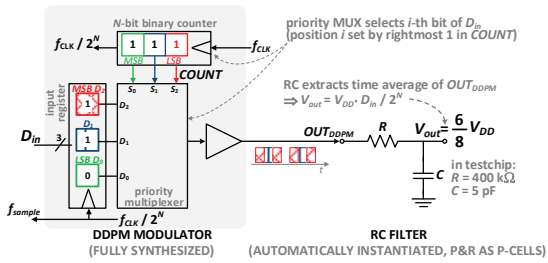

Fig. 6. DDPM DAC architecture, comprising a digital block generating the DDPM sequence and a 1st-order RC filter extracting the DC value of its output voltage.

III. Conclusion

A novel paradigm in mixed-signal IC design explored in [4] have been briefly overviewed in this paper. The proposed digital-in-concept design results in reduced form factors, improved energy-efficiency, extended lifetime and lower cost of any electronic device. This addresses the current challenges in feature-size shrinking, design effort reduction and energy efficiency that will become more and more critical in the IoT era.

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