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Ultra-Low Power and Minimal Design Effort Interfaces for the Internet of Things

(Invited paper)

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Abstract— This paper reviews the results of recent researches aimed to extend the standard-cell based digital design flow to analog building blocks, so that to enhance scalability, reconfigurability and portability across technology nodes and to reduce design effort, time-to-market and costs. In this framework, the application of the proposed fully digital design approach to a wake up oscillator and to a Digital-to-Analog Converter, which are two building blocks widely employed in IoT sensor nodes, is illustrated in detail.

Keywords—Fully-synthesizable, standard cell-based, technology portable, low design effort, low area, Wake-up oscillator, Digital-to-Analog Converter.

I. INTRODUCTION

Internet of Things (IoT), is the vision of a fully interconnected world where pervasive integrated electronic systems embedded in everyday life objects interact to collect, process and exchange useful information. Enabling the IoT faces technological challenges and relies on the possibility to integrate more and more complex functions in extremely compact, low cost, energy autonomous Systems-on-Chip (SoC) [1]. Thanks to technology scaling, described by the Moore's law as in Fig. 1, the density and complexity of integrated systems can be increased. However, feature-size shrinking only improves the performance in terms of speed, power consumption, and cost of digital ICs, while Analog ICs scarcely benefit from scaling [2]. As an example, Fig. 2 shows how the area of analog fundamental building blocks such as Operational Transconductance Amplifier (OTA) and Bandgap Reference, have been negligibly affected by this trend while digital blocks like SRAM have continuously benefited from technological advances. In ten years, the same analog function is implemented in an area in which the number of digital building blocks that can be placed is more than 5x the number of blocks that were placed a decade before (from 63 kbit of SRAM in 2003 to 352 kbit in 2013).

The design of analog cells in low-voltage, aggressively-scaled, mostly-digital technologies is more and more challenging because of reduced signal swing, worse matching and generally poor "analog" characteristics of nanoscale transistors. As a consequence, analog cells are progressively occupying a larger percentage of the die area in mixed-signal designs and are nowadays the main bottleneck - in terms of area and energy efficiency - which is limiting the further development, performance, and the costs of present day and future SoC solutions. In particular, the limitations in terms of integrability of analog functions in present day advanced CMOS technology is - and is going to become in the near future - a major obstacle to the development of SoC for

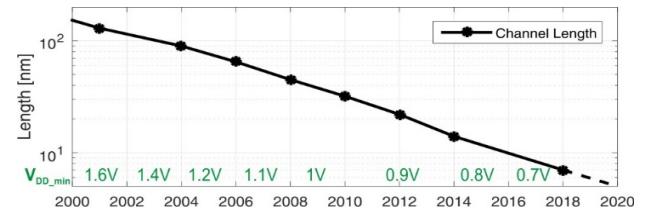


Fig. 1. Moore's Law with Voltage Supply scaling [1]

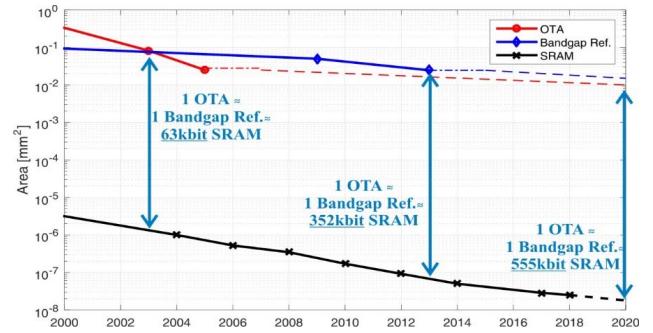


Fig. 2. Scaling of Analog ICs blocks as Operational Transconductance Amplifier (OTA), Bandgap and Digital ICs blocks as bit size of SRAM [2].

	2009	2014	Yearly changes
Computational Performance (Normalized)	1	57	125%
Thickness	12.5mm	~8mm	-7%
Battery Capability	1500mAh	2800mAh	10%

Fig. 3. Phone's Improvements of Performance/Battery-Capacity/ Thickness [3].

emerging analog intensive IoT and "sensor fusion" applications like sensor arrays, wireless sensor networks and body area networks including implantable and wearable devices. Moreover, Fig. 3 shows that, despite the dramatic improvements in data processing, battery capability does not follow the same trend [3]. It means that the limitations of analog cells in terms of energy efficiency and low-voltage operation are getting more and more serious. In addition, the situation is even more critical for energy-autonomous systems intended to operate from energy harvested from the external environment, where operation from a not accurately fixed power supply should be targeted. However, IoT applications require high integration density, low power consumption and low unit cost, as well as analog interfaces for IoT devices typically do not require outstanding performance in term of signal-to-noise ratio, operation speed and bandwidth of state-of-the-art analog techniques.

This scenario moves researches on architectures and subsystems that drastically reduce the design effort and are technology scaling-friendly or portable. This paper deals with alternative IC design solutions to implement analog functions exploiting a digital (automated) design flow, scaling both dimensions and operating voltages [4] - [5]. This allows the low-cost integration of multiple interfaces for different sensors in the same SoC and allows operation from a very low, possibly not accurate power supply as those obtained from harvested energy.

II. STATE-OF-THE-ART

The efforts of analog-mixed signal IC designers aim in finding the best trade-offs among speed, noise and power consumption. As analog building blocks and digital counterparts co-exist in any System-on-Chip, analog ICs are forced to conform to the evolution of digital ICs. Moreover, the power consumption of analog ICs (static consumption) is becoming even more important as CMOS technology scales to 5nm.

Digital-assisted analog ICs for the calibration and on-line correction of mismatch and other errors (i.e. in Analog-to-Digital Converters - ADCs) were developed in the last decade. Nevertheless, the interest toward analog solutions where the interaction with the digital part is more and more pervasive and whose operation concept is more and more digital in itself has been constantly increasing in recent years. In this perspective, ADCs [6], phase-lock loops [7] and class-D amplifiers [8] with a highly digital architecture, that provide better performance at lower supply voltages and area, have been proposed. A new paradigm in analog cell design that exploits design methodologies that are essentially digital has gained considerable interest in the last two years. A first digital-in-concept implementation of a Differential Stage was proposed in [9]. A tentative of digital Bandgap Reference in [10] continues to be mostly analog while another proof-in-concept digital prototype has been conceived [11]-[12].

While previous attempts towards “mostly-digital” analog IC design have been reported in the last years [6]-[12] the goal of the design approach discussed in this paper is to systematically re-think analog functions in ICs in digital terms in order to conceive and implement IC analog building blocks by means of a fully synthesizable design approach. This to exploit the automated digital tool to design analog (traditionally custom) building blocks. An example is the automatized design approach employed to conceive analog comparison using only standard cells (logic gates) [13].

This paper deals with two crucial building block in IoT sensor node as a wake-up oscillator and a Digital-to-analog Converter. The features of the first pW-range wake-up oscillator for IoT sensor nodes able to operate from 0.3V to 1.8V, avoiding the traditional need of additional power-hungry voltage regulation is described in Section III. Then in Section IV, the properties of the first fully synthesizable Digital-to-analog Converters (DACs) are considered.

III. WAKE-UP OSCILLATOR IN DLS LOGIC

Slow oscillators that periodically wake up IoT sensor nodes are fundamental building blocks in heavily duty cycled integrated systems that achieve very low power consumption

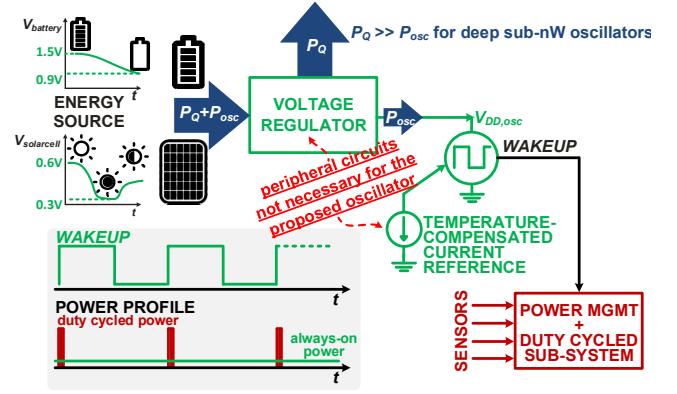


Fig. 4. Wake-up oscillators for duty-cycled sensor nodes, and peripheral circuitry necessary for their operation (e.g., voltage regulator, reference).

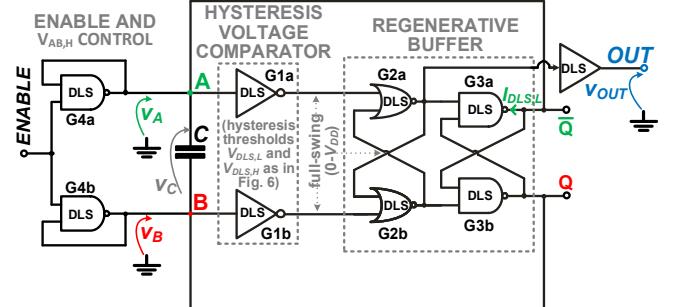


Fig. 5. Gate-level architecture of the proposed wake-up oscillator.

by staying in sleep mode for most of the time, while periodically waking up to perform the intended task as depicted in Fig. 4. Existing ultra-low power oscillators generally need always-on supply voltage regulation and temperature-compensated current reference to achieve adequate stability of frequency and power. These ancillary IC cells contribute to overall wake-up oscillator power consumption. Moreover, being always on, such power consumption sets the very minimum power consumption of any IoT sensor node under practical duty-cycles.

In order to address this issues, the proposed oscillator [14]-[16] can work stand-alone, with no further voltage or current reference and with a low frequency sensitivity to the supply voltage. Thus, the actual power consumed by the always-on oscillator, and hence by the entire system is drastically reduced. As represented in Fig. 5, the circuit solution is based on a compact architecture composed by a capacitor C and 9 logic gates implemented in the Dynamic Leakage Suppression (DLS) logic style [17]. The oscillator can be classified into 3 sub-blocks: an enabler made by two 2-input NAND; a hysteresis voltage comparator composed by 2 inverter and a regenerative buffer. The oscillation is found-out by the periodic (dis)charge of the on-chip flying capacitor C exploiting the features of the DLS logic gates.

A. Dynamic Leakage Suppression (DLS) Logic

The DLS Logic [17] (also known as Ultra-Low-Power - ULP logic style [18]) was proposed to reduce the OFF power well below the regular transistor leakage (i.e., at zero gate-source voltage), although at the cost of drastically reduced speed. The schematic of a DLS inverter gate is depicted in Fig. 6, where the pull-up (pull-down) network consists of transistor

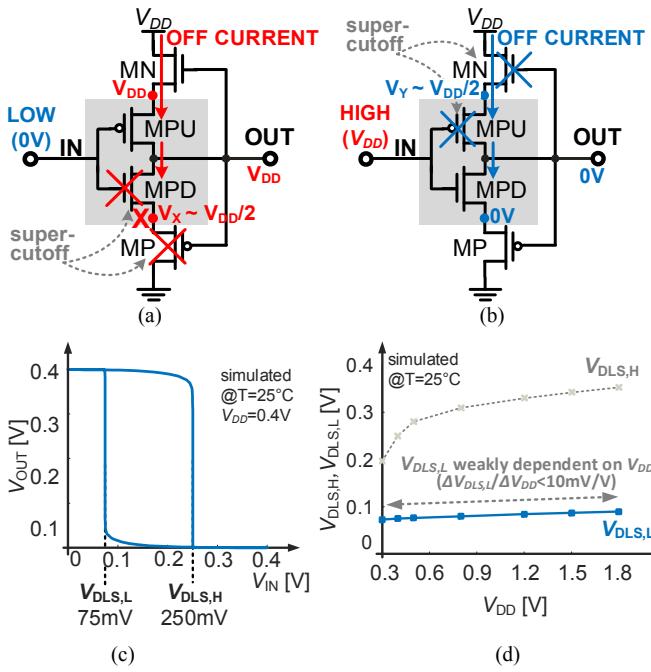


Fig. 6. Circuit analysis of the DLS inverter gate at a) high and b) low output, c) static transfer curve characteristics, d) hysteresis windows amplitude over the power supply.

MPU (MPD) as in a standard CMOS inverter gate. In general, the DLS pull-up and pull-down networks in any cell are the same as standard CMOS cells. Differently by standard CMOS logic gates, the DLS ones include an NMOS header transistor MN and a PMOS footer MP, whose gate terminal is driven by the cell output, thus creating a feedback loop. Regarding the standby current drawn by DLS logic gates, Fig. 6a shows that a low input turns off MPD and sets the output high, which in turn switches off the PMOS footer MP. Since the drain currents of MPD and MP are equal, the voltage V_x of their common node X settles to a value that is close to $V_{\text{DD}}/2$ [17]-[18]. This translates into a negative gate-source (source-gate) voltage in MPD (MP) around $-V_{\text{DD}}/2$, and hence operation in super-cutoff. Dual considerations hold for a high input, which determines super-cutoff operation in MN and MPU as shown in Fig. 6b. This explains why the OFF current of DLS logic gates is 2-3 orders of magnitude below the regular leakage current and in the order of 10fA/gate in 180nm CMOS [17].

The positive feedback loop in DLS logic also introduces hysteresis in the static transfer characteristics as shown in Fig. 6c. Interestingly, from the plot of the hysteresis thresholds versus V_{DD} in Fig. 1d, both DLS thresholds weakly depend on V_{DD} . In detail, the low hysteresis threshold $V_{\text{DLS},L}$ exhibits a very low supply sensitivity of 10 mV/V over the wide supply voltage range from 1.8 V down to 0.3 V.

The above interesting properties make DLS logic very well suited for wake-up oscillators. First, the current delivered to the load by DLS gates is very small (pA range), allowing Hz-range operation with small on-chip capacitors, and hence low area. Second, the transistor ON current is rather insensitive to V_{DD} , and permit to eliminate the voltage regulator. Similarly, the hysteresis thresholds of DLS logic

gates are relatively independent of the supply voltage, and can hence be leveraged to create a stable switching threshold that sets the oscillation frequency, as routinely required by relaxation oscillators. Third, the dominant standby current drawn by the DLS logic style is also relatively voltage-independent, which avoids the traditional drastic increase in the power consumption, when V_{DD} is increased from sub-threshold to nominal voltage.

IV. FULLY-SYNTHESIZABLE DIGITAL-TO-ANALOG CONVERTER

The proposed DACs significantly reduce the design effort compared to conventional analog design styles as they are based on digital standard cells approach. This allows the new DAC to meet the constraints imposed by tightly area- and power-constrained systems, and to address the related challenges in terms of resiliency, power-resolution scalability, low-voltage operation, area efficiency and design effort [19]-[20].

Conventional DACs suffer from catastrophic failure when the rated clock frequency f_{max} is exceeded, or V_{DD} falls below the minimum voltage $V_{\text{DD},\text{min}}$ (as depicted in Fig. 7). Indeed, operation beyond f_{max} causes timing violations in digital blocks, and exceeds the bandwidth and the slew rate specifications in analog circuits. Similarly, operation below $V_{\text{DD},\text{min}}$ causes timing failures in digital circuits at a given frequency, and pushes transistors out of the intended operating region in analog circuitry. On the contrary, the intrinsic digital nature of the proposed DACs have shown resiliency against clock frequency and voltage variations [19]. Such as graceful degradation under V_{DD} and f_{max} overscaling is related to how the Digital to analog conversion is addressed. The proposed DAC is based on the Dyadic Digital Pulse Modulation (DDPM) [21] sketched in Fig. 8.

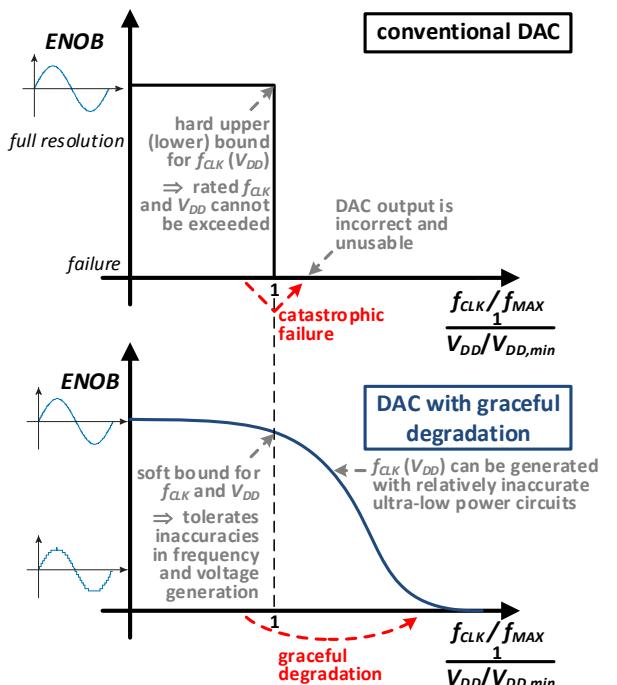


Fig. 7. Catastrophic vs. graceful degradation in digital-to-analog converters.

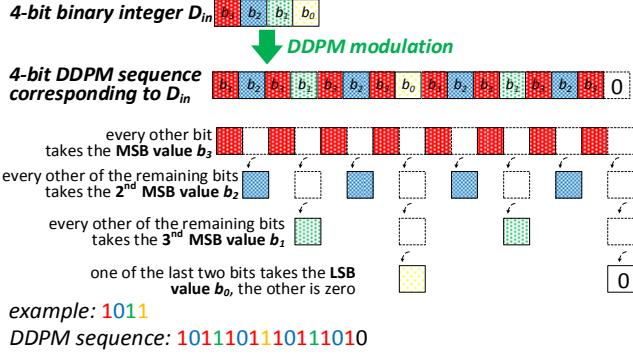


Fig.8. Example of 4-bit Dyadic Digital Pulse Modulation (DDPM) and related bit sequence associated with a generic integer $D_{in} = b_3 b_2 b_1 b_0$.

An N-bit binary code is converted into a 2^N -bit DDPM sequence. In this, the MSB of a binary code occupies the odd-numbered positions assigned b_{N-1} in the DDPM sequence. In the remaining spots, every other bit takes the value of b_{N-2} . The same assignment is recursively applied until two bits are left, of which the former is assigned to the least significant bit b_0 (LSB) of D_{in} , and the latter is forced to zero.

The DC voltage of a DDPM sequence generated by CMOS logic is extracted a simple low-pass filter, as in Fig. 9. Such a first-order low-pass filter represents the reconstruction filter that is invariably cascaded to any DAC. Based on the spectral characteristics of DDPM modulation, its time constant RC is set to make the filter cut-off frequency f_c approximately equal to $f_{sample}/\sqrt{3}$ [21]. This suppresses higher-frequency components of the DDPM sequence and requires resistor and capacitor whose values are reasonably be integrated on chip.

V. CONCLUSION

A novel paradigm in mixed-signal IC design have been briefly overviewed in this paper focusing on two main building block of IoT sensor node as a wake-up oscillator and a DAC. The proposed fully-synthesizable designs result in reduced form factors, improved energy-efficiency, extended lifetime and lower cost of any electronic device. This addresses the current challenges in feature-size shrinking, design effort reduction and energy efficiency that will become more and more critical in the IoT era.

The possibility to exploit the digital (automated) design flow even for analog building blocks can dramatically reduce the design effort of any system-on-chip that face with analog signal. The increment of the overall scalability and the higher level of automation in IC design given by a digital-in-concept approach have a straightforward and broad impact on the cost of electronic devices everyone experiences daily.

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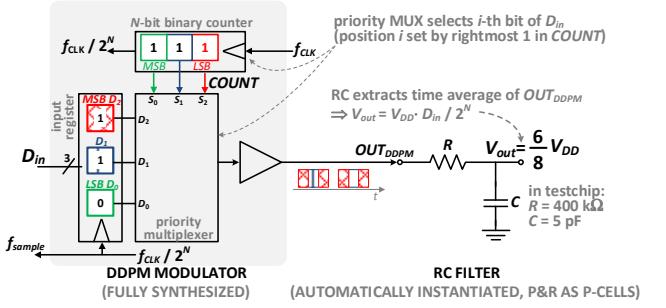


Fig. 9. DDPM DAC architecture, comprising a digital block generating the DDPM sequence and a 1st-order RC filter extracting the DC value of its output voltage.

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