Integrated front-end electronics for single photon time-stamping in cryogenic dark matter detectors

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Integrated front-end electronics for single photon time-stamping in cryogenic dark matter detectors

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Abstract: ALCOR is a first prototype of a 32-pixel low-power mixed-signal ASIC developed to readout silicon photomultipliers at low temperature. The chip, designed in 110 nm CMOS technology, performs single photon time-stamping with a maximum event rate of 5 MHz per pixel. The time measurement is performed using low-power TDCs based on analogue time interpolation. The time binning achievable at maximum clock frequency is 50 ps and the target power consumption is less than 5 mW per pixel. Generated data are serialised and transmitted through LVDS drivers. To assert the CMOS electronic behaviour at 77 K, a Test Chip has been produced and tested. Results of a digital synchronisation circuit are reported and discussed.

Keywords: Digital electronic circuits, Front-end electronics for detector readout, Cryogenic detectors, Noble liquid detectors

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1 Introduction

Silicon photomultipliers (SiPMs) are solid-state light sensors which robustness, compactness, compatibility with magnetic field and high photodetection efficiency make them strong candidates sensors for liquid noble Time Projection Chambers (TPC) employed in dark matter detection experiments [1, 2]. Current solution to readout cryogenic SiPM are based on analogue discrete electronics where generated signal is transmitted from the cryostat to an ADC module placed in the warm area [3, 4]. This paper describes the design of ALCOR, a 32-pixel mixed-mode signal CMOS electronics for the readout and digitisation of signals produced by SiPMs and optimised for an operation at cryogenic temperature. In this approach, the SiPM sensor is segmented into a sufficient number of independent cells, so that the number of photons impinging on each sensing element is small enough to avoid signal pile-up. A simple and low-power binary electronics can thus be used to perform a single-photon detection timestamp. Furthermore, digitised data can be easy multiplexed and serialised, thereby reducing the number of fibers required for data transmission from the cryostat to the outside DAQ system. The finer segmentation reduces the capacitance at the input each independent front-end. As a consequence, the same signal-to-noise ratio can be achieved with lower current per front-end pixel, maintaining the overall power dissipation comparable to that required in solutions adopting analogue summing of SiPM signals. This paper gives a general overview of ALCOR and describes the implementation of the data transmission both at the matrix level and periphery.

2 ALCOR

ALCOR (A Low-power Circuit for Optical Readout) is a first prototype of a 32-pixel mixed-signal ASIC optimised to readout SiPMs at low temperature. The chip, designed in a 110 nm CMOS technology, is implemented in an area of 4.95 mm x 3.78 mm. The CAD layout on Fig. 1 shows the floorplan of the chip, where pixels are placed in matrix structures of 4 rows and 8 columns. SiPMs are wire bonded to the pads placed on the top of ALCOR chip, then each of sensors's signal are transmitted to one pixel of the matrix. The power consumption of the single pixel is lower than 5 mW, for a total physical area of 500 μm x 500 μm. An average event rate of up to 5 MHz can be handled at the pixel level. Each pixel is designed with a regulated common-gate (RCG) input stage that acts as the interface between the sensor and the rest of the chain. Then the signal is conditioned by two amplifiers with external programmable gain. Two leading edge discriminators with external configurable threshold are used to generate the trigger CMOS signals that are fed to the pixel digital control block. The time-of-arrival for each event is built upon a convolution of a a coarse and a fine time measurement. A first time stamp is generated from a binary 15-bit coarse counter on-pixel with a time binning equal to the period of the system clock, while a fine time stamp of 9-bit is generated by a low-power time-to-digital converter (TDC) based on analogue interpolation. The TDC measures the time difference between the arrival time of the event and the next clock rising edge; this is illustrated in Fig. 2. The TDC is implemented with a Wilkinson ADC, therefore the conversion time is directly proportional to the input amplitude. The chip can be operated with a clock frequency between 80 MHz and 320 MHz. Operating the chip at 320 MHz, the TDCs have a binning time of 50 ps and a dead-time of 150 ns. Each pixel is implemented with four TDCs

that work in stand-alone when the chip operates in single-photon time-stamping mode. When the chip works in Time-over-Threshold (ToT) mode, two of the TDCs are intended for the arrival time stamp and the other two are used for the trailing edge of the trigger. The ToT operation halves the rate capability but allows for a non-linear measurement of the charge for each event. Transmitted data from each pixel are collected and wrapped in the periphery of the ASIC by the End-of-Column (EoC). Four LVDS drivers are used to transmit the data off-chip. ALCOR has been designed in such a way that the front-end and pixel operation mode can be configured externally by a FPGA and all the communications with the chip are managed through SPI protocol.

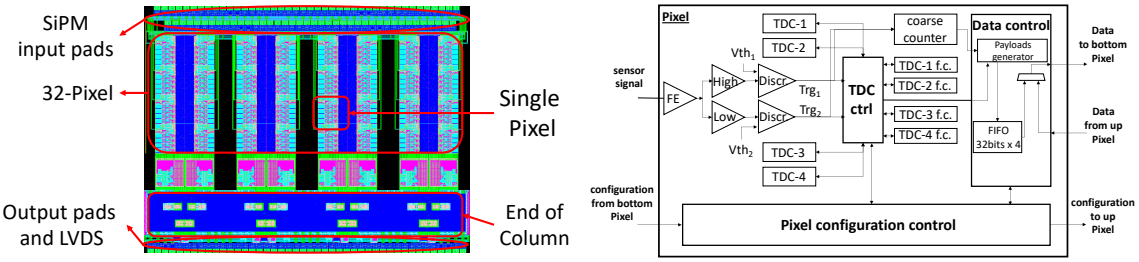

Figure 1. On the left the layout architecture of ALCOR, on the right the schematic diagram of the single pixel.

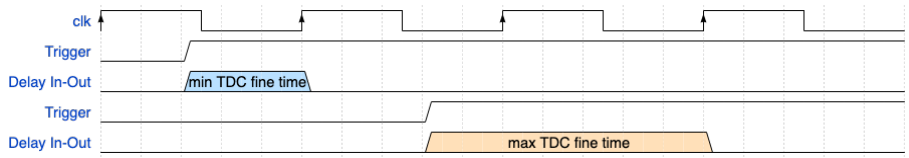

Figure 2. If the event occurs immediately before the falling edge of the clock, the TDC measures up to the first rising edge of the clock; if the event occurs immediately after the falling edge of the clock, the TDC measures up to the second rising edge of the clock.

2.1 Data transmission

When a photon is detected, the pixel generates a 32-bit event word containing a position-tag in terms of column (3-bit) and pixel (3-bit) identification, the TDC address (2-bit) used to perform the fine time conversion and a time-tag divided in coarse counter (15-bit) and fine counter (9-bit). Generated data are firstly queued and stored in a FIFO register (depth=4) in the pixel and then they are transmitted to EoC. Pixels on the same column are connected in a daisy chain network, therefore data flow downwards pixel by pixel until reach EoC. When a data word is ready, the data control starts a communication with the periphery of the chip. The data transmission timing diagram in Fig. 3 shows the hand shake protocol used between the pixel and the EoC. The communication starts with a *"write request"* to EoC (0 -> 1), which responds with a *"freeze"* signal first and then with a *"write enable from EoC"* signal. These two signals are sent through the column and enable the data transmission to all pixels ready to send data. The write token signal, referred to as *"pixel write enable"* in this diagram, is asserted by the pixel entitled to write the data bus and propagated to the bottom pixels. The data transmission of a single event-word lasts for 4 clock cycles in order

to be synchronised correctly in EoC. Internal data are transmitted only when the pixel has the token *"write enable"*, while in the other cases the pixel forward the data from upper pixels. An example with a post-layout simulation of the data transmission at the column level has been reported in Fig. 4. The transmission priority is given to pixels nearest to periphery. EoC needs at least an idle time of 3 clock cycles between two data transmission in order to be prepared for new incoming data. The total transmission lasts for 7 clock cycles. In this time window the EoC can read only one Event-Word from each column.

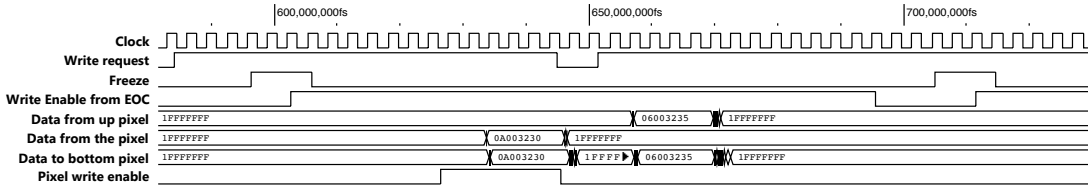

Figure 3. Timing diagram of the data transmission signalling between the data control unit in the pixel and EoC.

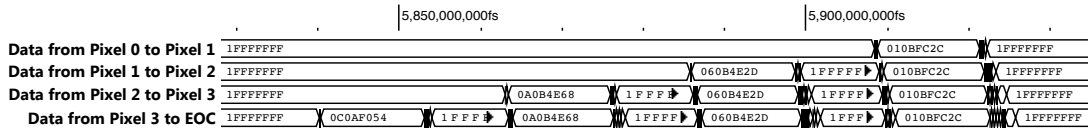

Figure 4. Time diagram of data flowing through the 4-pixel column.

The block diagram in Fig. 5 shows how data are collected and stored in EoC before to be dispatched outside the ASIC. The EoC is divided in three layers, in the first one data received from each column is stored in a FIFO of 16x32-bit. Here, data belonging to the same time window are collected together and extra information such as a header, the number of frame, the status of EoC and CRC 32-bit are added. Encapsulated data coming from two columns are then transmitted to a second layer, where a FIFO of 32x33-bit is used to store data temporarily before serialisation and off-chip transmission through LVDS links. The output data stream are encoded with a 8b/10b protocol with a maximum bandwidth of 640 Mb/s with double data rate.

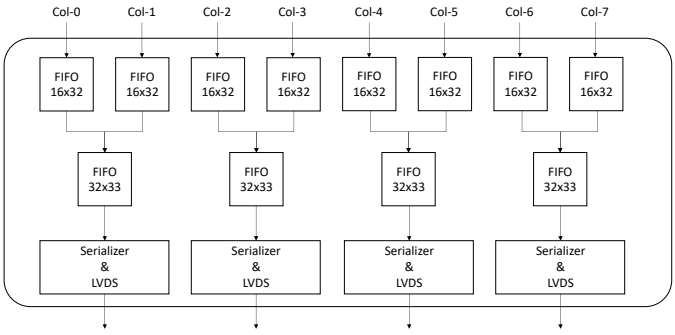

Figure 5. Schematic diagram of EoC data storage and transmission.

3 Test Chip experimental results

In order to asses significant insight of CMOS behaviour at cryogenic temperature, a Test Chip (TC) has been produced and tested. This IC embeds some of critical building blocks that are employed in the ALCOR design. In particular, a digital synchronisation circuit designed with 110 *nm* standard cells has been included in the TC. This because digital standard cells models below $-40°C$ are usually not provided by the technology vendor for timing simulation. Thus, dedicated tests at cryogenic temperature are necessary in order to evaluate the functionality of the synchronisation module and have a comparison with SPICE extrapolated models at 77 K. This module is a critical block in the architecture of ALCOR, it has been implemented to synchronise hand shaking signals between the single Pixel and EoC, as showed and discussed in the previous section. A synchronisation delay error can lead to the loss of data and therefore may compromise the ASIC functionality. Figure 6 depicts, in a time diagram, the behaviour of the synchronisation module. Depending of the arrival time of the input signal, the synchronisation time lasts in the range of a *'min delay time'* and a *'maximum delay time'*. These are the boundaries within the synchronisation time is measured. For the practicality purpose of the test, only these two values are considered as comparison with SPICE simulation results. The test is done providing to the synchronisation module an input signal of 250.1 $\mu\ s$ of period and varying the clock frequency from 40 MHz to 250 MHz. The minimum and maximum time delay between the asynchronous input signal and the synchronised output signal are then measured through an oscilloscope. Cryogenic test are performed cooling the TC in a bath of liquid Nitrogen, in order to reach 77 K temperature (Figure 7). Test results reported in Figure 8 shows min/max synchronisation delay in terms of time difference between room temperature and cryogenic temperature for both simulated and tested value. The time difference observed between the two temperatures do not lead the functionality of the digital circuit. From this graph it is possible to evince how the simulated value, performed using SPICE tool, are well reasonably approximated to the experimental behaviour of the digital circuit even without a model defined by the technology vendor. Therefore, it is possible to evince that no particular issue with the synchronisation circuit should be expected at 77 K.

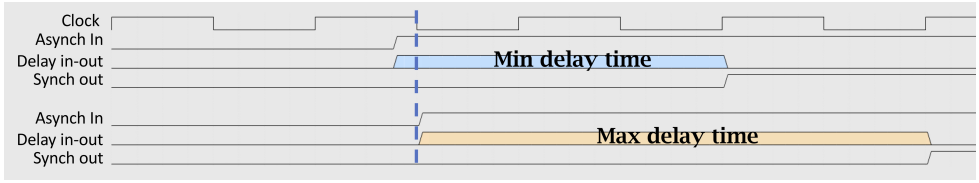

Figure 6. Synchronisation time diagram. If the input signal occurs immediately before the falling edge of the clock, the synchronisation lasts for 1 clock period and half, otherwise it lasts for 2 clock periods and half.

4 Conclusion

ALCOR is a versatile SiPM readout ASIC suitable for 3D integration with the silicon sensor. The first prototype implements a 32-pixel matrix, but the readout and data architecture is scalable to larger matrices. The chip performs time-based measurements of the Time-of-Arrival and Time-over-Threshold of signals produced by a SiPM, and a system clock of 320 MHz allows for a TDC

Figure 7. From left: The Test Chip is wire bonded in the center of the test board; Test setup used to measure time delays; Test board is dipped inside the small dewer in a bath of liquid Nitrogen at 77 K.

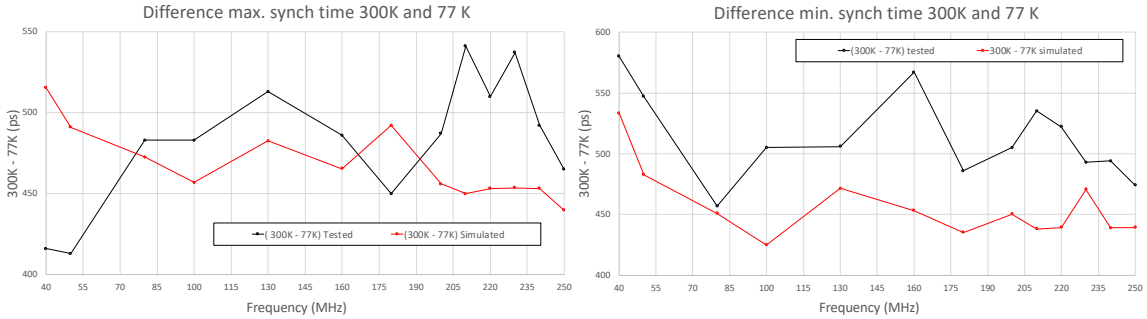

Figure 8. Results of synchronisation module expressed as time difference (300 K - 77 K), for both minimum and maximum time delay. In the graph are reported also time delay obtained from test and SPICE simulation.

time binning of 50 ps. An operation clock down to 80 MHz expands the usability of the chip on very low-power and low-rate applications with less stringent needs in terms of time resolution. ALCOR has been submitted to fabrication using a CMOS 110 nm technology node. The preliminary test performed on the Test Chip shows a correct behaviour of the digital synchronisation circuit at 77 K and that this can be predicted using extrapolated model of SPICE simulation tool.

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