Source/Load-Pull Characterisation of GaN on Si HEMTs with Data Analysis Targeting Doherty Design

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***Abstract*—This paper presents the source/load-pull characterisation of GaN HEMTs on Si substrate, with an analysis of the measurement data oriented to aid the design of Doherty power amplifiers for satellite communication applications in the 17-20 GHz band. In particular, fundamental load-pull, in both class AB and C, is used to identify the output power and efficiency contours and assess the scalability of the performance vs. device size. Second harmonic source/load-pull data is used to determine the harmonic impedance regions to avoid during matching network synthesis. The load-pull data allows to predict the optimum load modulation trajectory to be synthesised in the design phase and the associated performance in terms of efficiency, gain compression and phase distortion.**

***Index Terms*—Gallium nitride, K-band, satellite communications, power amplifiers.**

I. Introduction

In satellite systems, achieving a minimum target for efficiency in the transmitter does not only affect the cost of a project, but can be the factor that decides if a system can be deployed or not. In fact, in space applications, some specifications such as device temperature, DC power, and weight are not negotiable, since they affect the reliability and mission lifetime [1].

The power amplifier (PA) is the most critical component in the transmitter for its efficiency [2]. To fulfil the linearity requirements, the PA must operate in back-off, meaning a large efficiency reduction in conventional PAs. Hence, the adoption of efficiency enhancement solutions such as the Doherty power amplifier (DPA) [3], [4] is researched for satellite applications [5].

This paper focusses on the experimental characterisation of GaN on Si HEMTs aiming at providing key information for the design of DPAs for space applications, in particular for the Ka-band downlink that operates in the 17–20 GHz band. The work is motivated by the fact that foundry models are generally accurate enough to provide good guidance for designing conventional amplifiers, but they are not optimised for more complex designs such as DPA. The dedicated measurement campaign, with a proper data analysis, provides instead tailored information to the designers to improve the probability of a first pass successful design.

II. Fundamental load-pull results

GaN on Si [6] provides a cheaper alternative to GaN on SiC [7], at the cost of lower power handling and higher substrate losses. The transistors characterised in this paper are AlGaN/GaN HEMTs on a 100 μm Si substrate. The drain-source distance is 3 μm and the gate length is 100 nm, providing a cut-off frequency of around 100 GHz. An active load-pull system based on a vector signal analyser is used for the characterisation. A number of different transistor sizes have been characterised in continuous wave (CW) in this campaign, including devices with 4, 6 and 8 fingers, and gate widths of 50, 70, and 100 μm, at the fundamental frequency of 17.3 GHz. If not indicated otherwise, the devices are biased in class AB at 11 V, 60 mA/mm to respect derating rules, at baseplate temperature of 25°C.

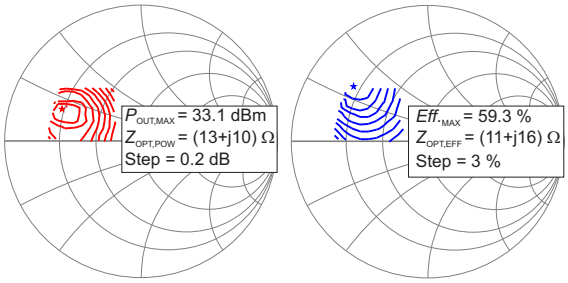

Fig. 1. Measured output power (left) and drain efficiency (right) load-pull contours for the 8x100 μm device at an input drive corresponding to approximately 2 dB gain compression.

Fig. 1 shows the output power and drain efficiency contours for the 8x100 μm device, at an input drive corresponding to approximately 2 dB gain compression. The optimum output power is 33.1 dBm, with associated drain efficiency of 54.7%. The maximum efficiency is 59%, with associated output power of 32.2 dBm. Fig. 2 compares the maximum output power measured

for each device size with the linear scaling of the smallest device (4x50 μm) power.

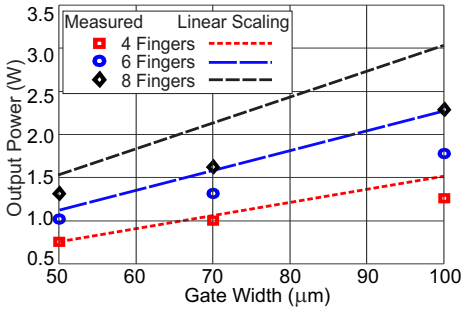

Fig. 2. Measured maximum output power for different device sizes, compared with linear scaling from the measured 4x50 μm performance.

The load-pull measurement has been repeated at baseplate temperature of 75°C, and a power/gain reduction of around 0.5 dB has been found consistently across the several peripheries.

Fig. 3 shows, for the 8x100 μm HEMT, the optimum load for output power and the corresponding gain curves at different bias conditions. The optimum load changes in class C, suggesting that a tailored impedance matching for the Auxiliary can improve performance. Moreover, both gain and maximum power are reduced in deep class C; this effect must be accounted for in the design since it will affect the power budget and load modulation.

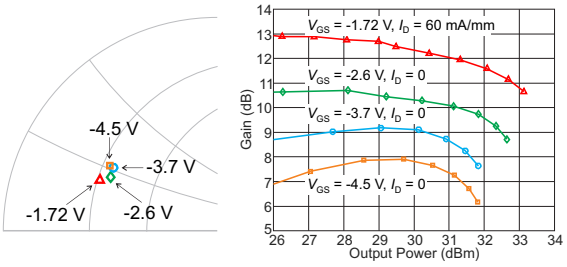

Fig. 3. Load pull results at different gate bias points for the 8x100 μm device. Measured optimum load for output power (left). Measured gain vs. output power (right) with load at the corresponding optimum.

III. Second Harmonic Source-/Load-Pull

Far from saturation, the second harmonic termination, at both load and source, is the one providing the largest effect on PA efficiency [8]. The active load-pull setup used for the experimental characterisation can control the second harmonic load ($\Gamma_{\mathrm{L,2f_0}}$) and source ($\Gamma_{\mathrm{S,2f_0}}$) impedance independently from the f_0 load impedance. The measurement procedure has been to identify the optimum load at f_0 first, and then to perform a nested sweep of $\Gamma_{\mathrm{L,2f_0}}$ and $\Gamma_{\mathrm{S,2f_0}}$ phases, while their magnitude has been fixed at 1. The input drive has been adjusted to avoid strong

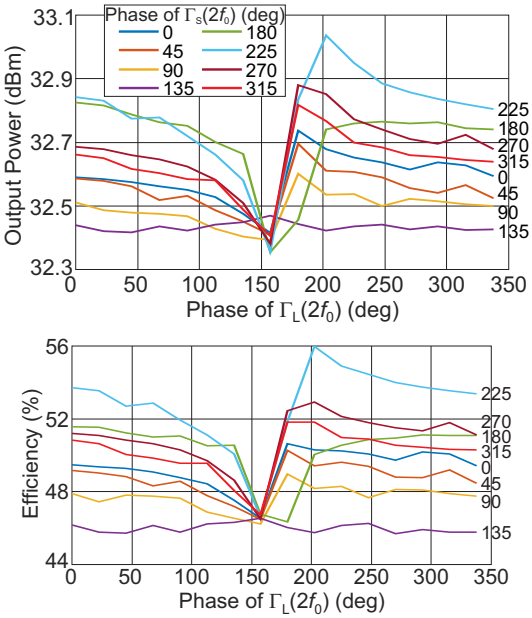

Fig. 4. Measured output power (top) and drain efficiency (bottom) vs. phase of $\Gamma_{\mathrm{L}}(2f_0)$ for the 8x100 μm device, for different $\Gamma_{\mathrm{S}}(2f_0)$ conditions. Fundamental load is at optimum for output power.

saturation. Fig. 4 show the measured results in terms of output power and drain efficiency vs. $\Gamma_{\mathrm{L,2f_0}}$ phase, for different $\Gamma_{\mathrm{S,2f_0}}$ phase values. There is clearly a critical region for $\Gamma_{\mathrm{L,2f_0}}$ from $\simeq 130°$ to $\simeq 200°$, where both output power and drain efficiency drop significantly and where small deviations in the synthesised impedance can lead to large variation in performance. On the other hand, there is a quite large region, from $\simeq 200°$ to $\simeq 360°$, where both output power and efficiency are higher and slowly varying. Regarding instead $\Gamma_{\mathrm{S,2f_0}}$, the region to avoid is located between 0 and $\simeq 130°$. For both load and source terminations, the region with high power and efficiency is reasonably wide. This means that the design space for the harmonic terminations is broad enough to increase the degrees of freedom in the design and to limit the sensitivity of performance to matching network inaccuracy. Overall, the proper selection of second harmonic terminations can improve output power up to 0.7 dB, and drain efficiency of 8% points. The same trend in terms of optimum terminations and associated performance has been found for all the devices characterised.

IV. DPA-oriented analysis of experimental data

Considering Fig. 2, it is clear that the very large peripheries have a considerably reduced power density. For this reason, a smaller size device, the 6x50 μm, that provides a maximum power slightly above 1 W, has been selected as a better candidate for the DPA design and for the data analysis oriented to DPA design.

The load modulation of the Main device largely determines the behaviour of the DPA in terms of drain efficiency and distortion. The optimum load for maximum output power $P_{\mathrm{out,MAX}}$ can be written as $Z_{\mathrm{OPT,POW}} = 1/Y_{\mathrm{OPT,POW}}$, where $Y_{\mathrm{OPT,POW}}$ is the optimum admittance $Y_{\mathrm{OPT,POW}} = \frac{1}{R_{\mathrm{opt}}} + \mathrm{j}B_{\mathrm{opt}}$.

When considering an RC output model for the device, the optimum DPA trajectory can be described by an admittance with constant imaginary part and real part varying from $2R_{\mathrm{opt}}$ to R_{opt} in a symmetrical Doherty. In particular, for a back-off α (where $\alpha = P_{\mathrm{out}}|_{\mathrm{W}} \,/\, P_{\mathrm{out,MAX}}|_{\mathrm{W}}$) the corresponding admittance seen by the Main will be $Y_{\alpha} = \frac{\alpha}{R_{\mathrm{opt}}} + \mathrm{j}B_{\mathrm{opt}}$. By analysing the load-pull data, the loads lying approximately on the DPA trajectory can be identified, see Fig. 5(left) [9]. Then, the power sweep plots at each

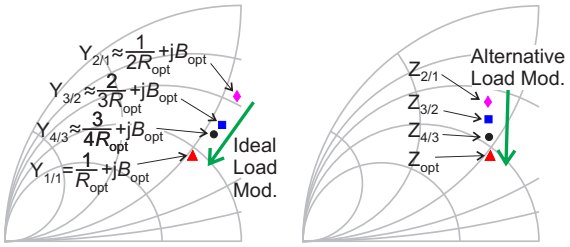

Fig. 5. Emulated DPA load trajectory on admittance chart for the Main device in the case of the 6x50 μm device. Ideal trajectory considering an RC device model (a); alternative trajectory (b).

load can be used to reconstruct the emulated load modulation for the Main amplifier. Fig. 6, left column, shows the corresponding result in terms of drain efficiency, gain, and amplitude to phase distortion (AM/PM, assuming the device to be perfectly matched at the input). The efficiency remains approximately constant at $\simeq$57%, with AM/PM in the DPA region of around 30°. The flat efficiency and the compression of around 3 dB suggest that the load trajectory followed must be rather close to the ideal DPA one, so that an RC modelling of this device size is a fair assumption. Fig. 5(right) shows an alternative load trajectory that does not correspond to assuming an RC model, and is used as a benchmark to assess the sensitivity of the device to an error in synthesising the load modulation in the design, while Fig. **??** shows the corresponding performance. The only parameter benefitting from the non-ideal load trajectory is the AM/PM. This can be ascribed to the fact that the output reactance of the device is not compensated equally throughout the trajectory compensates for the phase distortion effect due to input impedance variation.

V. Conclusion

This paper has shown the characterisation of GaN on Si HEMTs at 17.3 GHz to guide the design of a Doherty amplifier for satellite applications. The focus has been on critical characteristics such as load modulation and class C operation, as well as second harmonic source-load matching.

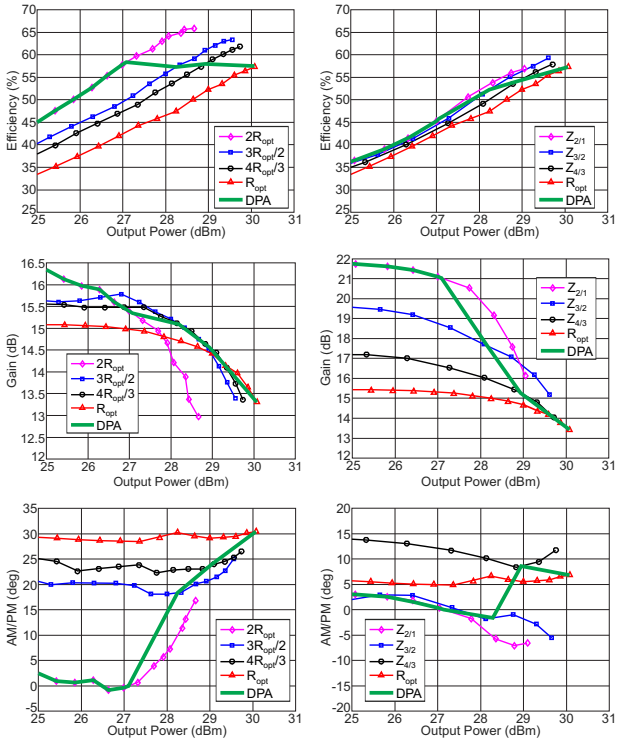

Fig. 6. Measured drain efficiency (a), gain (c) and AM/PM (e) vs. output power for different load impedances for the 6x50 μm device. With reconstructed ideal DPA trajectory (left column), and with alternative load trajectory (right column).

References

[1] N. Ayllon, et al., "Making Satellites Reliable: The Definition and Design Considerations of Space-Borne Solid-State Power Amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 9, pp. 24–31, Sep. 2016.

[2] F. Raab, et al., "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[3] V. Camarchia, et al., "The Doherty Power Amplifier: Review of Recent Solutions and Trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559-571, Feb. 2015.

[4] D. P. Nguyen, et al., "A Compact Ka-Band Integrated Doherty Amplifier With Reconfigurable Input Network," *IEEE Trans. Microw. Theory Techn.*, in press doi: 10.1109/TMTT.2018.2874249

[5] V. Valenta, et al., "High-gain GaN Doherty power amplifier for Ka-band satellite communications," *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Anaheim, CA, 2018, pp. 29–31.

[6] R. Leblanc, et al., "6W Ka Band Power Amplifier and 1.2dB NF X-Band Amplifier Using a 100nm GaN/Si Process," *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Austin, TX, 2016, pp. 1-4.

[7] V. Di Giacomo-Brunel, et al., "Industrial 0.15-μm AlGaN/GaN on SiC Technology for Applications up to Ka Band," *13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, 2018, pp. 1-4.

[8] T. Sharma, et al., "A Methodology for Implementation of High-Efficiency Broadband Power Amplifiers With Second-Harmonic Manipulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 54–58, Jan. 2016.

[9] L. Piazzon, et al., "Effect of Load Modulation on Phase Distortion in Doherty Power Amplifiers," *IEEE Microw. and Wirel. Comp. Letters*, vol. 24, no. 7, pp. 505-507, July 2014.