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Class-E Isolated DC-DC Converter with High-Rate and Cost-Effective Bidirectional Data Channel

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***Abstract*—We propose a methodology to create a through-the-barrier bidirectional communication channel between the two sides of an isolated class-E resonant dc-dc converter. Our methodology is innovative since communication occurs through the same transformer used for energy transfer, and relies on connecting and disconnecting an auxiliary capacitance. By doing so, the converter switches between a faster and a slower response without any change in the clock controlling its activity. With this, it is possible to achieve a very high-rate bidirectional communication (up to 1 bit per switching clock period) with virtually no limitations in the converter power with respect to a standard class-E implementation. Measurements performed on a prototype operating at 1 MHz and capable of delivering up to 1.2 W is presented as a proof-of-concept.**

***Index Terms*—Class-E converters, data transmission, through-the-barrier communication, resonant dc-dc converters.**

I. Introduction

GALVANIC isolation is a requirement in many electronic applications, mainly for safety and grounding purposes. It is commonly used in safety-critical devices, such as medical equipments [1]–[3], and benefit many other applications [4], [5].

In simple devices, the "isolated" part of the system is the one in charge of delivering the electrical energy, typically by means of a power transformer. Yet, more complex systems requiring galvanic isolation, also need a (possibly bidirectional) data transfer interface across the isolation barrier as sketched in Fig. 1(a). This is usually achieved by means of an extra pulse transformers [6]–[10], optocouplers [11], [12], or high-voltage capacitors [13]–[15]. Unfortunately, increasing the number of isolating devices in a system leads to many drawbacks, mainly due to the fact that these components are the most cumbersome, expensive, and difficult to integrate part of the circuit. This poses several limitations in the realization of miniaturized or even fully integrated isolated systems [16].

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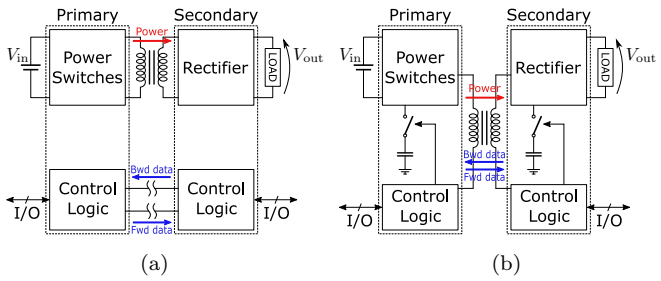


Fig. 1. (a): Standard solution for isolated power and data transfer. (b): Basic concept of the solution proposed in this paper.

The aim of this paper is to introduce a novel through-the-barrier communication technique for systems based on isolated resonant dc-dc class-E converters [17], which has minimal impact in terms of overall size/cost and negligible degradation in terms of power conversion efficiency.

The grand view of the system is depicted in Fig. 1(b), where a single isolation transformer is used **both** by the class-E resonant converter to transfer power from the primary side to the secondary side, **and** to exchange information from the secondary side to the primary side (*backward communication*) or from the primary side to the secondary side (*forward communication*). The methodology requires to connect and disconnect an auxiliary capacitance, switching, in this way, between a faster and a slower circuit response, with no changes in the converter overall activity. The proposed solution is capable of achieving a high-rate bidirectional data transfer with virtually no limitations in the converter power with respect to a standard class-E implementation. This represents a great advantage compared to other solutions proposed in the literature, that have strong limitations either in output power or in data-rate.

The paper is organized as follows. In Sec. II we propose a brief overview of the state-of-the-art in through-the-barrier communication, and a review of the most adopted solutions which appeared in the literature. Sec. III introduces the class-E converter topology considered in this work, while Sec. IV describes the modification we propose to the converter to allow communication. In Sec. V an example design is provided, while measurements on the implemented prototype are reported in Sec. VI. Finally, in Sec. VII we provide some consideration on the energetic cost of the transmission channel, and then we draw the conclusion.

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II. State-Of-The-Art and Comparison with other Solutions

A plethora of different solutions to enable power and data transfer between the two sides of isolated devices has been proposed, depending on the target application.

In telemetry (as, for example, biomedical internal electronic prosthetic devices) typical power is extremely low (μW up to a few mW). In the most general case, the design is focused on a data link via inductive coupled coils, while an additional power recovery stage aims at regenerating enough power for the secondary circuit [1]. In recent designs, to allow a high data rate while maintaining an adequate power transfer efficiency, multiband telemetry systems are employed transmitting power and data using different frequencies and sometimes different (overlapped or even completely superimposed in space) coupled coils [2], [3].

When power requirements increase, space issues are typically relaxed and the solution most commonly adopted is to use two independent interfaces, one for power- and one for data-transfer.

Optical coupling has been the leading isolation technique in the last decades in many applications in the areas of telecommunications, robotics and micro-systems [11], [12]. The main advantage is that optic is inherently immune to external electric or magnetic fields, allowing easy designs in any working condition. Furthermore, the unbounded lower coupling frequency allows for direct data transfer without any additional coding technique [18]. However, this solution has limitations in terms of integrability, speed and energy requirements, as well as in the degradation over time of the necessary LED system, which may lead to a complete loss of the coupling functionality [19].

As a consequence, in recent high-end systems, optocoupling has been replaced by alternative solutions. Many commercial products available today are based, in fact, on inductive coupling [20]–[22], and many application examples have been proposed by main ITC players [6]–[10]. Another solution is represented by capacitive coupling [13]–[15], which has the advantage of a lower cost and an easy embeddability in almost all CMOS technologies. In both cases, a much lower energy with respect to the optocoupling solution is required, and no performance degradation over time is observed. Yet, both solutions require special signal coding techniques due to a limitation of the bandwidth available for communication.

A few solutions where a single isolation device (namely, a transformer) is used both for power and data transfer has recently appeared in the literature. Yet, they all strongly differ in both methodology and application, so that a comparison (either among them, or with the methodology proposed here) is hardly possible. In [23] a $900\,\mathrm{mW}$ isolated dc-dc prototype based on a LLC full-bridge with embedded $1\,\mathrm{Mbit/s}$ communication channel is proposed. The forward communication is achieved by altering the full-bridge switching phase, and the backward one by altering the load impedance. In [24] a standard PWM-based dc-dc prototype with bidirectional communication at $1\,\mathrm{Mbit/s}$ rate is presented. The data encoding technique is based on AM for the backward communication and on FM for the forward one. Yet, the prototype is capable of delivering only $14\,\mathrm{mW}$. Another interesting solution is given by [16], where authors implemented an IC prototype capable of half-duplex communication over an integrated isolation transformer up to $40\,\mathrm{Mbit/s}$ via ASK modulation. The backward communication is performed by changing the impedance at the transformer secondary side, while the forward one requires switching a series resistor, thus modulating the oscillation signal at the transformer primary winding. However, also this solution can be used for transferring a limited power, and the prototype allows only a $23\,\mathrm{mW}$ power transfer.

III. Class-E Converter Topology and Design

The methodology discussed in this paper is applied to an isolated class-E dc-dc converter. This topology was introduced in the early '80s [25] taking advantage of the class-E RF circuit design principles. The basic idea grounding its working principle is to add passive resonant elements to a dc-dc switching converter with a twofold effect. On the one hand, additional resonant elements make many semiconductor parasitics negligible, which results in a circuit behavior almost independent of non-idealities. On the other hand, resonant elements can be designed to give a sinusoidal-like shape to the voltage across switching devices, to avoid abrupt voltage changes at switch turn-on instants. This waveform-shaping technique is commonly referred to as *soft-switching*, and alleviates switching-time requirements, thus allowing higher frequency operation and thus enabling transient response decrease and power density growth [26].

The schematic of the considered converter is depicted in Fig. 2(a). The circuit can be divided into an inverter and a rectifying block connected by an isolating transformer. The inverter block is oscillating by means of a single MOS switch directly controlled by a clock signal $V_{\mathrm{CK}}(t)$ with period T, while the rectifying block provides a dc output thanks to the diode. The reactive elements (i.e., the two capacitors C_{inv} and C_{rec}, the inductor L_{rec} and the transformer, whose inductance at the primary side is L_{p}) perform the waveform-shaping: referring to the notation of the figure, soft switching is achieved by synchronizing the zero-level-crossing of the MOS source-drain voltage $V_{\mathrm{DS}}(t)$ with the MOS turn-on instant (*zero-voltage switching*, ZVS), possibly with a zero-derivative (*zero-voltage-derivative switching*, ZVDS). A typical set of waveforms featuring both ZVS and ZVDS is shown in Fig. 2(b).

Historically, the design of a resonant converter has never been an easy task, since waveforms depend on all circuit elements. In many cases, it is difficult to achieve an exact zero value for the $V_{\mathrm{DS}}(t)$ at the MOS turn-on instant. Indeed, a low, but non-zero value is generally tolerated since efficiency is not impaired. This case is known as *quasi*-ZVS. Similarly, one can tolerate quasi-ZVDS behavior. Difficulties in the converter design are also due to the fact that, referring to Fig. 2(a), the optimal class-E condition is achieved only at the nominal I_{out} (or, equivalently, for the nominal R_{L}). To cope with a variable load, the converter design has to be increased in complexity, and one has either to lose optimal class-E operation, or to introduce a feedback such as a frequency control [25], [27]

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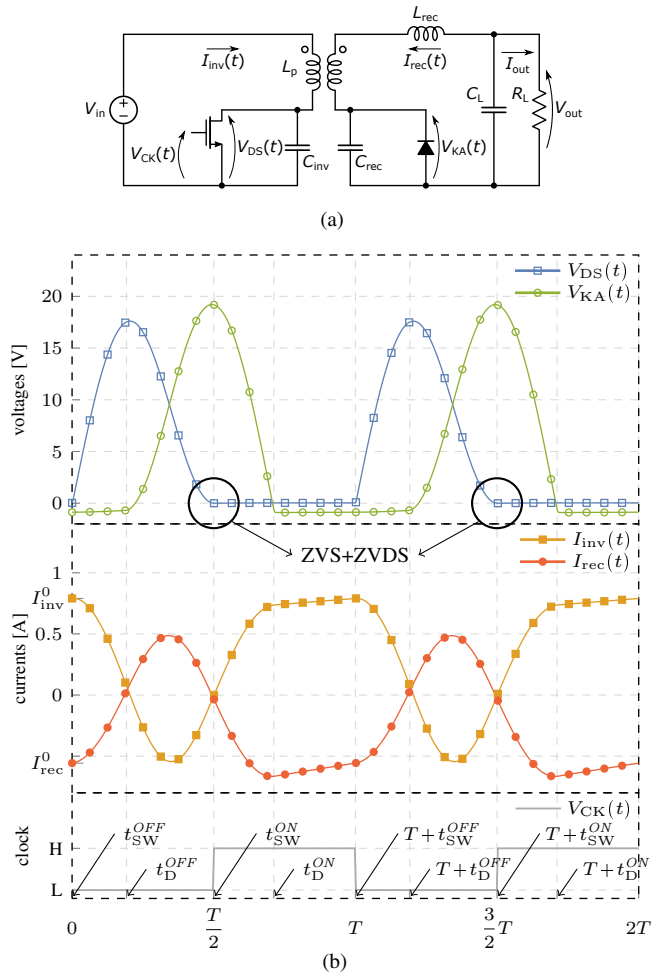


Fig. 2. (a): Schematic of the class-E resonant dc-dc converter considered in this paper. (b): Typical waveforms, showing almost perfect ZVS and ZVDS.

or an on-off control [26], [28]. The latter is preferred in more recent designs and consists in a sort of "*dimming*": the converter is turned on and off at a relatively low frequency so that it is either working at the optimal operating point, or it is off. Yet, implementing an on-off control in the schematic of Fig. 2(a) requires a (possibly isolated) feedback path. Our communication technique allows implementing such a feedback without requiring an additional (isolated) channel. Results of a possible implementation are presented at the end of the paper.

We base the design of the converter on the innovative approach recently proposed in [17]. Previous state-of-the-art was based on the so-called *sinusoidal approximation*: waveforms are assumed to be pure sinusoids or, in some design, sinusoids with a dc offset [26], [29], thus allowing to easily solve the design problem in an approximated way. Regrettably, this approach requires a further parameters tuning via very time-consuming SPICE simulations to eventually obtain the desired soft switching. This impasse is overcome in [17] by introducing an exact and semi-analytic methodology specifically developed for the converter of Fig. 2(a). Such an approach allows a direct and quick design, where optimal class-E conditions are perfectly achieved (as confirmed by the simulation of Fig. 2(b), obtained according to this procedure).

The approach, that has been further improved in [30], is also capable of take into account the most important circuit non-idealities (such as the switch on-state resistance, and all passive elements ohmic losses). This is of paramount importance as it allows us to get a very precise design even when considering elements with a finite quality factor. The basic working principle of the design procedure is to translate the problem of designing a converter that features ZVS and ZVDS when operating in the stationary condition, into a non-linear mathematical problem. For the aim of this paper, it is not necessary to recall all details; however, we summarize in the following the main steps to ease the understanding of the design approach proposed in Sec. V.

A. Design procedure steps

Let us consider a single clock period, i.e., $t \in [0, T]$. Let us also assume that $t = t_{\rm SW}^{OFF} = 0$ indicates the time instant when the MOS is externally turned off, and $t = t_{\rm SW}^{ON} = T/2$ the time instant when it is turned on. Let all quantities regulating the converter behavior (such as the main oscillating frequency, the input and output voltage $V_{\rm in}$ and $V_{\rm out}$, the reactive elements loss parameters, etc.) be a-priori fixed design constraints, except for $L_{\rm p}$, $L_{\rm rec}$, $C_{\rm inv}$ and $C_{\rm rec}$ that are design variables.

Authors of [17] were able to analytically solve the non-linear ordinary differential equation system regulating the evolution of the circuit of Fig. 2(a), and therefore to get a closed-form expression[1] for $I_{\rm inv}(t)$, $I_{\rm rec}(t)$, $V_{\rm DS}(t)$ and $V_{\rm KA}(t)$ in $t \in [0, T]$. From a mathematical point of view, the achieved expression are functions of all design parameters and of the the circuit initial condition[2] $\{I_{\rm inv}(0), I_{\rm rec}(0)\} = \{I_{\rm inv}^0, I_{\rm rec}^0\}$. Then, the design procedure involves to:

- consider $I_{\rm inv}(t)$, $I_{\rm rec}(t)$, $V_{\rm DS}(t)$ and $V_{\rm KA}(t)$ as mathematical functions of the six unknowns $L_{\rm p}$, $L_{\rm rec}$, $C_{\rm inv}$, $C_{\rm rec}$, $I_{\rm inv}^0$ and $I_{\rm rec}^0$;
- impose the converter stationary condition by means of mathematical constraints as

$$I_{\rm inv}(T) = I_{\rm inv}^0,\ I_{\rm rec}(T) = I_{\rm rec}^0,\ \langle I_{\rm rec}(t)\rangle_T = -I_{\rm out} \quad \text{(1a)}$$

  where $\langle\cdot\rangle_T$ stands for the average value in a period T, and the achievement of ZVS and ZVDS conditions as

$$V_{\rm DS}(t_{\rm SW}^{ON}) = 0,\ V'_{\rm DS}(t_{\rm SW}^{ON}) = 0 \quad \text{(1b)}$$

- find the set of unknowns that ensures both (1a) and (1b).

The solution of the mathematical problem can be numerically found with any mathematical tool, and ensures the optimal class-E operation once the converter works in stationary conditions. In fact, the first two equations in (1a) require that the state of the converter at the end of the period is equal to the initial one, while the last is needed to ensure a constant $V_{\rm out}$:

[1]Indeed, the design procedure in [17] is slightly more complex and introduces a normalization with respect to switching frequency, and output voltage and current. For the sake of simplicity, we do not consider any normalization here.

[2]In [17] it has been shown that, by properly setting the time origin, system evolution in a single period is dependent only on the two initial currents $I_{\rm inv}^0$ and $I_{\rm rec}^0$.

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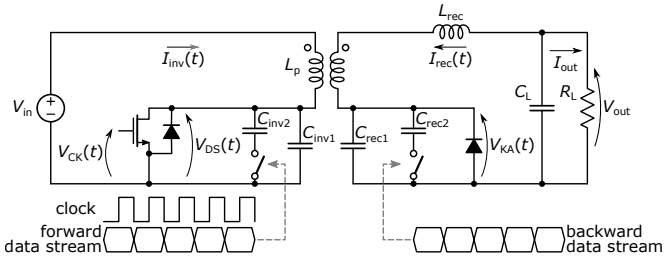


Fig. 3. Schematic of the proposed class-E resonant isolated converter capable of embedded bidirectional communication.

if the average value of $I_{\rm rec}(t)$ is $-I_{\rm out}$, the average current on $C_{\rm L}$ in a clock period is zero, so that only negligible ripple variations on $V_{\rm out}$ are allowed. Finally, (1b) impose that both $V_{\rm DS}(t)$ and its first derivative are zero for $t = t_{\rm SW}^{ON}$.

From a mathematical point of view, this a system of five equations in six unknowns. As a result, one unknown can be used as an additional degree of freedom. A convenient choice is to fix $L_{\rm p}$ according to the available transformer, and exploit the five equations to compute the remaining five quantities. A design example that follows this approach is provided at the beginning of Sec. V.

IV. Proposed Communication Technique

The idea grounding the proposed communication technique relies on the simple observation that changing one circuit parameter at the secondary side of the converter may result in an appreciable (and thus, easily detectable) modification of the waveforms at the primary side. Similarly, changes in voltages and currents at the secondary side occur due to a change in the circuit parameters at the primary side. For example, if one allows $C_{\rm rec}$ to change between two values, two $V_{\rm DS}(t)$ with different shapes are observed.

This intuition can be exploited to introduce backward/forward communication under the assumptions that: i- the introduced changes are *easily* detectable; ii- the converter behavior is still the desired one (at least, on average). The keypoint of this paper is that, by means of the procedure introduced in [17], we can design the circuit in a way that is accurate enough to satisfy both requirements. To ease reception of the transmitted bits, detection of changes in voltage waveforms is the most natural choice. As such, the prime candidates are $V_{\rm DS}(t)$ when considering a backward communication, and $V_{\rm KA}(t)$ for a forward communication.

In the following, with the notation 's'$_b$ we will refer to a symbol or a sequence s transmitted backward, and with 's'$_f$ to a symbol or sequence s transmitted forward. We also refer with $V_{\rm DS}^{\text{`}s\text{'}_b}(t)$ and $V_{\rm DS}^{\text{`}s\text{'}_f}(t)$ to the $V_{\rm DS}(t)$ waveform which one observes when 's'$_b$ and 's'$_f$, respectively, are sent, and use a similar notation for all other quantities.

A. Circuit Description

The circuit we propose is depicted in Fig. 3. With respect to the schematic of Fig. 2(a), there are three differences:

1) A diode is added in parallel to the main MOS switch. We refer to it as the *body diode*, as it could simply be the intrinsic diode of the discrete MOS switch. Note that this was not considered either in [17] or in Fig. 2(a) since a proper design guarantees that it never turns on;
2) Capacitor $C_{\rm inv2}$ is added to the circuit, and an additional MOS (modeled as an ideal switch for the sake of simplicity) is used to connect it in parallel to $C_{\rm inv1}$;
3) Capacitor $C_{\rm rec2}$ is added to the circuit and can be connected in parallel to $C_{\rm rec1}$.

In backward communication mode, $C_{\rm inv2}$ is always connected to the circuit, while $C_{\rm rec1}$ at each clock cycle, is connected to or disconnected from the circuit depending on the bit to be transmitted. We can simply imagine a system as in Fig. 3, where the switch at the rectifier side is directly driven by the backward data stream: the transmission of '1'$_b$ is achieved by connecting $C_{\rm rec2}$, and the transmission of '0'$_b$ by disconnecting it. The data stream is encoded at the same frequency at which the converter is operating. This allows us to transmit data at a rate equal to $1/T$, that is expected to be very high as class-E converter are usually designed to operate at a very high frequency.

Complementary, in forward communication mode, $C_{\rm rec2}$ is always connected to the circuit, while $C_{\rm inv2}$ at each clock cycle, is connected to (transmission of '1'$_f$) or disconnected from (transmission of '0'$_f$) the circuit. Again, the transmitted data rate is $1/T$.

B. Updated converter mathematical model

The effect of introducing the body diode is limited, since it turns on only if $V_{\rm DS}(t)$ reaches the threshold voltage $-V_{\rm B}^{ON}$. In the converter model, we simply consider that turning the diode on is almost equivalent to turning the MOS on, with the only difference that $V_{\rm DS}(t) = -V_{\rm B}^{ON}$ when the diode is on, while $V_{\rm DS}(t) = 0$ if the MOS is on.

Conversely, the introduction of $C_{\rm rec2}$ and $C_{\rm inv2}$ imposes a major change. Let us consider the two time-varying capacitances $C_{\rm rec}(t)$ and $C_{\rm inv}(t)$ defined as the instantaneous value of the capacitance connected to the anode-cathode and source-drain junctions. According to the transmission scheme described above, when communicating backward we have:

$$C_{\rm inv}(t) = C_{\rm inv1} + C_{\rm inv2}$$
$$C_{\rm rec}(t) = \begin{cases} C_{\rm rec1} & \text{when transmitting '0'}_b \\ C_{\rm rec1} + C_{\rm rec2} & \text{when transmitting '1'}_b \end{cases}$$

and when communicating forward we have

$$C_{\rm inv}(t) = \begin{cases} C_{\rm inv1} & \text{when transmitting '0'}_f \\ C_{\rm inv1} + C_{\rm inv2} & \text{when transmitting '1'}_f \end{cases}$$
$$C_{\rm rec}(t) = C_{\rm rec1} + C_{\rm rec2}$$

Let also assume that synchronization in the circuit is such that $C_{\rm rec}(t)$ and $C_{\rm inv}(t)$ can change their values only when the rectifying diode is on, or when the main MOS switch is on, respectively. This assumption allows us to consider, independently of the real switching instant, an equivalent system where $C_{\rm rec}(t)$ and $C_{\rm inv}(t)$ are constant in the whole $t \in [0, T]$, and therefore to use the same expressions for $I_{\rm inv}(t)$, $I_{\rm rec}(t)$, $V_{\rm DS}(t)$ and $V_{\rm KA}(t)$ as in Sec. III-A. In fact, referring to a backward communication (the situation is similar

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for forward communication), we can observe from Fig 2(b) that at the initial time $t = 0$ the rectifying diode is on, and turns off at $t = t_{\rm D}^{OFF}$. At $t = t_{\rm D}^{ON}$ it turns on, and stays on up to $t = T$. If $C_{\rm rec}(t)$ cannot change in $t \in [t_{\rm D}^{OFF}, t_{\rm D}^{ON}]$, and since outside this interval its value has no influence on the circuit (it is shorted by the rectifying diode), the circuit evolution is the same as in the system where $C_{\rm rec}(t)$ is constant in the whole $t \in [0, T]$.

So, without loss of generality, we can consider that both $C_{\rm rec}(t)$ and $C_{\rm inv}(t)$ can change only immediately before $t = 0$, and that the expression found in [17] for voltages and currents can still be used considering that the value of the two capacitances is given by $C_{\rm rec}(0)$ and $C_{\rm inv}(0)$.

C. Main changes in the converter behavior

Enabling communication as schematized in Fig. 3 results in a few important changes in the converter behavior. For the sake of simplicity, we focus in this section on the backward communication only, and consider to transmit a symbol (or a sequence) 's'$_b$. Similar considerations hold when transmitting forward a symbol (or a sequence) 's'$_f$.

The main changes can summarize as follows.

- Let us assume to transmit a bit 's'$_b$ starting from the circuit initial condition $\left\{I_{\rm inv}^{\text{`}s\text{'}_b}(0), I_{\rm rec}^{\text{`}s\text{'}_b}(0)\right\}$. Two different evolutions for $t \in [0, T]$ can be observed according to 's'$_b$: namely, we get $I_{\rm inv}^{\text{`}1\text{'}_b}(t)$, $I_{\rm rec}^{\text{`}1\text{'}_b}(t)$, $V_{\rm DS}^{\text{`}1\text{'}_b}(t)$ and $V_{\rm KA}^{\text{`}1\text{'}_b}(t)$ when sending '1'$_b$. We get $I_{\rm inv}^{\text{`}0\text{'}_b}(t)$, $I_{\rm rec}^{\text{`}0\text{'}_b}(t)$, $V_{\rm DS}^{\text{`}0\text{'}_b}(t)$ and $V_{\rm KA}^{\text{`}0\text{'}_b}(t)$ when '0'$_b$ is transmitted.
- The two different evolutions lead to i) a different performance in terms of ZVS and ZVDS, that clearly cannot be ensured anymore for both cases; ii) two different sets of turn on and off instants for the rectifying diode, that we indicate with $t_{\rm D}^{ON,\text{`}1\text{'}_b}$ and $t_{\rm D}^{OFF,\text{`}1\text{'}_b}$, and with $t_{\rm D}^{ON,\text{`}0\text{'}_b}$ and $t_{\rm D}^{OFF,\text{`}0\text{'}_b}$; iii) two different values of the current delivered to the load, i.e., two different values of $\left\langle I_{\rm rec}^{\text{`}1\text{'}_b}(t)\right\rangle_T$ and $\left\langle I_{\rm rec}^{\text{`}0\text{'}_b}(t)\right\rangle_T$.
- A *stationary condition does not anymore exist*, since the system ends for $t = T$ into two possible states $\left\{I_{\rm inv}^{\text{`}1\text{'}_b}(T), I_{\rm rec}^{\text{`}1\text{'}_b}(T)\right\}$ or $\left\{I_{\rm inv}^{\text{`}0\text{'}_b}(T), I_{\rm rec}^{\text{`}0\text{'}_b}(T)\right\}$, that it is not possible to make identical to the each other.

While additional details will be provided when considering separately the backward and the forward communication, it is here enough to highlight that the above changes have a twofold consequence. On the one hand, (1a) and (1b) cannot be verified at the same time for both for '1'$_b$ and '0'$_b$, so a new design approach is required. On the other hand, it is not anymore convenient to consider the evolution in a single clock period.

To cope with the latter observation, let us extend the approach in [17] to the case of multiple clock periods as follows. Let us refer to a n-period time, in which we are transmitting the sequence 's'$_b$ starting from an initial condition $\left\{I_{\rm inv}^{\text{`}s\text{'}_b}(0), I_{\rm rec}^{\text{`}s\text{'}_b}(0)\right\}$. For $t \in [0, T]$ one can compute the evolution of the converter assuming that the values of two resonant capacitance are $C_{\rm rec}(0)$ and $C_{\rm inv}(0)$. Hence, the state of the system for $t = T$ can be used as initial condition for computing the evolution of the converter for $t \in [T, 2T]$ along with the values of $C_{\rm inv}(T)$ and $C_{\rm rec}(T)$. The state at $t = 2T$ is then used as initial condition for the third time period $t \in [2T, 3T]$ along with the values of $C_{\rm inv}(2T)$ and $C_{\rm rec}(2T)$, and so on.

In this way one can easily construct step-by-step the waveforms $I_{\rm inv}^{\text{`}s\text{'}_b}(t)$, $I_{\rm rec}^{\text{`}s\text{'}_b}(t)$, $V_{\rm DS}^{\text{`}s\text{'}_b}(t)$ and $V_{\rm KA}^{\text{`}s\text{'}_b}(t)$ for $t \in [0, nT]$. Of course, these waveforms depend on the sequence 's'$_b$. As an example, for $n = 2$, up to four different evolutions, with final states $\left\{I_{\rm inv}^{\text{`}11\text{'}_b}(2T), I_{\rm rec}^{\text{`}11\text{'}_b}(2T)\right\}$, $\left\{I_{\rm inv}^{\text{`}10\text{'}_b}(2T), I_{\rm rec}^{\text{`}10\text{'}_b}(2T)\right\}$, $\left\{I_{\rm inv}^{\text{`}01\text{'}_b}(2T), I_{\rm rec}^{\text{`}01\text{'}_b}(2T)\right\}$, or $\left\{I_{\rm inv}^{\text{`}00\text{'}_b}(2T), I_{\rm rec}^{\text{`}00\text{'}_b}(2T)\right\}$ can be observed. For a generic value of n, there may be 2^n different evolutions, with 2^n final states, and 2^n different values of $\langle I_{\rm rec}(t)\rangle_T$.

In conclusion, while communicating, many issues have to be considered. Two of them are related to the sequence 's'$_b$:

1) the converter is wandering through a succession of different states $\left\{I_{\rm inv}^{\text{`}s\text{'}_b}(kT), I_{\rm rec}^{\text{`}s\text{'}_b}(kT)\right\}$, $k = 1 \ldots n$, that depend on all previously transmitted symbols, possibly without any periodicity. In strict sense, there is a *memory effect* in the circuit evolution. Even if it is reasonable to consider that this effect is limited (e.g., to a certain number of previous symbols), taking it into account is fundamental in the design of the system;
2) the current delivered to the load depends weakly on the converter state and strongly on the transmitted symbol. In other words, the effect of the transmitted symbol is stronger with respect to the memory effect. This will be clarified in the following.

To cope with the two above issues, it is necessary that the transmitted sequence has the following properties:

1) symbols '1' and '0' are required to be balanced, to allow the converter to work in a sort of *metastable* state that is intermediate between all different states $\left\{I_{\rm inv}^{\text{`}s\text{'}_b}(kT), I_{\rm rec}^{\text{`}s\text{'}_b}(kT)\right\}$. Long sequences of '1' and '0' cannot be transmitted to avoid that the converter state moves away from this metastable point;
2) symbols '1' and '0' are required to be equiprobable, in order to set to output current to an intermediate value between that delivered when sending '1'$_b$ and when sending '0'$_b$, making it in this way almost independent of 's'$_b$.

Note that the same requirements apply to almost any asynchronous communication scheme, and many coding techniques have been developed so far to solve these issues [18].

In the following, some details on the backward and the forward communication will be provided, while the complete design approach will be introduced in Sec. V.

D. Backward Communication

Let us consider a reference value $C_{\rm rec0}$ for $C_{\rm rec}$ as that used to generate the waveforms of Fig. 2(b). We aim at designing a system where $C_{\rm rec1}$ and $C_{\rm rec2}$ are such that $C_{\rm rec}(t)$ is increased to $C_{\rm rec1} + C_{\rm rec2} > C_{\rm rec0}$ when transmitting a '1'$_b$, thus resulting in a slower response. Conversely, $C_{\rm rec}(t)$ is

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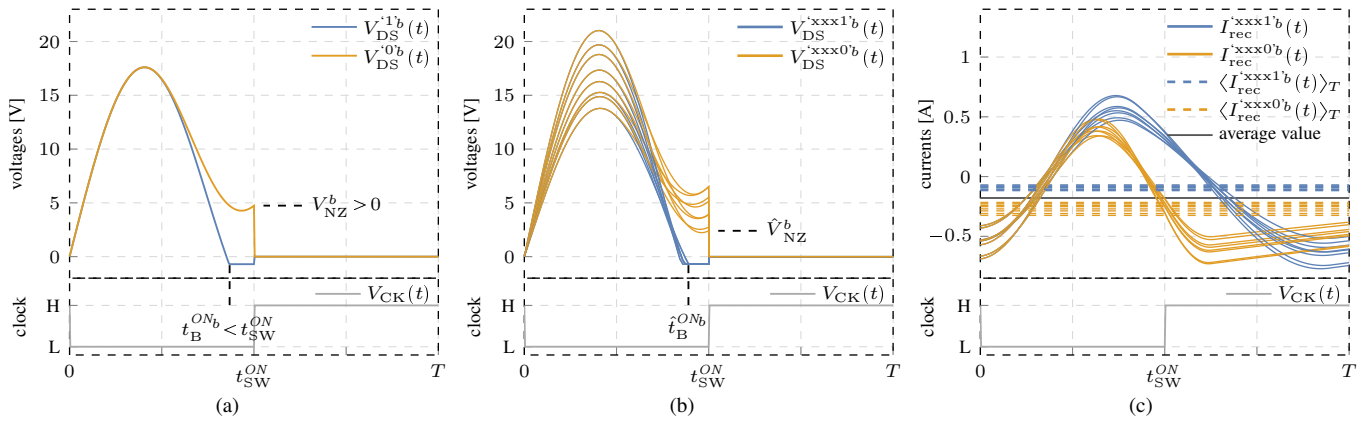


Fig. 4. (a): Intuitive working principle of the backward communication: $V_{\rm DS}^{`0'_b}(t)$ is always positive with $V_{\rm DS}^{`0'_b}(t_{\rm SW}^{ON}) = V_{\rm NZ}^b > 0$, while $V_{\rm DS}^{`1'_b}(t)$ turns the body diode on at the time $t_{\rm B}^{ON_b} < t_{\rm SW}^{ON}$. (b): The two different groups of $V_{\rm DS}(t)$ in a realistic situation where memory effect has been considered. Such a system must be characterized by its worst-case conditions given by the latest body diode turn on time $\hat{t}_{\rm B}^{ON_b}$ and by the lowest value $\hat{V}_{\rm NZ}^b$ reached by $V_{\rm DS}(t_{\rm SW}^{ON})$. (c): The two different groups of $I_{\rm rec}(t)$ (solid lines) along with their mean value (dotted lines) in a realistic situation where memory effect has been considered. The solid dark line is the average value of the mean values.

lowered to $C_{\rm rec1} < C_{\rm rec0}$ when transmitting a '0'$_b$, with a faster response.

This has effects both on $V_{\rm DS}(t)$ and on $V_{\rm KA}(t)$. We are not interested in the latter, even if easily detectable (in particular by means of a difference between the $t_{\rm D}^{ON,`1'_b}$ and the $t_{\rm D}^{ON,`0'_b}$), since in a backward communication we need to find evidences of the transmitted symbol at the primary side. The effect on $V_{\rm DS}(t)$ is intuitively explained in Fig. 4(a). In the system designed to have a slower response, $V_{\rm DS}^{`1'_b}(t)$ reaches a negative level and turns the body diode on at $t = t_{\rm B}^{ON_b} < t_{\rm SW}^{ON}$. In the system with a faster response, $V_{\rm DS}^{`0'_b}(t)$ is always positive, with $V_{\rm DS}^{`0'_b}(t_{\rm SW}^{ON}) = V_{\rm NZ}^b > 0$. Accordingly, the transmission of '1'$_b$ or '0'$_b$ can be identified by a simple level crossing detection circuit at the $V_{\rm DS}(t)$ node.

The drawback is that ZVS/ZVDS as defined by (1b) are no longer reached for none of the two configurations corresponding to the transmission of '1'$_b$ or '0'$_b$[3]. This is tolerable assuming that both $V_{\rm B}^{ON}$ and $V_{\rm NZ}^b$ are small, so that the converter enjoys *quasi-ZVS* condition.

A more realistic situation that keeps into account also the memory effect is considered in Fig. 4(b). Starting from the same initial condition, we have considered a system transmitting all $2^4 = 16$ possible sequences 's'$_b$ composed of 4 bits. The plot shows $V_{\rm DS}(t)$ observed in the last clock period. All waveforms can be easily divided into two *groups*. The first one is composed of the $V_{\rm DS}(t)$ associated to all sequences ending with symbol 1. We refer to this group as $V_{\rm DS}^{`xxx1'_b}(t)$. The second group is associated to sequences ending with symbol 0, referred to as $V_{\rm DS}^{`xxx0'_b}(t)$. The two groups are easily distinguishable, thus showing that the transmitted bit can be identified despite the memory effect. The only difference with respect to the simple case of Fig. 4(a) is that the detectability conditions should be set according to the *worst-case*. To this aim, let us define $\hat{t}_{\rm B}^{ON_b}$ as the *latest time* for which all possible $V_{\rm DS}^{`xxx1'_b}(t)$ turn the body diode on, and $\hat{V}_{\rm NZ}^b$ the *lowest value* of all possible $V_{\rm DS}^{`xxx0'_b}(t_{\rm SW}^{ON})$, as indicated in Fig. 4(b). Being able to set an upper bound on $\hat{t}_{\rm B}^{ON_b}$ and a lower bound on $\hat{V}_{\rm NZ}^b$ is equivalent to set the detectability condition for backward communication.

Finally, in Fig. 4(c) we have plotted the two groups of signals $I_{\rm rec}^{`xxx1'_b}(t)$ and $I_{\rm rec}^{`xxx0'_b}(t)$ (solid lines), along with their mean value $\langle I_{\rm rec}(t)\rangle_T$ in the period (dashed lines). Each waveform has a different mean value, with small differences among curves belonging to the same group, and large differences between curves belonging to different groups. The average value of all current mean values over a period has also been plotted as a solid, dark line. It is clear from the figure that the output current, that is given by the average value of $I_{\rm rec}(t)$, is strongly dependent on the currently transmitted symbol, and weakly on previous symbols (i.e., due to the memory effect of the system).

E. Forward Communication

Similarly to the previous case, while forward transmitting a sequence 's'$_f$, consequences on all waveforms can be observed, and thus on ZVS and ZVDS performance, output current value, and rectifying diode turn on and off instants.

In this setting, we need to ensure (at least) quasi-ZVS at the primary side, and to find a measurable evidence of the transmitted symbol at the secondary side. The difference between the (slower) group of signals $V_{\rm KA}^{`xxx1'_f}(t)$ and the (faster) group of waveforms $V_{\rm KA}^{`xxx0'_f}(t)$ characterizing the forward communication in a setting similar to that considered in the previous case (i.e., all 16 possible sequences 's'$_f$ composed of 4 bits are considered starting from the same initial condition to highlight the memory effect) can be observed in Fig. 5(a). All $V_{\rm KA}^{`xxx1'_f}(t)$ present a non-negligible phase lag with respect to any $V_{\rm KA}^{`xxx0'_f}(t)$. Let us focus on $t_{\rm D}^{ON}$ defined as the time instant when the rectifying diode turns on (i.e., $V_{\rm KA}(t)$ reaches $-V_{\rm D}^{ON}$). The observed values of $t_{\rm D}^{ON}$ for all $V_{\rm KA}^{`xxx1'_f}(t)$ are very similar to the average value $\bar{t}_{\rm D}^{ON,`1'_f}$, and

[3]Theoretically, the communication mechanism can be designed in a way that one of the two waveforms of Fig. 4(a) features perfect ZVS/ZVDS. It will be clear when considering the memory effect why this is not useful from a practical point of view.

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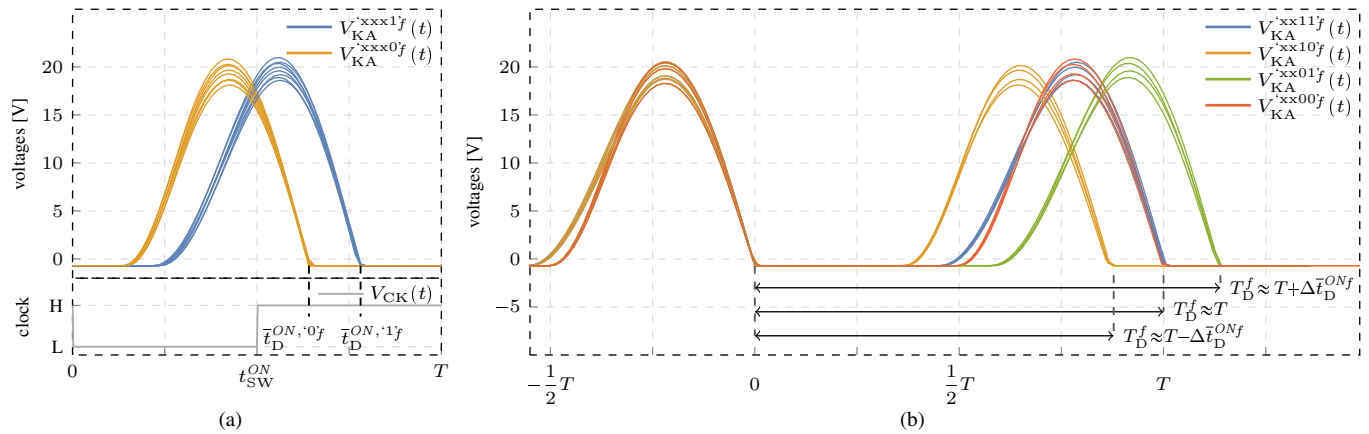


Fig. 5. (a): Some examples of $V_{\mathrm{KA}}^{\text{`xxx1'}_f}(t)$ and of $V_{\mathrm{KA}}^{\text{`xxx0'}_f}(t)$ in a realistic forward communication situation, where memory effect is taken into account. The former group present a rectifying turn on diode almost constant and approximately equal to $\bar{t}_{\mathrm{D}}^{ON,\text{`1'}_f}$, while the latter approximately equal to $\bar{t}_{\mathrm{D}}^{ON,\text{`0'}_f}$. (b): By looking at the time T_{D}^f between two consecutive rectifying diode turn on time instants it is possible to easily determine if the transmitted symbol is equal or different with respect to the former one.

can be approximated with it. Similarly, we can approximate the t_{D}^{ON} for all $V_{\mathrm{KA}}^{\text{`xxx0'}_f}(t)$ with $\bar{t}_{\mathrm{D}}^{ON\text{`0'}_f}$.

Even if the difference $\Delta\bar{t}_{\mathrm{D}}^{ONf} = \bar{t}_{\mathrm{D}}^{ON,\text{`1'}_f} - \bar{t}_{\mathrm{D}}^{ON,\text{`0'}_f}$ is large, the direct measure of t_{D}^{ON}, i.e., of the phase of $V_{\mathrm{KA}}(t)$, is not a good sensing strategy, mainly due to a lack of a reference time instant[4].

A solution is to adopt a *differential* sensing strategy. To do so, let us define T_{D}^f as the time between two consecutive rectifying diode turn on instants. Assuming that two '1'$_f$ are transmitted, the first instant when the diode turn on is approximately $\bar{t}_{\mathrm{D}}^{ON,\text{`1'}_f}$, while the second one is approximately $T + \bar{t}_{\mathrm{D}}^{ON,\text{`1'}_f}$, with $T_{\mathrm{D}}^f \approx T$. Conversely, transmitting '1'$_f$ as the first symbol, and '0'$_f$ as the second one, leads to two turn on instants approximately equal to $\bar{t}_{\mathrm{D}}^{ON,\text{`1'}_f}$ and $T + \bar{t}_{\mathrm{D}}^{ON,\text{`0'}_f}$, with $T_{\mathrm{D}}^f \approx T - \Delta\bar{t}_{\mathrm{D}}^{ONf}$. When considering all possible combinations, we have

$$T_{\mathrm{D}}^f \approx \begin{cases} T & \text{when sending sequence '11'}_f \\ T - \Delta\bar{t}_{\mathrm{D}}^{ONf} & \text{when sending sequence '10'}_f \\ T + \Delta\bar{t}_{\mathrm{D}}^{ONf} & \text{when sending sequence '01'}_f \\ T & \text{when sending sequence '00'}_f \end{cases}$$

An example is depicted in Fig. 5(b), showing the T_{D}^f for waveforms in a system transmitting all $2^4 = 16$ possible sequences 's'$_f$ composed of 4 bits.

In conclusion, when T_{D}^f is similar to T, then the transmitted symbol is the same as the previous one. When instead T_{D}^f is either shorter or longer enough with respect to T, the transmitted symbol has changed with respect to the previous one. The detectability of this approach is ensured if we are able to set a lower bound on $\Delta\bar{t}_{\mathrm{D}}^{ONf}$.

Even if not shown here, the situation for $I_{\mathrm{rec}}(t)$ is very similar to that depicted in Fig. 4(c), with small differences among curves where the last transmitted symbol is the same, and large differences between curves where the last transmitted symbol is different.

[4]Note, in fact, that the clock $V_{\mathrm{CK}}(t)$ (and so, the zero reference time for the period) is not available at the secondary side, and recovering it may be complicated.

F. Bidirectional Communication

A half-duplex bidirectional communication system can be easily obtained by merging the two design procedures for backward and forward communication. In particular, one should consider all detectability requirements coming both from the backward communication (such as an upper bound for $\hat{t}_{\mathrm{B}}^{ON_b}$ and a lower bound for $\hat{V}_{\mathrm{NZ}}^{b}$) and from the forward communication (lower bound for $\Delta\bar{t}_{\mathrm{D}}^{ONf}$).

V. Design Example

As a proof-of-concept of the methodology discussed in the previous section, we consider the design of a 5 V-to-5 V class-E isolated converter ($V_{\mathrm{in}} = 5\,\mathrm{V}$, $V_{\mathrm{out}} = 5\,\mathrm{V}$) with bidirectional communication capabilities and an output power $P_{\mathrm{out}} = 1.2\,\mathrm{W}$. The resonant converter is designed to operate at a 1 MHz frequency, with a data rate of 1 Mbit/s.

To ease the selection of passive components, we fix $L_{\mathrm{p}} = 8.5\,\mu\mathrm{H}$ since this is the inductance at the primary side of a commercial *WE-FLEX* transformer by Würth Elektronik. In a $1:1$ turns ratio configuration, this transformer has a coupling coefficient ≈ 0.98 and quality factor ≈ 45. We also consider *Murata* wire-wound chip inductors whose quality factor (in the µH range and around 1 MHz frequency) is ≈ 50, and we assume ideal capacitors[5]. Furthermore, we use a IRLML0030TR N-MOS transistor by International Rectifier as main MOS switch. It has an on-resistance $\approx 0.04\,\Omega$ and a body diode forward voltage $V_B^{\mathrm{ON}} \approx 0.7\,\mathrm{V}$. The rectifying diode is a ES1B by Vishay, with $V_D^{\mathrm{ON}} \approx 0.7\,\mathrm{V}$ and a on-resistance $\approx 0.3\,\Omega$.

A. Design of the canonical converter

Given the above specifications, and according to the procedure described in Sec. III-A, the design of a canonical class-E converter (i.e., without communication capability) is achieved by considering the associated mathematical problem where

[5]Ceramic capacitors with C0G dielectric ensure extremely high performance (quality factor > 1000) so that they can be assumed ideal.

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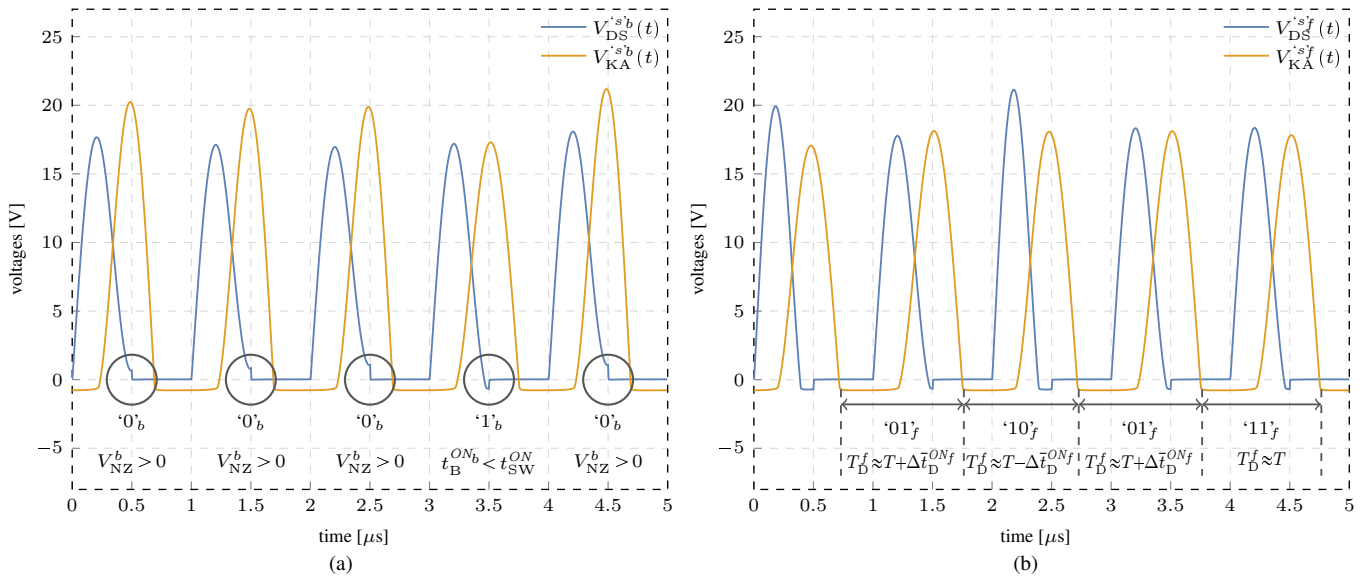


Fig. 6. Results of a SPICE simulation of the proposed class-E resonant converter with embedded communication capabilities, showing both $V_{\rm DS}(t)$ and $V_{\rm KA}(t)$ in backward and forward communication mode. In both cases, the transmitted sequence is the periodic repetition of (4). (a): Chunk (5 µs) of backward communication featuring '00010'$_b$; and (b): chunk (5 µs) of forward communication featuring '01011'$_f$, and generating $T_{\rm D}^f\approx\{T+\Delta\bar{t}_{\rm D}^{ON_f},T-\Delta\bar{t}_{\rm D}^{ON_f},T+\Delta\bar{t}_{\rm D}^{ON_f},T\}$.

(1a) and (1b) are the five equations to be solved, and $I_{\rm inv}^0$, $I_{\rm rec}^0$, $L_{\rm rec}$, $C_{\rm inv}$ and $C_{\rm rec}$ the five unknown variables. The solution is given by $L_{\rm rec}=3.3\,\mu$H, $C_{\rm inv}=6.3\,$nF and $C_{\rm rec}=5.3\,$nF. Waveforms of Fig. 2(b) correspond to this design.

B. Design of the converter with communication capability

The design we propose to enable communication capability in a converter with the specifications reported at the beginning of the section is $L_{\rm rec}=3.3\,\mu$H (identical to the canonical converter of the previous subsection), $C_{\rm inv1}=4.7\,$nF, $C_{\rm inv2}=1.3\,$nF, $C_{\rm rec1}=4.4\,$nF, and $C_{\rm rec2}=1.6\,$nF. A spice simulation of this design showing $V_{\rm DS}(t)$ and $V_{\rm KA}(t)$ both in the case of backward and forward communication and relying on a realistic model for the MOS and the rectifying diode is shown in Fig. 6. Note that $V_{\rm DS}(t)$, in backward communication mode, always features quasi-ZVS as in Sec. IV-D. In forward communication mode, being $C_{\rm rec}=C_{\rm rec1}+C_{\rm rec2}$, $V_{\rm DS}(t)$ always reaches a negative level and turns on the body diode, thus featuring quasi-ZVS also in this case.

This design was obtained as the solution of a properly modified version of the mathematical problem of Sec. III-A as described in the following.

According to Sec. IV-C, since a stationary condition is not existing anymore, the only possibility we have to is to rely the circuit design on the converter *average* behavior.

In detail, let us first focus on backward communication, and consider the system transmitting the n-length sequence 's'$_b$ starting from the initial condition $\left\{I_{\rm inv}^{`s'_b}(0),I_{\rm rec}^{`s'_b}(0)\right\}$, with n long enough. Let also assume that this sequence is characteristic of any other possible realistic sequence of any length, i.e., that it has the same statistical features of any possible sequence to be transmitted. Hence, we can base the design of the converter on 's'$_b$.

In other words, we are considering that the system is transmitting 's'$_b$ in a *ciclostationary* condition, so that we can replace (1a) with

$$I_{\rm inv}^{`s'_b}(nT)=I_{\rm inv}^{`s'_b}(0),\ I_{\rm rec}^{`s'_b}(nT)=I_{\rm rec}^{`s'_b}(0),\ \left\langle I_{\rm rec}^{`s'_b}(t)\right\rangle_{nT}=-I_{\rm out} \tag{2}$$

The first two equations in (2) impose that the initial state of the system has to be the same after the transmission of sequence 's'$_b$, whereas the last one ensures that the zero-average current condition on $C_{\rm L}$ is verified only after the transmission of all n symbols of 's'$_b$.

In forward communication mode we can proceed in the same way. In this case we are assuming that the system initial condition is given by $\left\{I_{\rm inv}^{`s'_f}(0),I_{\rm rec}^{`s'_f}(0)\right\}$, and that we have a sequence 's'$_f$ that is characteristic for any possible real sequence. The ciclostationary condition is expressed as

$$I_{\rm inv}^{`s'_f}(nT)=I_{\rm inv}^{`s'_f}(0),\ I_{\rm rec}^{`s'_f}(nT)=I_{\rm rec}^{`s'_f}(0),\ \left\langle I_{\rm rec}^{`s'_f}(t)\right\rangle_{nT}=-I_{\rm out} \tag{3}$$

A good candidate for 's'$_b$ and 's'$_f$ to be representative for all realistic sequences is

$$\text{'11010100001001011001111100011101'} \tag{4}$$

A first argument supporting this statement is as follows. An additional argument will be mentioned in Section V-C.

Sequence (4) is coming from the Fibonacci implementation of the maximum-length linear-feedback shift register (LSFR) of width $\ell=5$, and whose length is $n=2^\ell-1=31$ bits. The periodic repetition of a sequence from a maximum-length LFSR has two interesting properties: *i*) '0' and '1' are (almost) balanced[6]; and *ii*) all different sub-sequences of length ℓ (excluding one, in this case '00000') can be found.

[6]Being $n=2^\ell-1$ an odd number, a perfect balancing is not possible for any value of ℓ.

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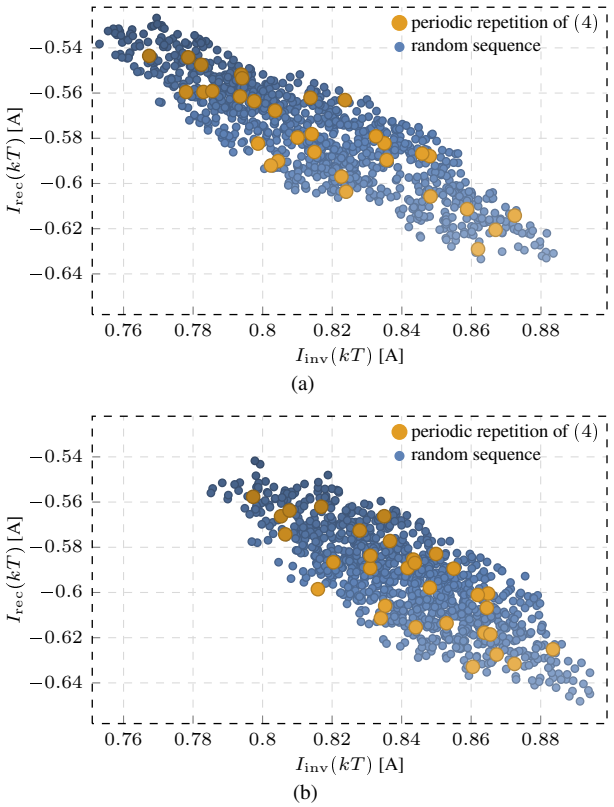


Fig. 7. Comparison between the $n = 31$ circuit states $\{I_{\rm inv}(kT), I_{\rm rec}(kT)\}$, $k = 0 \ldots, n-1$ characterizing the circuit behavior when transmitting the periodic repetition of (4) (large, orange dots), and the $n = 1000$ achieved by a random sequence (small, blue dots). (a): Backward communication; and (b): forward communication.

In conclusion, using the proposed sequence allows an easy and fast way to (almost) exhaustively investigate the response of the system to any sequence of length $\ell = 5$ which is important since, experimentally, the memory effect is negligible after this length. Furthermore, being this sequence balanced, the output power generated by the converter can be considered representative for any balanced sequences.

Once 's'$_b$ and 's'$_f$ are chosen, it is possible to compute in an analytic way the evolution of the system (i.e., to get analytic expressions for $V_{\rm DS}(t)$, $V_{\rm KA}(t)$, $I_{\rm inv}(t)$ and $I_{\rm rec}(t)$) and to use it for translating the design of the converter operating in a ciclostationary condition in a way similar to that considered for the design of standard converter. From a mathematical point of view, the design problem described so far has ten unknowns, i.e.:

$$I_{\rm inv}^{\text{`}s\text{'}_b}(0),\ I_{\rm rec}^{\text{`}s\text{'}_b}(0),\ I_{\rm inv}^{\text{`}s\text{'}_f}(0),\ I_{\rm rec}^{\text{`}s\text{'}_f}(0),$$
$$L_{\rm p},\ L_{\rm rec},\ C_{\rm inv1},\ C_{\rm inv2},\ C_{\rm rec1},\ C_{\rm rec2}.$$

In terms of equations, three are given by (2) to ensure the ciclostationary condition for backward communication, three by (3) to ensure the ciclostationary condition for forward communication, and other three by the *worst-case* detectability conditions, that we set to

$$\hat{V}_{\rm NZ}^{b} = 0.7\,{\rm V}, \quad t_{\rm SW}^{ON} - \hat{t}_{\rm B}^{ON_b} = 25\,{\rm ns}, \quad \Delta\bar{t}_{\rm D}^{ON_f} = 30\,{\rm ns} \quad (5)$$

which results to nine equations overall.

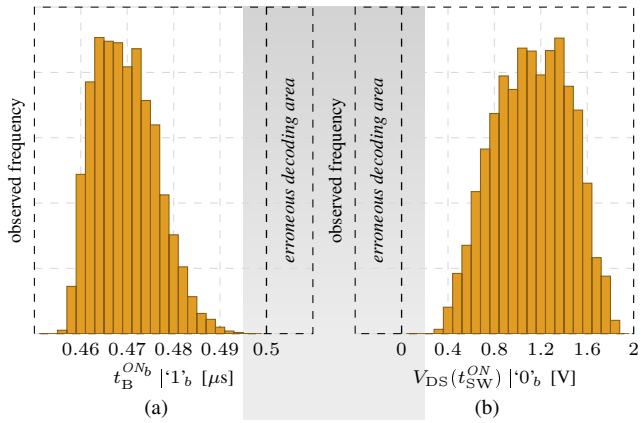


Fig. 8. Observed frequencies of detectability quantities in backward communication mode. (a): $t_{\rm B}^{ON_b}$ while transmitting '1'$_b$; and (b): $V_{\rm DS}(t_{\rm SW}^{ON})$ while transmitting '0'$_b$. The shaded areas indicate the thresholds for an erroneous decoding.

As in the canonical design, there is therefore a degree of freedom, that can we conveniently use to set $L_{\rm p}$. The design proposed at the beginning of this subsection corresponds to the set of parameters satisfying all mentioned constraints.

C. Verification of the proposed design

In addition to the argument given above, we can now verify the assumption that the behavior when transmitting the periodic repetition of sequence (4) is effectively representative for more complex and realistic cases. To do so, we consider here two approaches.

The results of the first approach are shown in Fig. 7, where the two scatter plots represent, separately for the backward (top plot) and forward (bottom plot) communication, the comparison between: i) the $n = 31$ circuit states $\{I_{\rm inv}(kT), I_{\rm rec}(kT)\}$, $k = 0 \ldots, n-1$ that characterize the circuit behavior when transmitting the periodic repetition of (4) (large, orange dots); and ii) the $n = 1000$ states that have been observed when transmitting a random non-periodic sequence (small, blue dots).

Both sets of points roughly identify the same area, showing that even when considering a more complex sequence the state of the converter does not leave the area identified by using (4). This allows us to expect, in a realistic situation, detectability conditions well approximated by that in (5), and confirms the validity of the approximated design procedure.

As a second approach, we recall that, in backward communication, an error is generated if the body diode turns on when sending '1'$_b$, or if the body diode does not turn on when sending '0'$_b$. In Fig. 8 we have plotted the frequencies of the $t_{\rm B}^{ON_b}$ and of the $V_{\rm DS}(t_{\rm SW}^{ON})$ observed in a very long (about 80×10^3 clock periods) simulation of the developed model when transmitting '1'$_b$ and '0'$_b$, respectively. Even if it is hard to use these distributions to extrapolate a value for the bit error rate (BER), it is clear that frequencies are very rapidly decreasing to zero when approaching the two thresholds that, once reached, will generate an error (the shaded area in the plots). In other words, given the rapid decay of the distribution to zero before the error threshold, it is reasonable to assume

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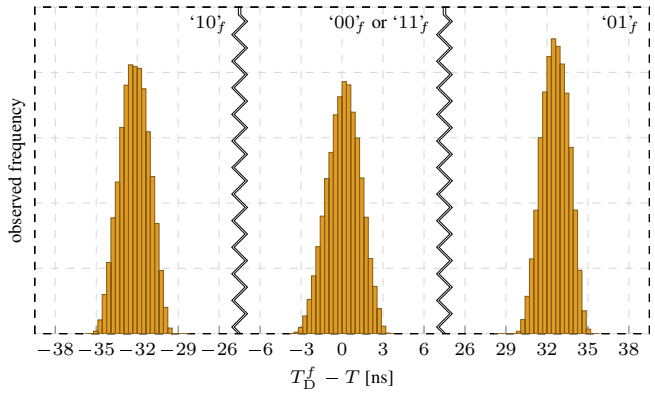


Fig. 9. Observed frequencies of $T_D^f - T$ in forward communication mode according to transmitted bits. The time axis is not in scale to allow the three distributions to be clearly visible.

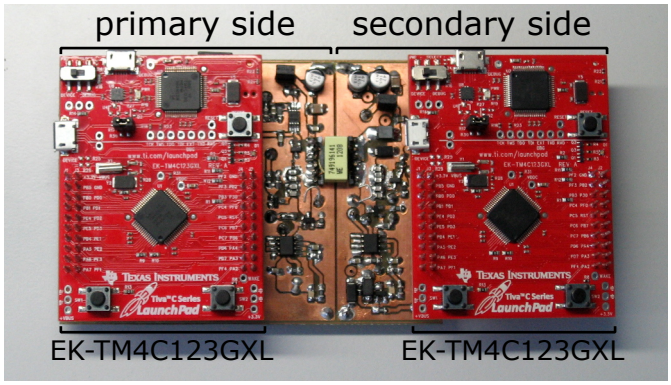


Fig. 10. Prototype photograph, clearly showing the isolation transformer and the two EK-TM4C123GXL boards.

that the system will have a very low BER, which is consistent with the fact that no error occurred in the simulation.

Conversely, in forward communication mode, the T_D^f has the three expected values T, $T - \Delta\bar{t}_D^{ON_f}$ and $T + \Delta\bar{t}_D^{ON_f}$. A possible solution to identify to what category the T_D^f belongs to is to compare it with the two thresholds $T \pm \Delta\bar{t}_D^{ON_f}/2$.

In Fig. 9 we have plotted the frequencies of the T_D^f observed when the last transmitted symbols are '10'$_f$ (expected value $T - \Delta\bar{t}_D^{ON_f}$), are '11'$_f$ or '00'$_f$ (expected value T), or are '01'$_f$ (expected value $T - \Delta\bar{t}_D^{ON_f}$).

These distributions are pretty far from the each other (the time axis in Fig. 9 is not in scale to allow the three distributions to be visible), suggesting once again a negligible error probability.

VI. Prototype and Experimental Results

A prototype of the class-E converter described in Sec. V has been fabricated and tested. Fig. 10 shows the photograph of our circuit while connected to the two (clearly visible in the figure) EK-TM4C123GXL evaluation boards, one at the primary side and the other at the secondary side of the transformer, and used to generate all time reference signals and to control the communication. Each of these boards, developed by Texas Instruments [31], embeds a low-power low-cost ARM Cortex-M4F TM4C123GH6PMI microcontroller. The

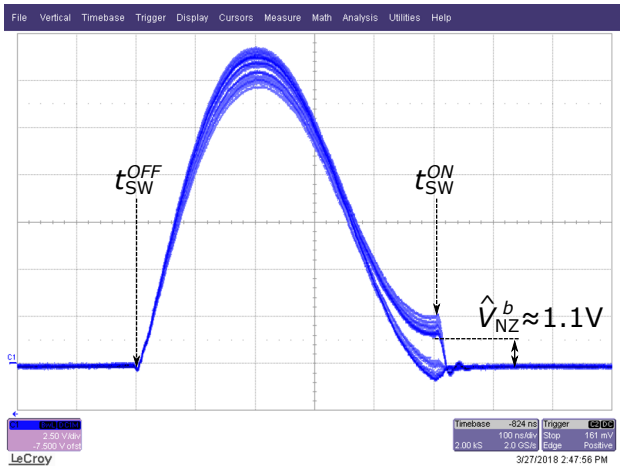


Fig. 11. Eye-diagram of the $V_{DS}(t)$ in backward communication mode.

main clock signal generated by the ARM microcontroller is fed into a Texas Instruments LM5112 gate driver, whose output is connected to the IRLML0030TR N-MOS transistor. The additional capacitors C_{inv2} and C_{rec2} are connected to two small 2N7002 N-MOS switches, that are driven directly by an output pin of the ARM device.

The prototype features two additional isolated communication channels using optocouplers, used to generate reliable communication channels for bit error-rate computation purposes. The prototype also includes a simple sensing circuitry to detect the transmitted bit both at the primary and secondary side, as described in the following.

A. Backward communication

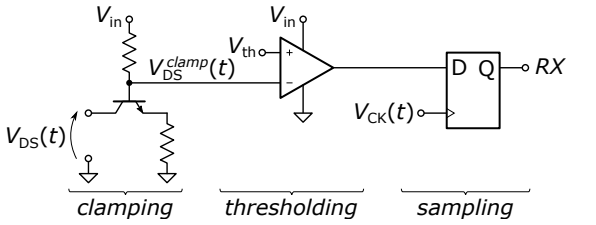
The eye-diagram of $V_{DS}(t)$ measured while backward transmitting a pseudo-random stream is shown in Fig 11. From the figure, it is possible to see that the achieved detectability conditions approximately match that imposed by (5).

The circuit used for detecting the transmitted bit is schematized in Fig. 12(a). The $V_{DS}(t)$ (ranging from $-V_B^{ON} \approx -0.7\,V$ to about $15\,V$) is first processed by a clamping circuit with a twofold purpose: *i*) when $V_{DS}(t) > V_{in}$, the BJT is in forward active region, with $V_{DS}^{clamp}(t) \approx V_{in}$; *ii*) when $V_{DS}(t) < V_{in}$ the base-collector junction of the BJT is forward biased, with $V_{DS}^{clamp}(t) \approx V_{DS}(t) + V_{BC}^{ON}$. This allows $V_{DS}^{clamp}(t)$ to be in a suitable range (approximately $V_{DS}^{clamp}(t) \in [0, V_{in}]$) for being safely input to an analog comparator, and to be compared with a threshold voltage V_{th}. The output of the comparator is then triggered at the rising edge of $V_{CK}(t)$ by a standard flip-flop, whose output is the recovered transmitted symbol.

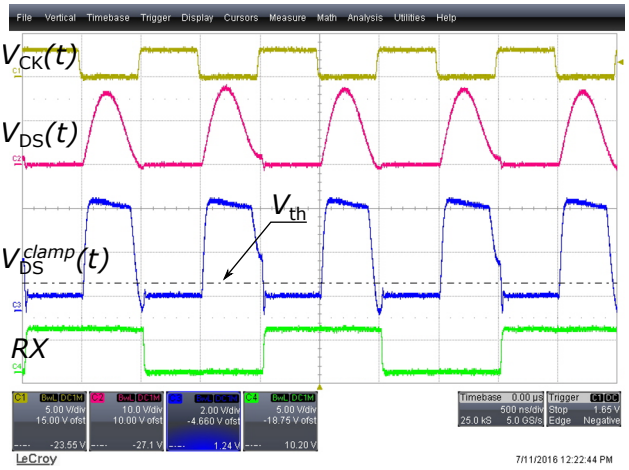
An example of the detection process can be observed in Fig. 12(b). The figure shows, from top to bottom, $V_{CK}(t)$, $V_{DS}(t)$, $V_{DS}^{clamp}(t)$, and the recovered symbol. The figure also shows V_{th} as the dashed-dotted cursor line. In order to allow a correct recovery, it should be $V_{BC}^{ON} - V_B^{ON} < V_{th} < V_{BC}^{ON} + \hat{V}_{NZ}^b$. In the prototype, we set $V_{th} \approx 1.2\,V$. With this value, a correct recovery has been always ensured, and no transmission errors have been recorded in several hours of circuit testing.

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(a)



(b)

Fig. 12. (a): Circuit used at the primary side of the converter for detecting the transmitted symbol in backward communication mode. (b): Example of recovering the transmitted symbol. From top to bottom: $V_{\mathrm{CK}}(t)$, $V_{\mathrm{DS}}(t)$, $V_{\mathrm{DS}}^{clamp}(t)$ along with V_{th}, and finally the recovered symbol (high level is '1'$_b$, low level is '0'$_b$).

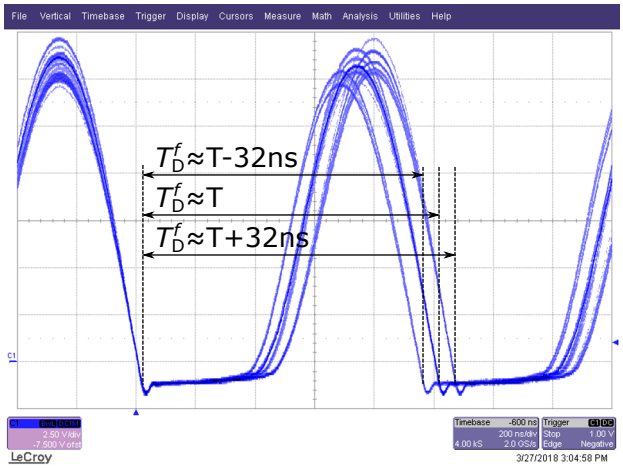
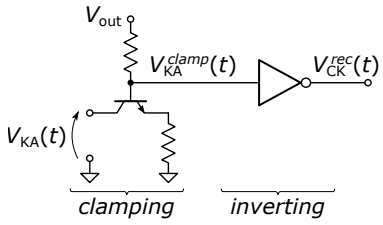


Fig. 13. Eye-diagram of the $V_{\mathrm{KA}}(t)$ in forward communication mode.

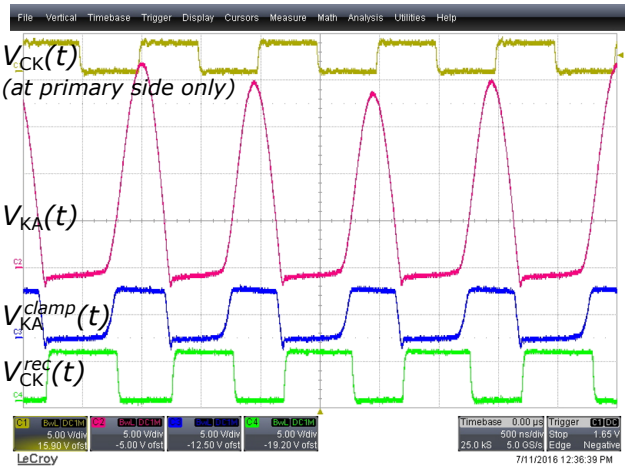
B. Forward communication

The eye-diagram of $V_{\mathrm{KA}}(t)$ measured while forward transmitting a pseudo-random stream is shown in Fig 13. According to the figure, the obtained $\Delta\bar{t}_{\mathrm{D}}^{ON_f}$ well matches the one imposed by (5).

The circuit used at the secondary side of the converter to generate the recovered clock signal $V_{\mathrm{CK}}^{rec}(t)$ is schematized in Fig. 14(a). The $V_{\mathrm{KA}}(t)$ is first processed by a clamping circuit similar to that in Fig. 12(a), to get a signal $V_{\mathrm{KA}}^{clamp}(t)$ that is approximately in the range $[0, V_{\mathrm{out}}]$. The signal is then squared



(a)



(b)

Fig. 14. (a): Circuit used at the secondary side of the converter for recovering the system clock. (b): Example of clock recovering at the secondary side of the converter. From top to bottom: $V_{\mathrm{CK}}(t)$ (available only at the primary side), $V_{\mathrm{KA}}(t)$, $V_{\mathrm{KA}}^{clamp}(t)$, and finally the recovered clock $V_{\mathrm{CK}}^{rec}(t)$.

off by a digital inverter to get $V_{\mathrm{CK}}^{rec}(t)$.

The purpose of the recovered clock is twofold: i) it is used as reference timing signal for synchronizing symbols transmission/reception at the secondary side[7] (where $V_{\mathrm{CK}}(t)$ is not available); ii) it is used to measure the T_{D}^f as the time between two rising edges of $V_{\mathrm{CK}}^{rec}(t)$ in forward communication mode.

An example of the clock recovering process is depicted in Fig. 14(b). In the figure, from top to bottom, we show $V_{\mathrm{CK}}(t)$ (available only at the primary side), $V_{\mathrm{KA}}(t)$, $V_{\mathrm{KA}}^{clamp}(t)$, and the recovered clock $V_{\mathrm{CK}}^{rec}(t)$. The time between two rising edges of the recovered clock is the T_{D}^f according to its definition in Sec. IV-E.

Due to hardware limitations of the timing peripherals embedded into the ARM processor of the EK-TM4C123GXL boards, we rely on the detection of forward transmitted symbols to a simple asynchronous circuit whose working principle is illustrated in Fig. 15. Two delay circuits, with delays τ_1 and τ_2 and such that $T - \Delta\bar{t}_{\mathrm{D}}^{ON_f} < \tau_1 < T < \tau_2 < T + \Delta\bar{t}_{\mathrm{D}}^{ON_f}$, feed two flip-flops, from whose output one can identify the value of T_{D}^f. In fact, as shown also in Fig. 15, when $T_{\mathrm{D}}^f \approx T - \Delta\bar{t}_{\mathrm{D}}^{ON_f}$ thanks to the choice of τ_1 and τ_2, we get $Q_1Q_2 =$ '11'. Similarly, $Q_1Q_2 =$ '01' or $Q_1Q_2 =$ '00' when $T_{\mathrm{D}}^f \approx T$ or $T_{\mathrm{D}}^f \approx T + \Delta\bar{t}_{\mathrm{D}}^{ON_f}$. By setting $\tau_1 \approx T - 15$ ns and $\tau_2 \approx T + 15$ ns, a correct recovery is always ensured and

[7]The $V_{\mathrm{CK}}^{rec}(t)$ recovered in this very simple way presents a duty-cycle and a phase lag that are different at each clock cycle, as visible in Fig. 14(b). Indeed, this is enough if the purpose of this clock is only to synchronize the communication process.

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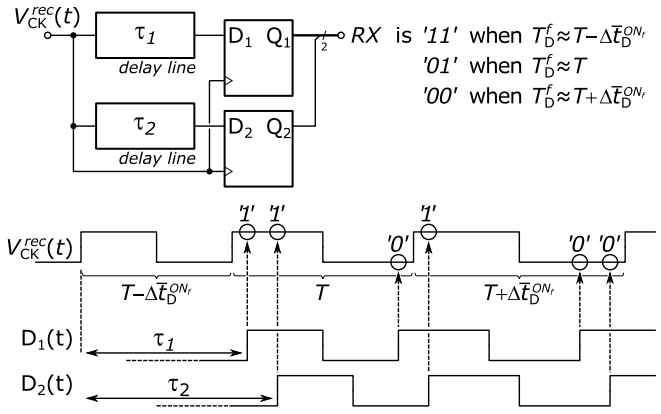


Fig. 15. Schematic and working principle of the simple asynchronous circuit used for the detection of forward transmitted symbols.

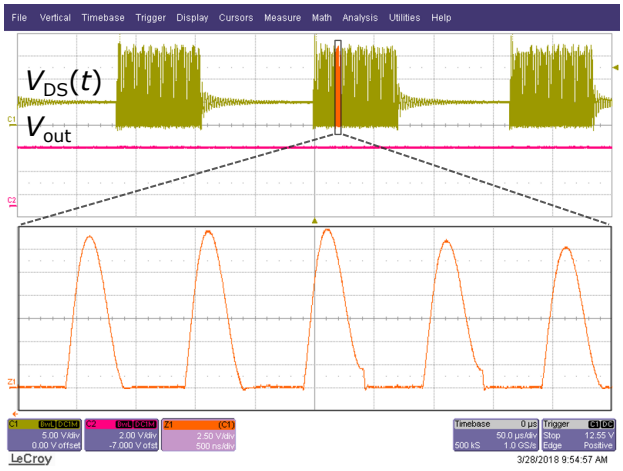


Fig. 16. Waveforms of the resonant converter in on-off operating mode.

no transmission errors have been recorded in several hours of circuit testing.

C. Application example: ON-OFF control

In order to provide a possible application for the proposed communication approach, we have implemented an on-off control to set the output voltage to $5\,\mathrm{V}$.

The working principle is very easy. All timings, including the clock, the length of time period in which the converter is enabled (i.e., the clock is turned on), and the length of the time period in which it is disabled (clock turned off), are set by the timing module of the ARM controller at the primary side. However, the regulation algorithm is run on the ARM controller at the secondary side as follows.

First, the output voltage is read and converted into a digital word by means of the ADC embedded in the ARM. Then, the resulting value is compared with a reference one. If the output voltage is too high, then the processor increases the value of the on-off duty cycle with respect to the actual one, while decreases it if the output voltage is too low. The desired value of the duty cycle is sent backward to the primary side.

The ARM controller at the primary side reads the desired value of the on-off duty cycle, and updates the internal registers of the timing module. Of course, communication is possible only in the on state, and requires a complex synchronization mechanism whose description is out of the scope of this example. Without entering into details, as soon as the converter is turned on, the secondary side wakes up the transmission module, and sends the updated value of the desired on-off duty cycle. The primary side reads the value, but can apply it only after the successive turn on event, with a delay that in our prototype is in the order of fractions of ms. Since the bandwidth of our converter is limited, this is not an issue. Note that enabling the backward communication is enough to implement this example.

Fig. 16 shows the converter operating in this mode. The two waveforms plotted in the figure are V_{out}, that is regulated to the desired value of $5\,\mathrm{V}$, and $V_{\mathrm{DS}}(t)$, from which it is possible to see both the backward communication and the on-off modulation with a duty cycle of about 40%.

VII. The Performance-Reliability Trade-off

In the designed prototype, no transmission errors have been recorded either in forward or in backward communication mode. Indeed, the detectability conditions in (5) have been set to very conservative values, thus ensuring a pretty easy recovery of the transmitted bit.

It is intuitive that by lowering the values of $\hat{V}_{\mathrm{NZ}}^{b}$, $t_{\mathrm{SW}}^{ON} - \hat{t}_{\mathrm{B}}^{ON_b}$ and $\Delta\bar{t}_{\mathrm{D}}^{ON_f}$, the detection of transmitted symbols would be more difficult, and transmission errors may arise. The system would also become more sensitive to the tolerance of the elements of the circuit, whose variations modify in a random way all the detectability conditions. However, there would be also a positive effect, since the converter working point would be more similar to that of a converter operating according to the optimal class-E conditions, and so also performance. In other words, the proposed communication scheme comes at the cost of a reduction in converter performance. This degradation depends on the detectability conditions, and plays a role similar to the E_b/N_0 in a standard communication scheme.

A complete evaluation of the trade-off between performance and communication reliability would be extremely complex, and is out of the scope of this paper. Yet, we provide here some comparison between results obtained by the simulation of the canonical class-E converter of Fig. 2(a) and the proposed converter of Fig. 3. We prefer to propose results based on circuit simulation since, by comparing the design of Sec. V-A and that of Sec. V-B, it is clear that once a prototype has been designed for communicating, it is not possible to disable the communication module and allow it to operate as a conventional converter. Hence, comparing performance of two different prototypes would result unfair, in particular, if the differences are expected to be small. Note however that a simulation-based comparison is not impairing the reliability of the result. In fact, it has already been shown in [17] that the non-idealities considered in the design model allows a pretty good matching between expected and measured performances.

The first aspect we consider is the converter efficiency. The converter designed to operate at the optimum class-E working

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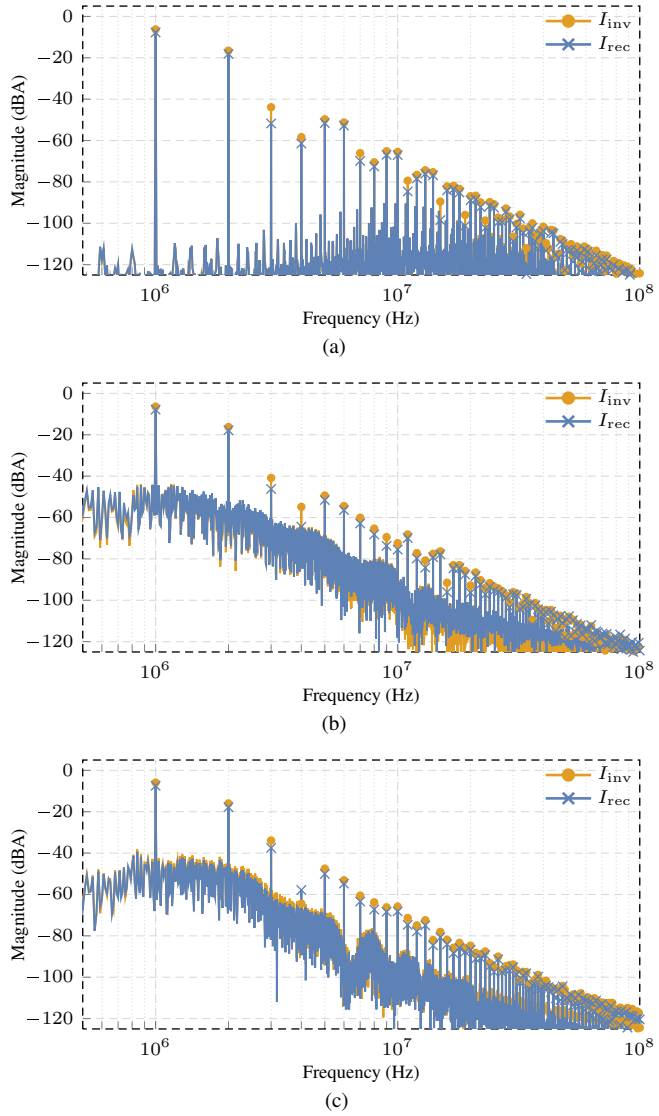


Fig. 17. Comparison between spectrum magnitude of the two currents $I_{\rm inv}$ and $I_{\rm rec}$ in the three cases: (a): standard converter with no communication capability; (b): proposed converter during backward communication; and (c): proposed converter during forward communication. The $0\,\mathrm{dB}$ reference level corresponds the magnitude of a sinusoidal tone whose RMS amplitude is $1\,\mathrm{A}$.

point has a 75.4% efficiency. Almost all the wasted energy is dissipated by the rectifying diode (46.6% of losses), while the energy dissipated by the MOS switch is only the 4.6% of the wasted energy. In backward communication mode the converter efficiency is equal to 74.3%. Again, almost all of the wasted energy (44.3% of the losses) is dissipated by the rectifying diode, while the energy dissipated by the MOS, thanks to the quasi-ZVS, is only slightly increased with respect to the reference case (5.0% of the losses). The efficiency in forward communication mode is 73.0%, that is lower with respect to the previous cases. This is mainly due to the fact the body diode always turns on, sometimes for long periods of time, and this is actually the worst condition. Wasted energy is still dominated by the rectifying diode (41.3% of losses), but that dissipated by the MOS grows to 6.7%[8].

A difference even smaller is observed in the output voltage ripple. When using a $10\,\mu\mathrm{F}$ capacitance as output filter with a $25\,\mathrm{m}\Omega$ equivalent series resistance, we get an RMS value of $12.57\,\mathrm{mV}$ for the output ripple. For the backward and forward communication, the RMS ripple slightly increases to $12.60\,\mathrm{mV}$ and $13.11\,\mathrm{mV}$ respectively. Such a tiny difference will be hardly noted in a real measurement, and it is justified by the fact that the $I_{\rm rec}(t)$ is indeed dependent on the transmitted symbol, but the observed variations are small.

As a final performance comparison, we consider the Electro-Magnetic Interference (EMI) of the prototype by comparing the magnitude spectrum of the two currents $I_{\rm inv}$ and $I_{\rm rec}$ flowing into the inductance $L_{\rm rec}$ and the transformer, which are the main sources of EMI emissions. Fig. 17(a) refers to the canonical class-E case, whereas Fig. 17(b) to the backward communication and Fig. 17(c) to the forward communication. All spectra have been computed with a $10\,\mathrm{kHz}$ resolution using a uniform window, and markers have been placed at all harmonics of the switching frequency. By comparing the plots, we can say that there is a negligible difference in the spectral components with the highest power, given by the lowest harmonics of the switching frequency, that are slightly higher (small fractions of dB) in the non-communication case. However, in the neighborhood of all harmonics, many low-energy components (whose magnitude is about $-40\,\mathrm{dB}$ with respect to the corresponding harmonic) arise. This is indeed expected: with the communication we are introducing a sort of *random modulation* into the considered waveforms in a scenario very similar to that one can find in the *spread spectrum* approach [32]–[37], where new spectral components are intentionally introduced with the aim of reducing the already existing ones. Since the modification of the $I_{\rm inv}$ and $I_{\rm rec}$ is very limited, also this effect is limited, and the EMI behavior of the converter while communicating is expected to be almost the same as that of the converter operating in the standard mode.

VIII. Conclusion

In this paper we have presented an innovative high-speed bidirectional through-the-barrier communication methodology for isolated class-E resonant converter. The proposed methodology is based on connecting and disconnecting an auxiliary capacitance, thus allowing the waveforms of the converter to switch between a slow and a fast response mode, that is easy detectable at the other side of the galvanic barrier. In this way, the transformer used for transferring power from the primary to the secondary side is used also to create the bidirectional data channel. The main advantage of the proposed methodology is that the creation of the communication channel comes at no cost in terms of limitation of the maximum transferred power, that is the same of a standard class-E converter. The methodology is supported by measurements on a low-frequency proof-of-concept prototype.

[8]Note that, for the sake of simplicity, in the computation of the efficiency the energy required for driving the MOS switches has not been considered.

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