Optimisation of a Doherty power amplifier based on dual-input characterisation

Optimisation of a Doherty power amplifier based on dual-input characterisation

Anna Piacibello[1,2], Roberto Quaglia[3], Vittorio Camarchia[2], Chiara Ramella[2], Marco Pirola[2]
[1]*Università di Roma Tor Vergata*, Roma, Italy
[2]*Politecnico di Torino*, Torino, Italy
[3]*Cardiff University*, Cardiff, UK
[1,2]anna.piacibello@polito.it, [3]quagliar@cardiff.ac.uk

***Abstract*—The success of the Doherty architecture compared to other efficiency enhancement techniques derives mainly from its simple design and full-RF nature, not requiring complex digital signal processing to achieve high back-off efficiency.**
In this work we propose a design strategy for the optimisation of a Doherty power amplifier to mitigate the typical practical issues of this architecture related to inaccuracy of the non-linear model and of the manufacturing. The approach is based on the experimental characterisation of a dual-input Doherty prototype without input section. This test structure is obtained from a single-input Doherty amplifier, designed only through non-linear simulations, by removing the input section and allowing for separate control of the two RF inputs. From the collected data, approximated functions for the phase shift and power splitting versus frequency are identified to be realizable in hardware with RF networks. Compared to the reference single-input Doherty stage, a significantly improved behavior is registered in terms of output power (up to 2.7 dB), efficiency at saturation and back-off (30 % and 15 % respectively) and power gain (2 dB).

***Index Terms*—power amplifier, Doherty, high efficiency**

I. Introduction

The Doherty power amplifier (DPA) [1] is an efficiency enhancement architecture popular for medium-/high-power telecom amplifiers working below 6 GHz. Conventional class-AB amplifiers [2]–[4], and even solutions that can reach very high efficiency at saturation, such as harmonically tuned class-F [5], [6] and switching class-E [7], [8] amplifiers, result in poor average efficiency of the transmitter in the presence of non-constant envelope modulations. Conversely, the DPA allows the transmitter to operate efficiently thanks to its extended high-efficiency region [9], [10]. The DPA is gaining momentum also in microwave monolithic integrated circuit (MMIC) realisation at higher frequencies, for applications like backhaul, satellite and, in the near future, the next generation (5G) of mobile communications [11]. One of the reasons behind the success of this technique is its full-RF implementation, which makes — at least in principle — any digital signal processing (DSP) unnecessary, as opposed to other techniques such as envelope tracking [12] or outphasing [13], [14].

Despite the simplicity of the DPA architecture, an optimised design of the input phase alignment and power splitting must be ensured to achieve the proper load modulation and output power combination over a wide frequency range. This is particularly critical when the target bandwidth exceeds few fractional points, as often required by modern applications [15], [16]. Practical implementations of hybrid DPAs frequently present sub-optimal load modulation due to the inaccuracy of the large-signal models of active devices, especially when biased in class-C, thus requiring post-tuning.

In this paper we present an experimental design approach for the optimisation of the DPA input section, based on the characterisation of a dual-input test structure that allows to determine the optimum amplitude and phase functions of the two inputs versus frequency to be synthesised for the final DPA module. To this aim, two prototypes have been fabricated: a single-input 20 W standard 6 dB AB-C DPA working in the S-band, designed through non-linear simulations and used as a reference, and its equivalent dual-input DPA. The optimised DPA shows in the 2.7 GHz to 3.3 GHz range an output power higher than 43.2 dBm and an efficiency in excess of 49 % and 33 % at saturation and 6 dB output back-off (OBO), respectively. This represents an improvement of up to 2.7 dB of output power, 30 % and 15 % of efficiency at saturation and back-off, respectively, and 2 dB of power gain with respect to the reference single-input DPA.

II. Optimisation strategy

The DPAs are composed of two branches (see Fig. 1): a Main PA and an Auxiliary PA. At a given OBO (6 dB for the standard DPA) the Main PA reaches its maximum output voltage swing becoming maximally efficient. From this power level onwards, the Auxiliary turns on and injects current into the common node, increasing the output power and modulating the load seen by the Main PA. The load at the Main active device is ideally modulated from $2R_{\mathrm{opt}}$ at low power to R_{opt} at saturation. This is achieved by means of an impedance inverter at the output of the Main PA. At high frequencies, where active device parasitic elements become non-negligible, offset lines are often added to the matching networks to restore the optimal load modulation [17]. At the input of the Auxiliary PA a delay line is required to set the correct phase alignment of the currents at the output common node, which is crucial for proper power combination. The extension in power of the Doherty region is related to the ratio between Auxiliary and Main currents at the common node. Hence, the input splitter is a key component in designing a DPA since it is the

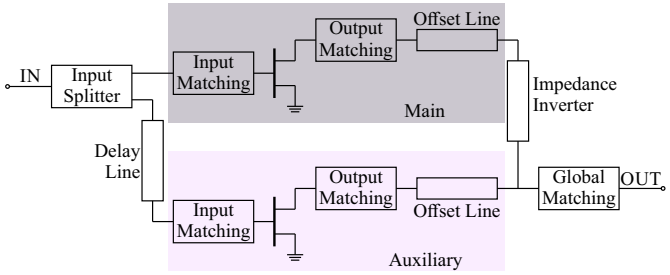


Fig. 1. Block diagram of a Doherty power amplifier.

main component to influence the phase and amplitude relation between the input of the two PAs.

In practical DPA implementations, power splitting and phase alignment are often difficult to design based on simulations. This is due to the inaccuracy of large-signal models in predicting the input impedance of the active devices, especially for class-C operation, leading to non-optimal load modulation and power combination. This problem, emphasized in case of wide operating bandwidths, often requires post-production tuning to restore optimal performance in full-RF DPAs. On the contrary, in dual-input DPAs [18]–[20] it is possible to adjust these two parameters dynamically as a function of input power and operating frequency. However, this comes at the cost of complex DSP algorithms that must be included in the transmitting system and accounted for in the overall efficiency budget. In previous works [19], [20], the simulated comparison of the two equivalent DPA prototypes was shown, highlighting the maximum performance improvement attainable thanks to the additional degrees of freedom offered by the dual-input DPA. This was achieved through a dynamical control of the two inputs, compatible only with a complex DSP implementation, and by applying also a variable bias point as an additional degree of freedom. Conversely, in this work, the optimisation space for the experimental characterisation of the dual-input DPA is limited to functions that can be implemented in hardware with RF networks and could serve as an alternative design approach for the DPA input section.

The dual-input test structure should include the input bias and stabilization networks, the active devices and the complete output combiner (output matching, impedance inverter and optional offset lines), i.e. all the elements of the DPA under development except the input splitter and phase delay line, which are instead present in the original single-input DPA used as a reference. The experimental characterisation of the dual-input prototype is carried out to determine the optimum phase difference $\phi = \phi_{\mathrm{Aux}} - \phi_{\mathrm{Main}}$ and power splitting $k = P_{\mathrm{Aux}}/P_{\mathrm{Main}}$ functions and quantify the possible improvement achievable with respect to the original single-input DPA. The employed dual-input test bench allows independent control of phase difference, input power and bias setting at each frequency and for each power level. However, the choice of extracting approximated smooth functions that limit the two-dimensional optimisation space (ϕ, k) has a twofold motivation. On one side, approximating the optimum driving conditions with functions that are realizable in hardware with RF analog networks can provide design guidelines for the synthesis, based on experimental data, of an input section that can improve the original DPA performance. On the other side, avoiding an arbitrarily fast variation of the branch driving signals makes the DSP more robust and less sensitive to calibration inaccuracies.

In particular, it is chosen to limit the optimisation space to:

- constant bias point
- power-independent phase difference ϕ

Once the phase and amplitude functions versus frequency are found for each branch driving signal, these can be applied to drive the DPA both under CW and modulated signal excitations.

III. Fabrication and Experimental Characterisation

In order to demonstrate the potential benefits of the proposed approach with respect to standard CAD-based design, a standard DPA and its equivalent dual-input test structure have been fabricated and tested, as shown in Fig. 2.

The active device adopted for both the Main and Auxiliary PAs is the CGH40010F 10 W packaged GaN transistors from Wolfspeed. The Main stage is biased in class-AB ($V_{\mathrm{DS}} = 28\,\mathrm{V}$, $I_{\mathrm{D}} = 70\,\mathrm{mA}$), while the Auxiliary is biased in class-C ($V_{\mathrm{DS}} = 28\,\mathrm{V}$, $V_{\mathrm{GS}} = -5\,\mathrm{V}$). The dual-input DPA differs from the single-input DPA in the input section only, where the input splitter and the delay line have been removed.

A. Small-signal characterisation

Small-signal characterisation is used as an initial assessment of the prototypes. The small-signal measurements are performed using a Keysight E8361A PNA Network Analyzer. Fig. 3 reports the simulated and measured scattering parameters for the two DPAs, adopting the port numbering indicated in Fig. 2. The two DPAs have been designed to work in a 10 % fractional band around 3.5 GHz, but a 300 MHz shift between simulated and measured direct voltage gain (S_{31}) is observed in both prototypes and is therefore ascribed to some inaccuracy in the manufacturing of the output section, which is identical in the two cases. The single-input DPA, exhibits an input return loss lower than 10 dB from 3 to 3.7 GHz, with a minimum around 3.4 GHz, while some mismatch is observed in the dual-input case as a consequence of the removal of the power divider.

B. Large-signal CW characterisation

Due to the frequency shift measured in small-signal conditions, the large-signal measurements have been performed in the frequency range 2.7 GHz – 3.3 GHz. Fig. 4 reports the block diagram of the measurement setup employed for both CW and system-level characterisation. Two vector signal generators (Keysight N5182B MXG) are used as RF signal sources, with shared local oscillators (LO) and base-band streams alignment to maintain phase coherency at both RF and base-band. Two nominally identical linear

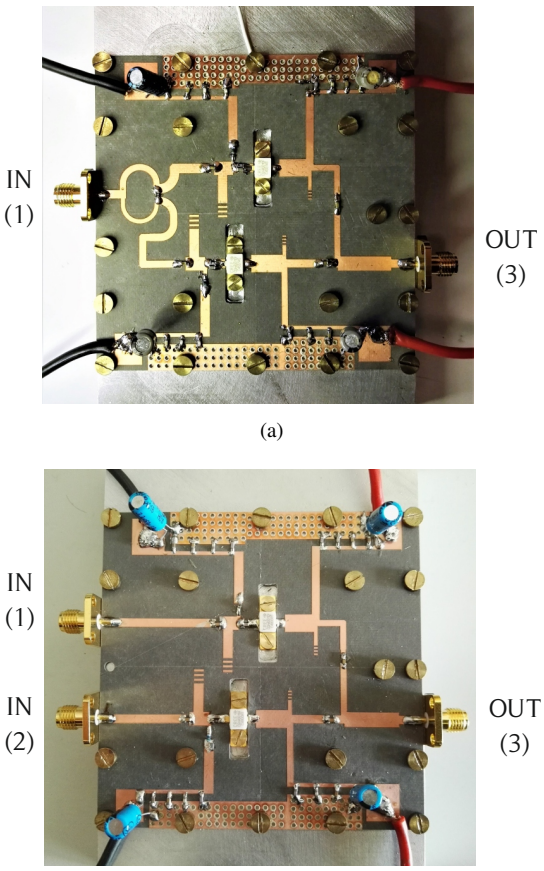


Fig. 2. Photographs of the single-(a) and dual-(b) input DPA.

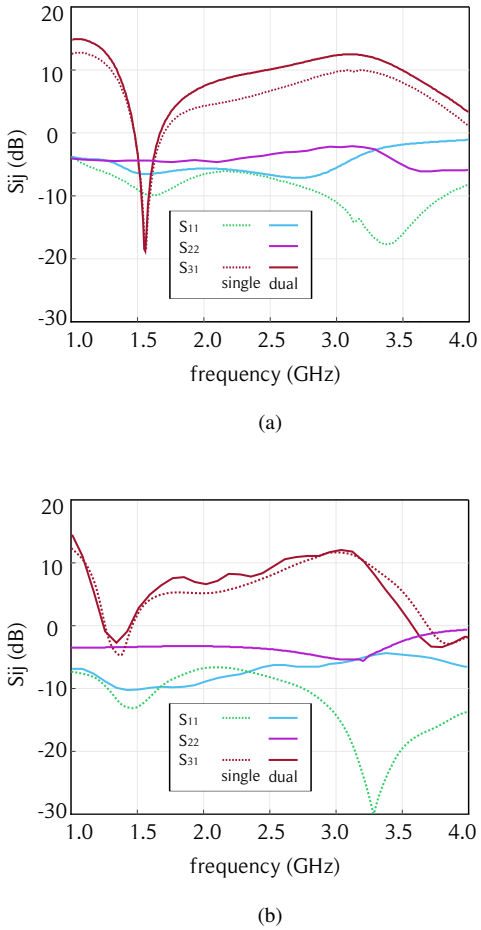


Fig. 3. Simulated (a) and measured (b) scattering parameters of the two DPA prototypes.

drivers amplify the RF signals and feed them to the DUT inputs. Pre-calibrated directional couplers at the input and output allow to measure the input (incident and reflected) and output power, by means of power meters. The output signal is down-converted to IF by a mixer, whose LO signal is generated by a Keysight E4422B MXG, and sampled by a Keysight DSO9254A oscilloscope (DSO) to perform digital *I/Q* down-conversion for system-level characterisation. The hardware setup has been used also for CW characterisation by simply applying a constant value base-band signal.

The same bias is adopted at all frequencies, while different phase delays ϕ and power splitting ratios k are explored in the characterisation of the dual-input prototype, searching for their optimum values. In particular, the phase is adjusted first, using the Main input signal as a reference and determining the optimum phase of the Auxiliary branch at the MXG plane at each frequency in the band of interest. While the phase coherency between the two generators is guaranteed and maintained by the hardware configuration used, the phase difference between the inputs at the DUT plane is unknown, and hence it requires calibration. The phase calibration procedure provides a $\Delta\phi_{\mathrm{CAL}}$ value that links the phase difference set at the generators $\Delta\phi_{\mathrm{GEN}}$ with the phase difference at the DUT as $\Delta\phi_{\mathrm{DUT}} = \Delta\phi_{\mathrm{GEN}} - \Delta\phi_{\mathrm{CAL}}$. The calibration procedure is based on a known 3-port DUT, in particular a 3 dB 90° hybrid. The two inputs are connected to the direct and coupled ports of the hybrid. The output power at the sum port of the hybrid is measured while sweeping $\Delta\phi_{\mathrm{GEN}}$. Ideally, the two inputs cancel each other when the phase difference between them is +90° (the S-parameters of the hybrid can be used to refine the phase value for the minimum and maximum), that corresponds to a generator phase difference of $\Delta\phi_{\mathrm{GEN,MIN}}$. The phase calibration value is determined as $\Delta\phi_{\mathrm{CAL}} = \Delta\phi_{\mathrm{GEN,MIN}} - 90°$. Once the optimum phase is set, the Main power is swept linearly and the input power splitting k is optimised following a piecewise constant approach, so that power is fed to the Auxiliary branch only in proximity of its turn-on, to further enhance gain and efficiency at low power.

Table I reports the optimum phase delay and splitting factor obtained for the prototype, constrained to be compatible with analog implementation.

The resulting CW performance of the optimised DPA at the band edges and at centre frequency is reported in Fig. 5, compared to that of the reference single-input DPA. A

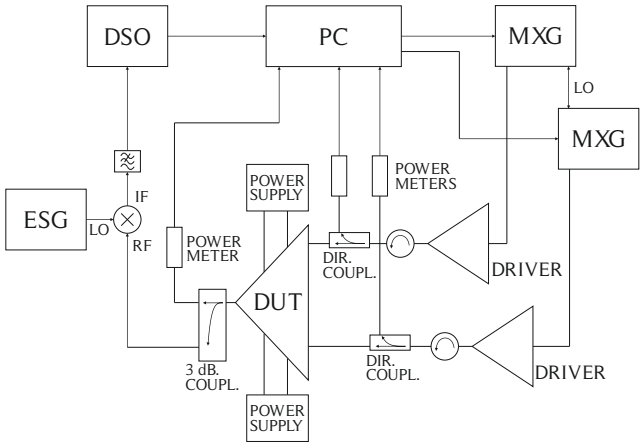


Fig. 4. Block diagram of the dual-input measurement setup.

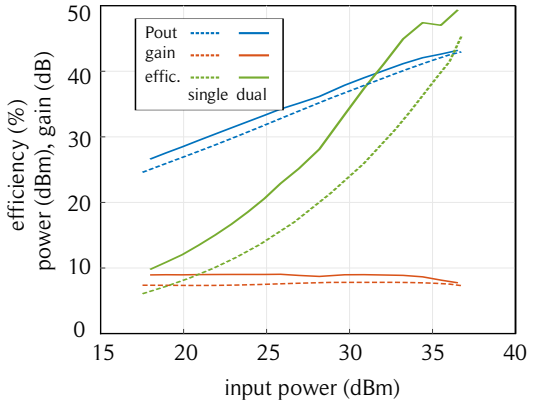
TABLE I
OPTIMUM DPA INPUT DRIVING VERSUS FREQUENCY.

Frequency	**Phase difference** ϕ	**Power splitting ratio** k (after break point)
2.7 GHz	100°	0.7
3 GHz	60°	0.5
3.3 GHz	30°	0.9

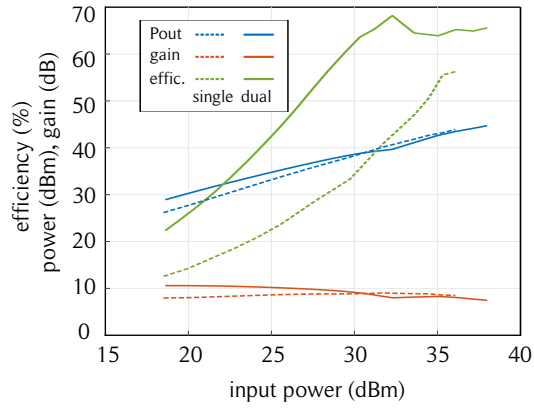
significant improvement is visible in all cases. In particular, an increase in saturated output power of 0.2 dB, 0.8 dB and 2.7 dB is achieved at 2.7 GHz, 3.0 GHz and 3.3 GHz, respectively. This aspect is the most indicative of the effectiveness of a frequency dependent phase re-alignment in improving and equalizing the DPA performance. A gain increase as high as 2 dB (also due to the piecewise constant splitting ratio) is observed, while the 6 dB OBO efficiency improvement ranges from 7 % at 2.7 GHz up to 30 % at 3 GHz frequency. Finally, saturated efficiency is improved up to 15 % at the highest frequency.

C. System-level characterisation

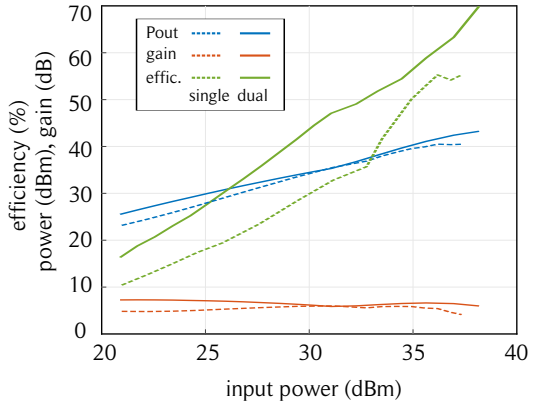
The system-level characterisation of the dual-input DPA is performed using the setup of Fig. 4. An OFDM LTE signal with 5 MHz bandwidth and 9 dB Peak-to-Average Power Ratio (PAPR) is used. The same optimum phase setting found for the CW measurements is adopted, together with a static splitting ratio for the two amplitudes. The measured output spectrum is reported in Fig. 6 (red) at an average output power of 35.9 dBm. In order to be compliant with spectral emission in terms of Adjacent Channel Leakage Ratio (ACLR), a digital predistortion (DPD) algorithm has been applied. In particular, a memory polynomial DPD has been used to generate a single predistorted signal that is then split according to the static phase and amplitude settings. The output spectrum with predistortion is shown in Fig. 6 (blue) at the same average output power of 35.9 dBm of the un-predistorted case. The resulting average efficiency is of 38 %. The DPD polynomial has odd order of 7 and 2 memory taps, corresponding to the minimum complexity that allows to meet the -45 dBc ACLR requirements.



(a) 2.7 GHz



(b) 3.0 GHz



(c) 3.3 GHz

Fig. 5. CW performance of the two DPA prototypes.

IV. CONCLUSION

A two-step design strategy to optimise the performance of hybrid Doherty PAs has been introduced, based on the experimental characterisation of a dual-input test prototype. The performance improvement with respect to a single-input

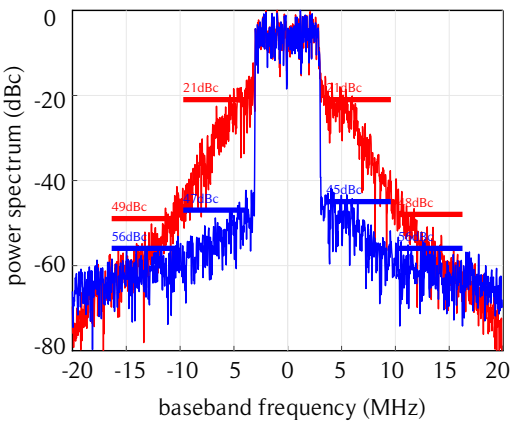


Fig. 6. Measured output power spectrum of the optimzed DPA with 5 MHz OFDM LTE signal and 9 dB PAPR, before (red) and after (blue) DPD. Centre frequency: 3 GHz. Average output power: 35.9 dBm. Average efficiency: 38 %.

DPA whose input section was designed based purely on simulations has been proved experimentally. Measurements under both CW and modulated signal excitation are presented.

REFERENCES

[1] W. H. Doherty, "A new high-efficiency power amplifier for modulated waves," *Bell Syst. Technical J.*, vol. 15, no. 3, pp. 469–475, Jul. 1936.

[2] Hui Li, K. Bathich, O. Bengtsson, and G. Boeck, "A Si LDMOS class AB power amplifier for UMTS LTE base stations," in *German Microwave Conference Digest of Papers*, March 2010, pp. 272–275.

[3] N. Khalid, T. Abbas, and M. Bin Ihsan, "Power amplifier design using GaN HEMT in class-AB mode for LTE communication band," in *2015 International Wireless Communications and Mobile Computing Conference (IWCMC)*, Aug 2015, pp. 685–689.

[4] M. Iqbal and A. Piacibello, "A 5W class-AB power amplifier based on a GaN HEMT for LTE communication band," in *2016 16th Mediterranean Microwave Symposium (MMS)*, Nov 2016, pp. 1–4.

[5] J. Moon, S. Jee, J. Kim, J. Kim, and B. Kim, "Behaviors of Class-F and Class-F^{-1} Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1937–1951, June 2012.

[6] M. Iqbal and A. Piacibello, "GaN HEMT based class-F power amplifier with broad bandwidth and high efficiency," in *2016 International Conference on Integrated Circuits and Microsystems (ICICM)*, Nov 2016, pp. 131–134.

[7] D. Kalim, D. Erguvan, and R. Negra, "Broadband CMOS class-E power amplifier for LTE applications," in *2009 3rd International Conference on Signals, Circuits and Systems (SCS)*, Nov 2009, pp. 1–4.

[8] S. Jee, J. Moon, J. Kim, J. Son, and B. Kim, "Class-E power amplifier optimization for operation above maximum frequency," in *2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS 2011)*, Nov 2011, pp. 1–5.

[9] A. Grebennikov and S. Bulja, "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190 –3219, Dec. 2012.

[10] R. Quaglia, V. Camarchia, J. J. Moreno Rubio, M. Pirola, and G. Ghione, "A 4-W Doherty Power Amplifier in GaN MMIC Technology for 15-GHz Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 365–367, April 2017.

[11] V. Camarchia, A. Piacibello, and R. Quaglia, "Integrated Doherty power amplifiers for satellite systems: challenges and solutions," in *2019 IEEE Topical Workshop on Internet of Space (TWIOS)*, Jan 2019, pp. 1–4.

[12] F. Wang, A. H. Yang, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.

[13] F. Raab, "Efficiency of Outphasing RF Power-Amplifier Systems," *IEEE Trans. Commun.*, vol. 33, no. 10, pp. 1094–1099, October 1985.

[14] A. Piacibello, R. Quaglia, M. Pirolaf, and S. Cripps, "Design of an S-Band Chireix Outphasing Power Amplifier Based on a Systematic Bandwidth Limitation Analysis," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2018, pp. 186–189.

[15] J. J. Moreno Rubio, V. Camarchia, R. Quaglia, E. F. Angarita Malaver, and M. Pirola, "A 0.6–3.8 GHz GaN Power Amplifier Designed Through a Simple Strategy," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 446–448, June 2016.

[16] C. Ramella, A. Piacibello, R. Quaglia, V. Camarchia, and M. Pirola, "High Efficiency Power Amplifiers for Modern Mobile Communications: The Load-Modulation Approach," *Electronics*, vol. 6, no. 4, 2017.

[17] R. Quaglia, M. Pirola, and C. Ramella, "Offset Lines in Doherty Power Amplifiers: Analytical Demonstration and Design," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 2, pp. 93 –95, Feb. 2013.

[18] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A Dual-Input Digitally Driven Doherty Amplifier Architecture for Performance Enhancement of Doherty Transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1284–1293, May 2011.

[19] A. Piacibello, R. Quaglia, V. Camarchia, C. Ramella, and M. Pirola, "Dual-input driving strategies for performance enhancement of a Doherty power amplifier," in *2018 IEEE MTT-S International Wireless Symposium (IWS)*, May 2018, pp. 1–4.

[20] A. Piacibello, M. Pirola, V. Camarchia, C. Ramella, R. Quaglia, X. Zhou, and W. S. Chan, "Comparison of S-Band Analog and Dual-Input Digital Doherty Power Amplifiers," in *2018 48th European Microwave Conference (EuMC)*, Sep. 2018, pp. 1237–1240.