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19 November 2026

Thermal-aware GaN/Si MMIC design for space applications

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***Abstract*—Thermal stress in microwave power devices is a major issue for space applications, with a detrimental impact on the operating life-time of MMICs on board satellites. To limit this, derating rules are applied to the maximum operating junction temperature, which however limit the potential device performance when GaN/Si technology is employed. In this framework, classical power amplifier design paradigm must be reconsidered, moving to a thermal-aware design approach. To this aim, it is crucial to have access to highly reliable thermal models of the adopted devices. This work will show that, adopting a simplified but effective thermal model and proper design strategy, GaN/Si technology can be successfully adopted for space-compliant MMIC design up to Ka-band. In particular, the preliminary design of a 10 W MMIC working in Ka-band at 36 GHz will be presented based on the 100 nm gate-length GaN/Si HEMT process from OMMIC foundry.**

***Index Terms*—power amplifier, MMIC, satellite communication, thermal analysis, Raman scattering**

I. Introduction

Satellite technology counts a large number of different applications both commercial, such as communications, navigation and weather forecasting, and scientific, such as astronomy, glaciology, geophysics and environmental research [1]. Satellite communication to/from earth demands for the development of highly efficient microwave front-ends, and in particular power amplifiers (PAs), working in the high frequency Ku- to Ka-bands.

Power efficiency is a key feature for a PA conceived for space application, being solar-cells and batteries the only power supply available on board satellites, which still represents a great challenge at high frequency, often demanding for efficiency enhancement approaches [2]. Besides efficiency, high reliability and slow aging must be ensured in order to sustain long-term operation of the satellites (several years/decades of mission). To increase reliability and insure sufficient life-time, electronics systems for space applications must comply with derating rules [3], i.e. they must be designed so as to operate at a significantly reduced level of stress. The major source of stress for high-power active devices is self-heating, and in space applications the absence of heat conduction and convection exasperates this aspect. Therefore, the maximum operating temperature of active devices must be drastically limited with respect to the maximum values allowed for reliable earth applications and this in turns limits the device capabilities and performance.

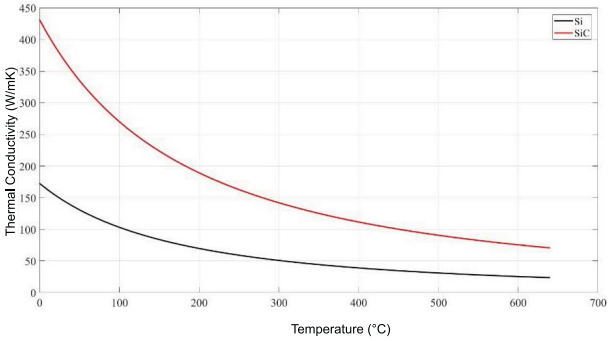


Fig. 1. Thermal conductivity of 100 μm SiC and Si substrates.

GaN technology, already well exploited within PAs for terrestrial applications [4], is becoming interesting also for space usage, since it provides remarkably high power densities at the frequencies of interest, together with low losses (passive networks) and low-noise performance (receiver). GaAs, even if suitable for this frequency range, is strongly limited by low breakdown voltage [5]. GaN epitaxy can be grown on both SiC and Si substrates. SiC is characterized by extremely good thermal behaviour, that greatly mitigates the heat dissipation issue, but it is very expensive, also considering the limited number of high quality SiC substrate providers. On the other hand, the use of Si substrate, while penalizing thermal behaviour as shown in Fig. 1, would lead to lower cost with respect to SiC, which is an essential aspect for high volume of production, and it would allow, in the future, for the integration of RF and digital sub-systems on the same chip.

GaN/Si technology, compared to GaN/SiC counterpart, is therefore sensibly limited by thermal issues, in particular in case of space applications where temperature and voltage derating must be applied. In such scenario, the classical design paradigms usually adopted for power amplifiers must be reconsidered, targeting the best possible trade-off between desired output power and maximum allowable channel temperature. To this aim, it is crucial to have access to highly reliable and accurate thermal models.

This work will show the rationale behind a thermal-aware

TABLE I
DESIGN SPECIFICATIONS.

Specification	Value
Operating frequency	36 GHz
Output power	10 W (40 dBm)
Operating temperature (base-plate)	80 °C
Maximum junction temperature	160 °C
Maximum gain compression	2 dB

TABLE II
FEATURES OF THE OMMIC D01GH GAN/SI PROCESS.

Parameter	Value		Derating
Cut-off frequency, f_T	105 GHz	Typ.	-
Saturation current, I_{DSS}	1.3 mA/mm	Typ.	-
Supply voltage, V_{DS}	15 V	Max.	75 % $\Rightarrow$ 11.25 V
Breakdown voltage, V_{GDb}	40 V	Min.	-
Junction temperature, T_j	200 °C	Max.	-40 °C $\Rightarrow$ 160°C

design process, exploiting a 100 nm gate-length GaN/Si HEMT process from a commercial European foundry (OMMIC). The thermal model of the active devices will be discussed and compared to thermal measurement results, and the design of the output stage of a 10 W PA for space applications working at 36 GHz will be presented.

II. DESIGN EXAMPLE: 10 W GAN/SI KA-BAND MMIC

The present work aims to highlight the differences between standard GaN/Si MMIC PA design, for terrestrial (e.g. telecom) applications, and a thermal-aware design approach, tailored instead for space applications. To contextualize the discussion a design example is considered, which main design requirements are summarized in Table I. The considered example is a narrow-band 10 W PA at 36 GHz, which is considered as a possible uplink frequency for next satellite communication applications. The maximum junction temperature of 160 °C is a typical value for GaN devices constrained to space applications and corresponds to a temperature 40 °C below the maximum value indicated by the selected manufacturer [3], [6], [7]. The example design focuses only on the final (power) stage of the PA, neglecting the design of driver stages, which would be required in a complete PA design to achieve usable gain levels. A simple but effective parallel combined strategy is considered [8] and, as an additional constraint, the maximum number of parallel combined device is set to 8 in order to limit the chip area and output combiner losses to a reasonable value. For the latter, a worst-case value of 1 dB is considered, which increases the output power requirement to roughly 12.6 W.

III. TECHNOLOGY

The selected process is the D01GH 100 nm gate-length GaN/Si HEMT process from OMMIC, a commercial European foundry. Process design kit (PDK) is available for this process, both for Keysight ADS (adopted in this work) and NI AWR-MWO design suites, including electro-thermal nonlinear model, electromagnetic model, components' layouts and statistic data. The main features of the selected technology are summarized in Table II [6]: the high cut-off frequency of this process makes it suitable for application in Ka-band [9], [10].

Considering the given $V_{DS,max} = 15$ V and $I_{DSS} = 1.3$ mA/mm, an output power density around 5 W/mm is expected. When derating is applied to V_{DS}, this value reduces to roughly 4 W/mm, which is a remarkable output power for Ka-band applications. However, when derating is applied also to the maximum junction temperature T_j, the achievable output power is clearly limited (see Table III), and a careful selection of the optimum load is required, as discussed in Section V. The results reported in Table III are based on ADS simulations, carried out adopting the thermal model discussed in Section IV below. Two different device sizes are compared: 8x50 μm (400 μm periphery) and 8x75 μm (600 μm periphery). In both cases the maximum output power exceeds the nominal value, however, the junction temperature is well above its maximum value, making such power levels practically unachievable and confirming that device heating is the actual limit of this technology. A maximum output power density around 4 W/mm is obtained, as expected, at the maximum thermal limit of the technology ($T_j = 200$ °C), indicating that a minimum periphery around 3.2 mm is required to achieve the required output power of 12.6 W. Conversely, at the maximum derated junction temperature ($T_j = 160$ °C), the achievable output power density decreases to only roughly 3 W/mm, thus increasing the minimum necessary periphery to 4.2 mm to reach the same output power.

TABLE III
SIMULATED MAXIMUM OUTPUT POWER AT DIFFERENT JUNCTION TEMPERATURES. SUPPLY VOLTAGE 11.25 V.

Device	P_{out} W/mm	T_j °C	P_{diss} W/mm	PAE %	Notes
8x75 μm	5.6	250	4.0	45	max. P_{out}
	4.2	200	3.0	47	max. T_j
	3.0	160	2.1	47	max. derated T_j
8x50 μm	4.6	240	4.1	41	max. P_{out}
	4.1	200	3.2	46	max. T_j
	3.3	160	2.2	50	max. derated T_j

IV. THERMAL MODEL

The OMMIC PDK comes with two different thermal models of its active devices. The first is a simplified static 1D heat flow model, while the second is a 3D thermal stack that can be used within a FEM-based numerical thermal simulator (e.g. HeatWave for Keysight ADS). Such simulators solve the dynamic Fourier heat equation using as heat source the electrical power dissipated within the device. The latter is computed from electrical simulations within an electro-thermal loop. This approach is more accurate and can account, for example, for the different finger temperatures within the same device. Despite this, the numerical effort it requires, in terms of simulation time, makes the simplified model the only viable approach for design and optimization purposes. Accurate

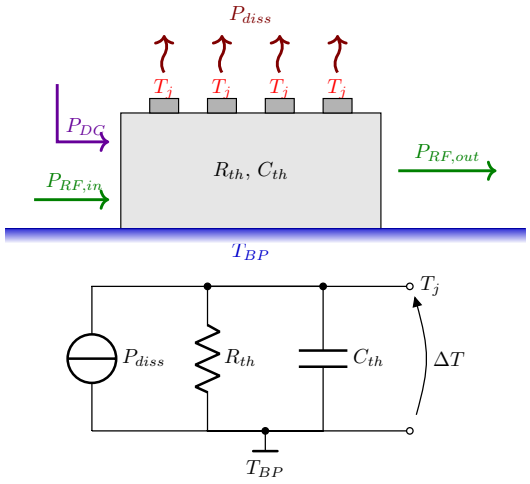


Fig. 2. Simplified thermal model of the active device and electrical equivalent.

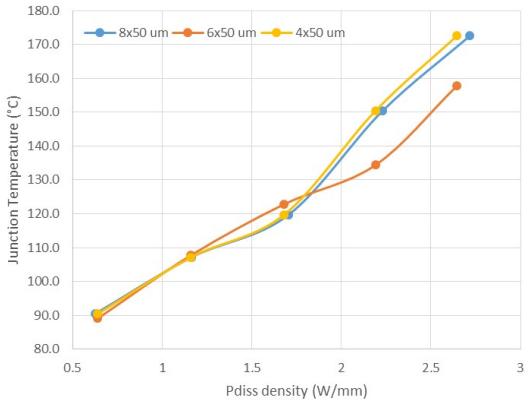


Fig. 3. Raman measurements: junction temperature of different devices as a function of the dissipated power density.

electro-thermal simulations, on the other hand, can be used for *a posteriori* verifications during the most relevant design steps.

The simplified thermal model adopts a thermal resistance approach. As shown in Fig. 2, the device is modeled by a thermal resistance R_{th} defined as

$$R_{th} = \frac{\Delta T}{P_{diss}} \tag{1}$$

where ΔT is the temperature increase due to power dissipation in the device, and represents the difference between the maximum temperature T_j reached in the device active region, right below the fingers (and considered the same for all the device's fingers), and the base-plate temperature T_{BP}. The dissipated power, when the transistor is operated in continuous wave, is given by

$$P_{diss} = P_{DC} + P_{RF,in} - P_{RF,out} \tag{2}$$

The dynamic thermal behaviour is modeled by means of a thermal capacitance C_{th}, which gives, in combination with R_{th} a thermal time constant $\tau_{th} = R_{th}C_{th}$. The resulting system is a single time-constant low-pass filter, as highlighted in Fig. 2. According to the foundry model, the thermal time constant is $\tau_{th} = 160\,\mu$s, thus the junction temperature reaches its maximum value $T_{BP}+R_{th}P_{diss}$ after approximately 800 μs of continuous wave operation.

The simplified non-linear thermal model adopts a thermal conductivity with hyperbolic dependence on temperature [11], and implements a 1D Fourier heat equation, where heat is considered to adiabatically flow from the top surface, where the active device junctions generate it, to the bottom, where the heat sink keeps a constant base-plate temperature. This model correctly accounts for substrates built up with layers having different thermal properties, provided that all layers share the same functional temperature dependence on thermal conductivity [12]. In this case, in fact, the Kirchhoff transformation validity is maintained across the several layers [13].

Introducing the total thermal resistances of the substrate evaluated at the reference temperature T_0^a (superscript a denotes absolute temperatures in kelvin) as

$$R_{th,REF}(T_0^a) = \frac{H}{A} \cdot \frac{1}{K_{th}(T_0^a)} \tag{3}$$

where H is the substrate thickness, A the area of the device footprint and $K_{th}(T_0^a)$ the thermal conductivity at T_0^a , we have

$$T_j^a = T_{BP}^a \exp \frac{R_{th,REF}(T_0^a)P_{diss}}{T_0^a} \tag{4}$$

where T_{BP}^a is the (absolute) base-plate temperature. The OMMIC PDK gives, for any device periphery, the value of $R_{th,REF}$ at 20 °C (293.15 K).

A. Thermal model verification

The validity of the simplified thermal model is verified both through 3D electro-thermal simulations and through experimental Raman characterization [14], [15].

The Raman characterization of the devices has been performed monitoring the Raman shift of the Si layer below the GaN layer in the channel region [16]. A calibration law is extracted first, with no bias applied to the device, to correlate Raman shift to temperature. Then, in the dissipation phase, the temperature of the base-plate is fixed (80 °C), and the power dissipated in the device is varied by changing the bias voltage. In order to correlate the measured temperature in the Si layer to the junction temperature in the GaN channel region, the 3D thermal simulation results are exploited. Raman measurements were carried out on different active device samples made available from the foundry, namely the 8x50 μm, the 6x50 μm and the 4x50 μm devices. The measurement results are compared in Fig. 3.

Finally Fig. 4 reports the comparison between the results obtained with the electro-thermal simulation, the Raman characterization and the simplified model predictions, for the

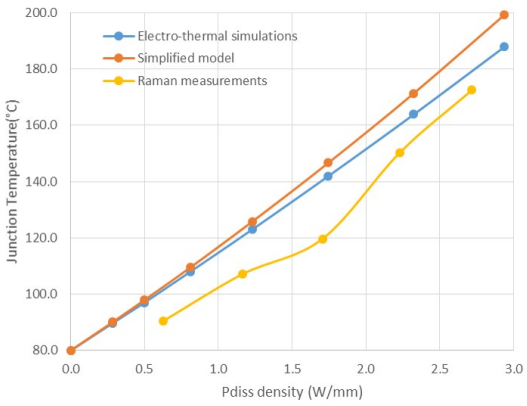


Fig. 4. Junction temperature as a function of dissipated power density: comparison between electro-thermal simulations, simplified model predictions and Raman measurement results (8x50 μm device).

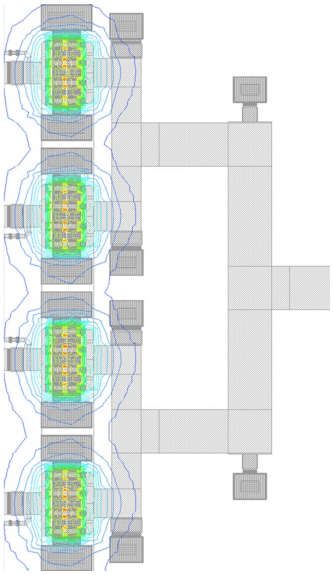


Fig. 5. 3D thermal simulation results for 4 parallel combined 8x75 μm devices.

8x50 μm device. The results are in very good agreement, with the simplified model showing slightly higher temperatures than the other, more accurate, models. Therefore, despite the approximations, the simplified model is a very effective tool for quick junction temperature estimation for MMIC design purposes.

B. Crosstalk effect

Equation (4) is valid for a single isolated device. When more devices must be combined in parallel in a small chip area, as is usually the case for Ka-band PAs, the device heating due to neighbour devices (crosstalk effect) must be accounted for. This can be done by adjusting (increasing) the value of $R_{th,REF}$, but 3D electro-thermal simulations are required to find the actual value of this equivalent reference thermal resistance for the actual device configuration considered in the PA under development.

Fig. 5 reports, as an example, the 3D thermal simulation results for 4 parallel combined 8x75 μm devices. As can be noted the heat spread through the output combiner is negligible and the cooling effect of the via holes at the source terminals makes the devices almost thermally decoupled. In fact, an increase of only 2.2 % of $R_{th,REF}$ is required to correctly account for thermal crosstalk.

V. Thermal-aware design of the 10 W Ka-band PA

The results of Fig. 4 highlight that the junction temperature is the most stringent limit of this technology, which bounds the maximum allowable dissipated power to approximately 2.2 W/mm at $T_{BP} = 80\,°\text{C}$.

Performance of microwave devices depends on the selected load termination. Dissipated power, and thus junction temperature, is not an exception, therefore, when moving in space applications framework, the optimum load is no more the one that gives the maximum output power, like in classical PA design, but it must be selected as the best compromise between output power and junction temperature. Moreover, power gain, efficiency and eventually output mismatch should be considered, since an optimum trade-off typically exist among all these device performance. To find this optimum termination, simulated thermal load-pull maps must be drawn, which give the most complete and straightforward information on optimum load selection.

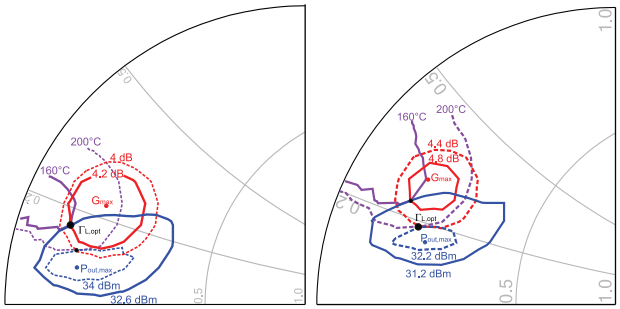
In Fig. 6 the load-pull simulation results for the 8x50 μm and 8x75 μm devices are compared. Contours are referred to 1 dB gain compression. The junction temperature contours are computed from the CW dissipated power with (4) adopting the $R_{th,REF}$ values obtained from 3D simulations for 8 parallel devices, thus slightly higher than the values given in the PDK (see Section IV-B). This results confirm that, targeting a minimum output power of 32 dBm, the 8x50 μm device can be used in a classical PA design ($\Gamma_{L,opt}$ laying on the $T_j = 200\,°\text{C}$ contour), while the larger 8x75 μm device is required when dealing with the $T_j = 160\,°\text{C}$ limit posed by space derating. Fig. 7 reports a more detailed load-pull chart for the 8x75 μm device, showing also PAE (contours with 1 percentage point step) and output mismatch contours (2.5 dB step). The latter are computed as

$$\text{Mismatch} = 20\log_{10}\left|\frac{\Gamma_L - \Gamma_{out}^*}{1 - \Gamma_L\Gamma_{out}}\right| \tag{5}$$

and represent a good estimation of the PA output return loss. From these results the optimum load can be selected as $\Gamma_{L,opt} = 0.82\text{e}^{j161°}$, which guarantees the best trade-off among all the considered performance, as shown in Table IV.

Figure 8 shows the large-signal CW simulations results at 36 GHz of the device terminated with the selected optimum load, the temperature increase ΔT is defined as $T_j - T_{BP}$, where $T_{BP} = 80\,°\text{C}$.

To complete the design of the final stage, an output combiner network matching $\Gamma_{L,opt}$ at each device output to a common 50 Ω load, has been developed, as shown in Fig. 9.



(a) 8x75 μm device (b) 8x50 μm device

Fig. 6. Load-pull results at $V_{DS} = 11.25$ V, 1 dB compression.

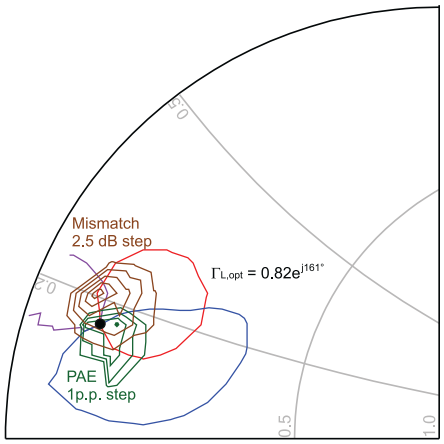


Fig. 7. Load pull contours at 1 dB compression for the 8x75 μm device, $V_{DS} = 11.25$ V.

The performance of this final stage are shown in Fig. 10: the devices are well matched to $\Gamma_{L,opt}$ and output power of each single device is around 32 dBm. The output combiner losses are within 0.85 dB, thus the achieved output power is above 40 dBm at a gain compression slightly above 1 dB. The associated junction temperature is within the 160 °C limit, thus demonstrating the potentiality of the selected GaN/Si technology for high-frequency space applications.

VI. Conclusion

This work shows a thermal-aware MMIC PA design approach that should be adopted when designing GaN/Si amplifiers for space applications. On one hand, it is demonstrated how space thermal requirements limit device performance in case of GaN/Si technology, thus requiring larger peripheries for the same targeted output power. On the other hand, following a thermal load-pull approach, it is also demonstrated how, with proper selection of the load termination, GaN/Si technology is able to achieve competitive

TABLE IV
Performance of the 8x75 μm device at 36 GHz and 1 dB compression.

Feature	Value
V_{DS}	11.25 V
T_{BP}	80 °C
Γ_L	$0.82e^{j161°}$
P_{out}	32.6 dBm
T_j	160 °C
Gain	4.2 dB
PAE	47 %
Output mismatch	-13 dB

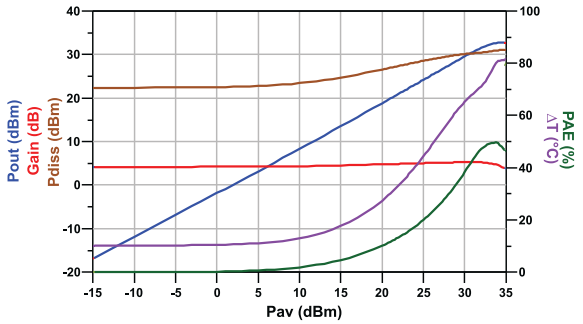


Fig. 8. Large-signal CW simulation results for the 8x75 μm device, $V_{DS} = 11.25$ V.

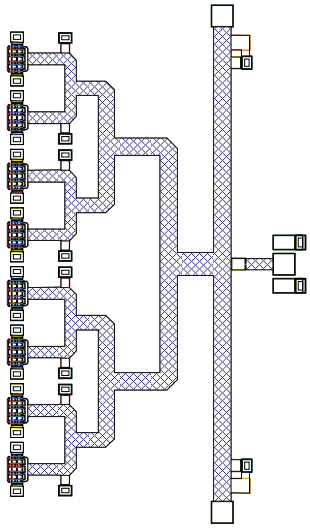


Fig. 9. Layout of the 8x8x75 μm final stage of the designed PA.

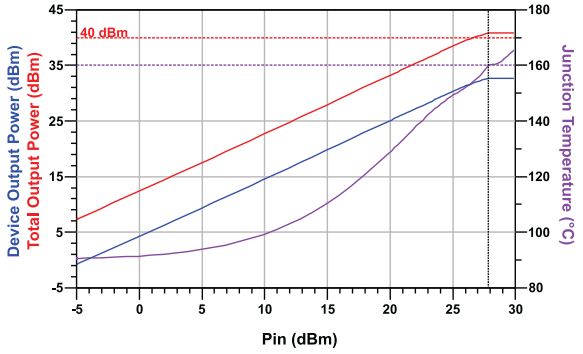


Fig. 10. Performance of the final stage of designed PA.

results at Ka-band also when enforcing space derating rules.

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