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Interfacial Charge Dynamics in Metal-Oxide–Semiconductor Structures: The Effect of Deep Traps and Acceptor Levels in GaN

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Using numerical simulations, we investigate the effects of deep traps and deep acceptor levels in magnesium-doped GaN on interface charges in the semiconductor-oxide interface. Specifically, in this work we address two open issues observed in experimental studies on GaN trench metal-oxide-semiconductor field-effect transistors. (i) We investigate the observed clockwise hysteresis in the transfer characteristics and elucidate the underlying physical mechanism causing it. By employing appropriate models for substitutional carbon at nitrogen sites (C_N) and nitrogen vacancies (V_N), we calculate the hysteresis dependence on the trap concentrations and the measurement sweep duration T_s . We show that C_N acceptor traps in p -GaN are likely responsible for this phenomenon and the largest hysteresis is predicted for a sweep duration of $T_s \approx 30$ s. (ii) We also address the apparent inconsistency between the experimental and theoretically predicted magnesium-ionization levels and the variations of the measured transfer characteristics, specifically the threshold voltage. We show that the bands bending in the channel area creates a layer in which magnesium is completely ionized. As a result, the magnesium partial ionization does not have an effect and, while the threshold voltage decreases, nor does the breakdown voltage, as observed experimentally. The measured threshold voltage, which is lower than the theoretically predicted value, is caused by fixed and trapped charges at the interface, in agreement with values reported in the literature.

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I. INTRODUCTION

Understanding the physics of semiconductor-oxide interfaces and their behavior under nonequilibrium is critical for the development of novel electronic devices. This is especially important for gallium-nitride- (GaN) based power devices that are expected to operate under more extreme conditions than their silicon counterparts. Among these, the gallium-nitride vertical-trench metal-oxide-semiconductor field-effect transistor (MOSFET) is a very appealing technology for power applications. It is naturally suitable for integration with high packing densities, leading to high absolute current switching capabilities. Using thick drift layers, high breakdown voltages can be attained, exceeding the rating of lateral transistor architectures. For device layers grown in the (0001) direction, the resulting gate trenches are on the m planes ($1\bar{1}00$), mitigating unwanted polarization effects. Fabricated vertical-trench GaN-MOS devices [1–5] have achieved high channel mobility [1] and low on-resistance

and threshold voltages (V_T) [6]. Using field plates, Oka *et al.* have fabricated a device with a high breakdown voltages of 1.6 kV [3] and, subsequently, an optimized structure with a hexagonal cell structure that has attained a breakdown voltage of 1.25 kV with specific on resistance of $1.8 \text{ m}\Omega \text{ cm}^2$ [4].

These successful efforts also expose important gaps in the understanding of the physics of the GaN-oxide interface and its impact on the device performance. An unexplained clockwise hysteresis in the gate transfer characteristics has been observed, both in the device fabricated by Oka ($\Delta V_G = 0.5$) [4] and in Li ($\Delta V_G = 0.6$ V) [5]. Moreover, the measured threshold voltages of all fabricated devices have turned out to be consistently lower than the theoretical values computed using a standard MOS model [7]. This trend has been consistent over different gate oxides and application methods, as presented in Table I. The observed low threshold has been attributed to [3,4] (i) insufficient activation of the magnesium impurities in the gate layer and (ii) the presence of fixed charges and/or nitrogen vacancies (V_N) on the gate trench surface. However, as stated by Oka *et al.* [4], a low magnesium activation would also have led to punch-through

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TABLE I. Measured and calculated values of the threshold voltage in actual devices, the observed hysteresis voltage ΔV_G , the gate-insulator composition, and its application method used for each structure. In [3,4] atomic layer deposition (ALD) was used to apply the gate oxide.

Ref.	V_T measured	V_T calculated	ΔV_G	Gate insulation
[1]	5.1/25.5	11.2–29	...	SiN/SiO ₂ , ECR/PECVD
[2]	10	44	...	SiN LPCVD
[3]	7	57	...	SiO ₂ ALD
[4]	3.5	33	0.5	SiO ₂ ALD
[5]	4.8 ^a		0.6	AlN/SiN MOCVD

^a V_{th} is calculated in this case as the gate voltage at which the drain current is 1000 times smaller than the “fully on” case, which seems to be an overestimate.

and breakdown at much lower drain-source voltages than observed, i.e., around 10 V. Other authors have attributed the observed low threshold voltage to the creation of an *n*-type region near the trench surface [1,2].

In this paper, we employ a physics-based numerical device-simulation model to investigate the impact of defects and dopants on the gate transfer characteristics of a prototype trench GaN-MOS devices. Specifically, we intend to address two main open questions: (i) What is the mechanism responsible for the observed clockwise hysteresis in the transfer characteristics? (ii) Can one explain the apparent contradiction between the predicted activated magnesium concentration in the *p*-gate layer and the measured threshold and breakdown voltages?

II. METHOD AND MODELS

A drift-diffusion model, as implemented in the TCAD SENTAURUS package [8], is used for this investigation. All simulations are performed at a constant temperature of 300 K. A two-dimensional structure, based on the cross section of the device fabricated by Oka *et al.* [4] is used as the geometrical device model for the simulations. Figures 1(a) and 1(b) show the device cross section and the gate area from the simulation. The structure’s layer thicknesses, doping type, and doping concentrations are presented in Table II. The gate insulator layer is 80-nm-thick SiO₂, deposited on the etched channel, as shown in Figs. 1(a) and 1(b). Silicon and magnesium are used as *n* and *p* impurity atoms, respectively. The geometrical model is designed to be consistent with a 12.6- μm -pitch hexagonal cell. The conduction channel thickness, as well as the areas affected by the phenomena studied in this work, are very thin compared to a gate section and are equal to a cell side length of 12.6 μm . Therefore, the effect of the cell corners is expected to be negligibly small, allowing accurate modeling of the device by its two-dimensional cross-section representation. Symmetry considerations and

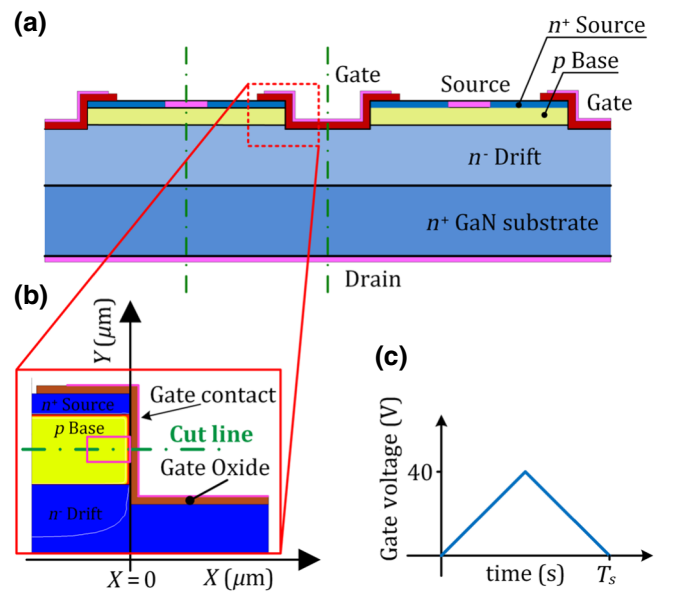


FIG. 1. (a) A schematic (not to scale) cross section of the simulated device structure, based on the actual device in Ref. [4]. (b) A detailed look at the device structure near the gate: the GaN/SiO₂ interface at $X = 0$ and the cut line that is used as the X axis in Figs. 3 and 7. (c) The gate-voltage sweep waveform used in the transient simulations.

a reduced substrate thickness are used to limit the numerical simulation requirements in terms of memory and execution time. The dark green dashed-dotted lines in Fig. 1(a) show the boundaries of the structure used in the simulation. Finally, the mesh on which the discretize equations are solved is optimized to properly capture the physical phenomena near the oxide-semiconductor interface and the channel area. The Arora [9] model is employed to account for the dependence of the mobility on doping. At high electric fields, the carriers’ velocity saturation is described by the Cauchy-Thomas and transferred-electron models [9], for holes and electrons respectively. The relevant fitting parameters for GaN, derived using numerical and experimental data, are obtained from Ref. [9]. The avalanche-generation model of Okuto and Crowell is used, with parameters from Ref. [10].

The magnesium-ionization energy, E_a , relative to the valance-band maximum (VBM), has been reported by

TABLE II. The simulated structure’s layer thicknesses, doping type, and doping concentrations.

Layer name	Type	Thickness (μm)	Concentration (cm^{-3})
Gate oxide	...	0.08	...
Source	<i>n</i>	0.2	6×10^{18}
Base	<i>p</i>	0.7	2×10^{18}
Drift	<i>n</i>	13	9×10^{15}
Substrate	<i>n</i>	3	10^{18}

several authors, with values ranging from 117 [11] to 380 meV [12]. In this work, we use values based on data and meta-analysis given by Brochen *et al.* [13], as follows. The concentration of ionized magnesium atoms, N_A , is calculated using the Fermi-Dirac distribution:

$$N_A = \frac{N_{A,0}}{1 + g \exp[(E_a - E_{F,p})/kT]}, \quad (1)$$

where g is the degeneracy factor ($g = 4$) and $N_{A,0}$ is the substitutional magnesium concentration. The effect of the doping concentration on the effective acceptor level E_a is given by [13–15]

$$E_a = E_{a,0} - \alpha N^{1/3}, \quad (2)$$

where N is the total doping concentration and $E_{a,0} = 0.245$ eV is the ionization energy of an isolated impurity center. The geometrical coefficient α , accounting for electrostatic effects, is calculated as follows [16]:

$$\alpha = \Gamma\left(\frac{2}{3}\right) \left(\frac{4\pi}{3}\right)^{1/3} \frac{q^2}{4\pi\epsilon_r\epsilon_0} = 3.3086 \times 10^{-8} \text{ eV cm}. \quad (3)$$

By iteratively solving Eqs. (1)–(3) and the Fermi energy level, the effective acceptor level and concentration of ionized magnesium atoms are calculated. Figure 2 shows the calculated results for a range of substitutional magnesium-atom concentrations. The Ionized magnesium concentration (left vertical axis) is shown by the blue dashed line and the effective ionization level above the VBM is shown

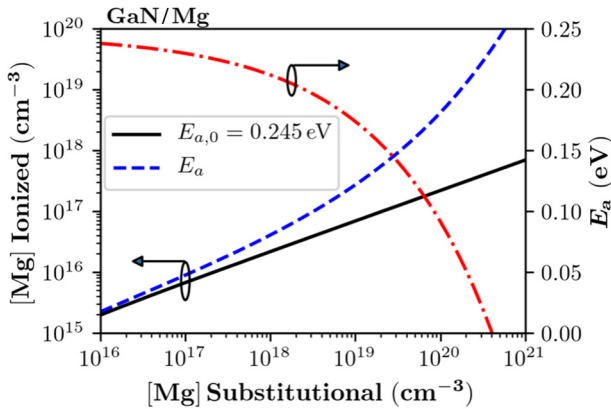


FIG. 2. The calculated magnesium-ionized concentration as a function of the concentration of substitutional atoms. The ionized concentration in the case of a constant acceptor level $E_a = 0.245$ eV is shown by the black solid line and the case including the ionization-level decrease due to the electrostatic interaction is shown by the blue dashed line. The red dashed-dotted line shows the dependence of the effective acceptor level (right vertical axis) on the doping concentration.

by the red dashed-dotted line (right vertical axis). Additionally, the (black) solid line represents the case of a constant energy level, $E_a = E_{a,0} = 0.245$ eV, which gives an underestimate for the magnesium-ionization level.

The simulation also takes into account traps, both donor and acceptor, that have been identified as being prevalent in GaN [12,17–19]. Nitrogen vacancies (V_N) are included as donor traps at 0.47 eV above the VBM [20], with a capture cross section of $\sigma = 1.3 \times 10^{-15} \text{ cm}^{-2}$ [21,22]. Carbon substitution at nitrogen sites (C_N) is modeled as acceptor traps at 0.9 eV above the VBM [17,18,23,24], with $\sigma = 2.5 \times 10^{-12} \text{ cm}^{-2}$ [25]. Carbon impurities are common in GaN grown in both metalorganic chemical-vapor deposition (MOCVD) and molecular-beam epitaxy (MBE) [19]. In the former, hydrocarbon fragments from the metalorganic precursor (trimethylgallium), which is used as the gallium source, are the main source of carbon contamination. Also, CO and CO₂ contaminants in NH₃, which is used as the nitrogen source, are also considered as culprits. In the case of MBE, impurities are adsorbed during air exposure in standard substrate-loading procedures. Fixed charges with several areal densities are introduced at the GaN/SiO₂ interface. The threshold voltage is extracted from the simulation results using the linear extrapolation method with a drain voltage of 0.5 V.

To analyze the observed gate transfer-characteristic hysteresis (ΔV_G), we study the time-dependent device behavior employing transient simulations. In practical transfer-characteristics measurements, hysteresis may be observed when sweeping the gate bias from zero to a given voltage and back. Therefore, transient simulations are performed with V_G increased linearly from zero to 40 V and back to zero with period T_s [see Fig. 1(c)]. The maximum value of V_G is chosen to be able to perform the numerical simulation under the same conditions as for the measurements. The hysteresis value, ΔV_G , is then extracted by finding $V_G[\max(g_m)]$ for the up and down sweeps, where g_m is the up-sweep curve transconductance.

III. RESULTS AND DISCUSSION

The semiconductor band bending near the interface at the metal-insulator-semiconductor system is controlled by the Poisson equation and affected by the metal work function and the charge balance across the insulator-semiconductor interface. These charges are usually classified as interface traps, trapped charges, oxide-trapped charges, and mobile ionic charges. These are balanced by the space-charge region created at the semiconductor side by the band bending [26]. We investigate first the effect of fixed charges, located at the GaN/SiO₂ interface, on the threshold voltage. We compute the transfer characteristic for a number of areal charge densities and find that the measured value of $V_T = 3.5$ V [4] corresponds to a fixed-charge density of $[Q_f] = 7.52 \times 10^{12} \text{ cm}^{-2}$. Furthermore,

V_T decreases rapidly with increasing areal densities. This result is consistent with experimentally measured values of $[Q_f]$ in p -type GaN/SiO₂ interfaces [27–29]. It should be noted that GaN/SiO₂ interface characterization is typically performed on c -plane interfaces and not m -plane interfaces, as is the case for the device being studied. Obviously, these values are sensitive to process parameters, and controlling $[Q_f]$ requires further experimental research.

When simulating data obtained by measuring I - V curves, one usually assumes steady-state conditions. However, although relatively slow (in the order of a few seconds), these results are actually transient and time-dependent in nature. Therefore, the transfer-characteristic hysteresis is considered next by introducing trap states, either C_N or V_N in the p -gate layer, and performing transient simulations to investigate the capture and emission dynamics of traps. Both in the case of C_N and V_N , increasing the gate voltage causes a downward bending of the energy bands, resulting in a wider region in which the Fermi energy is higher than the trap energy (see Fig. 3). Acceptor traps in p -type material, C_N in our case, are neutral in the bulk and become negatively ionized by electron capturing due to the band bending [see Fig. 3(a)]. For donors (V_N), the opposite occurs; they are positively ionized in the bulk and become neutral by electron capture, due to band bending [Fig. 3(b)]. As a result, increasing the band bending increases the negative charge (C_N^-) or decreases the positive one (V_N^+), as shown by the shaded areas in Fig. 3. The capture rate for conduction-band electrons by C_N traps is given by

$$r_n^c = n[C_N](1 - f_{FD}(Et))\sigma v_{th}, \quad (4)$$

where n is the electron density, f_{FD} is the Fermi-Dirac distribution, and v_{th} is the thermal velocity. As the bands are bent by the gate voltage, more electrons become available for trapping and thus the duration of the capturing process is controlled by the concentration of empty traps: $[C_N](1 - f_{FD})$ and the capture cross section (σ). Due to their smaller cross section and the fact that the change in charge distribution occur farther away from the interface, V_N traps do not induce hysteresis. Figure 4 shows the hysteresis, ΔV_G , calculated from transient simulations, for sweep durations ranging from 10^{-2} to 10^3 s. A baseline curve with $[C_N] = 10^{18}$ cm⁻³ and physical-parameter values from the literature (mentioned above) is shown by the black solid line and round markers. In this case, $\Delta V_G \gtrsim 0.5$ V is obtained, in good agreement with the experimental data. This value is obtained at $T_s \sim 30$ s, which is a reasonable sweep time for such a measurement. Reducing $[C_N]$ decreases ΔV_G (Fig. 4, green plus markers) and no hysteresis is present when no C_N traps are included. Since the additional trapped charges stored by (C_N^-) increase the threshold voltage (in the steady state), $[Q_f]$ is adjusted in order to obtain the experimentally obtained V_T . For $[C_N] =$

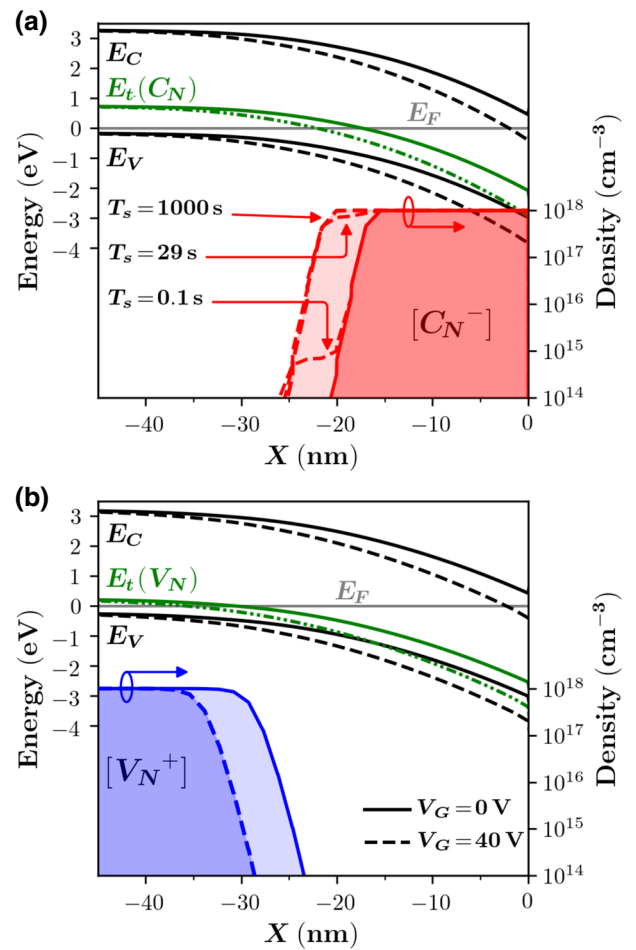


FIG. 3. Calculated C_N (a) and V_N (b) ionization profiles as a function of the gate voltage and the band bending near the GaN/SiO₂ interface ($X = 0$), along the cut line shown in Fig. 1(b). In the cases shown, $[C_N]$ or $[V_N] = 10^{18}$ cm⁻³. Zero gate voltage is shown by the solid lines and 40 V by the dashed lines. The light shaded area shows the space-charge difference between the two biases. In (a), the $[C_N^-]$ profile at 40 V (at $t = T_s/2$) is also shown for different sweep times, T_s (in s).

5×10^{17} and 10^{18} cm⁻³, $[Q_f]$ is set to 8.3×10^{12} and 9×10^{12} cm⁻², respectively. Additionally, Fig. 4 shows the sensitivity of ΔV_G to the C_N trap level $E_t \pm 0.05$ eV, σ , and $[C_N]$. Higher E_t (dashed-dotted red line and diamond markers) or lower σ (dashed line and blue triangle markers) both reduce the capture rate, resulting in an increased time delay between the band bending and subsequent occupation of all traps. Therefore, the curve is shifted toward longer sweep times and vice versa for a lower trap level (red dashed-dotted line and square markers). In order to understand the resonancelike behavior of the hysteresis magnitude with the sweep duration, we analyze the time evolution of the ionized traps C_N^- near the interface. The predefined area used for the integration is marked by the

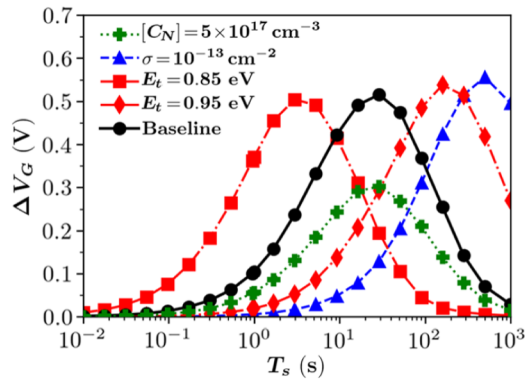


FIG. 4. The calculated hysteresis voltage ΔV_G as a function of the sweep time T_s . For the baseline case (black round markers), the largest hysteresis value > 0.5 V is obtained for $T_s \sim 30$ s. The effect of different E_t values is shown by the red curves. Decreasing (square markers) or increasing (diamond markers) E_t by 0.05 eV shifts the curve by nearly an order of magnitude. The green curve (cross markers) shows the effect of halving $[C_N]$, which correspondingly reduces ΔV_G ($[Q_f]$ is adjusted to maintain the V_T value). Finally, decreasing the capture cross section σ (blue triangle markers) correspondingly increases the trap lifetime and right shifts the curve.

magenta rectangle in Fig. 1(b). The results are then normalized with respect to the p-Base layer thickness. In Fig. 5, the results from simulations with baseline parameters are presented for three representative cases, $T_s = 0.1$, 29, and 1000 s. When the gate voltage is swept much faster than the trap capture rate (blue dashed-dotted line $T_s = 0.1$ s), hardly any traps are filled and no hysteresis is observed. On the other hand, for an extremely slow sweep (green solid line, $T_s = 1000$ s) the trap-filling time is negligibly small and the trap occupation follows the gate bias. Consequently, the number of charged traps in the up and down sweeps is equal and no hysteresis is observed. The maximal hysteresis occurs when the sweep duration is double that of the trap charging (red dashed line $T_s = 29$ s). Subsequently, during the down sweep, the charges in $[C_N^-]$ are stored until the bands return to their initial ($V_G = 0$) state and the trapped electrons are released. Thus, the difference in trap occupation between up and down sweeps is maximal. We conclude that the observed clockwise hysteresis is likely caused by the trapping time, in the order of a few seconds, of C_N^- acceptorlike traps. Our results indicate that reducing $[C_N]$ by approximately an order of magnitude will eliminate the observed hysteresis in the transistor transfer characteristics.

Lastly, we investigate the effect of magnesium partial ionization in the p -type gate layer. For a magnesium concentration (N_A) of $2 \times 10^{18} \text{ cm}^{-3}$ and an effective acceptor activation energy of $E_A = 0.2$ eV above the VBM, the bulk Fermi level is computed to be 50 meV below the acceptor level and the ionized magnesium concentration

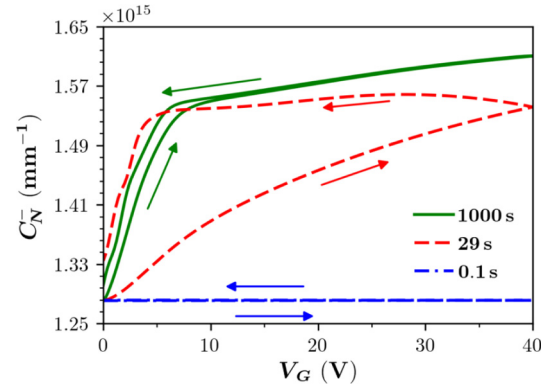


FIG. 5. The calculated time dependence of the ionized traps integrated over the channel area for the baseline case and three values of $T_s = 0.1$ (blue dashed-dotted line), 29 (red dashed line), and 1000 s (green solid line).

is $6.8 \times 10^{16} \text{ cm}^{-3}$ or 3.4%. However, for a device in which the Fermi level changes with the position and the gate applied bias, an assumption of complete and incomplete ionization leads to a different outcome. As shown in Fig. 6, the effect of including the model for incomplete magnesium ionization is much smaller than actually reducing the layer doping, as one would do by considering the bulk value in the case of partial ionization. In fact, for $N_A = 2 \times 10^{18} \text{ cm}^{-3}$, the calculated V_T is 32 and 31.4 V when assuming complete and position-dependent incomplete magnesium ionization, respectively. If one simply uses a constant-bulk incomplete-ionization value of $N_A = 6.8 \times 10^{16} \text{ cm}^{-3}$ throughout the layer, V_T is reduced to 5.9 V. No interface fixed charges are included in these calculations.

Finally, Fig. 7 shows the calculated energy-band profile near the GaN/SiO₂ interface and its effect on the magnesium-ionization level. Similarly to the case of acceptor traps, a layer of fully ionized magnesium is

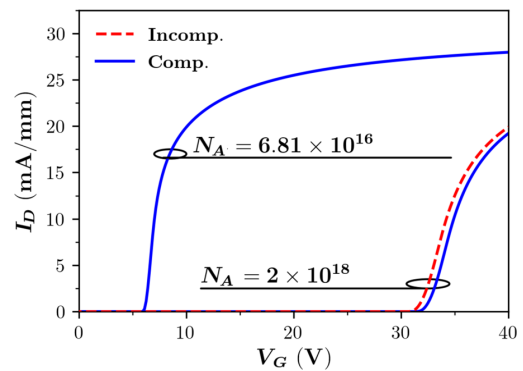


FIG. 6. The calculated transfer characteristics with $N_A = 2 \times 10^{18}$ and $6.8 \times 10^{16} \text{ cm}^{-3}$. The blue solid lines are obtained assuming complete magnesium ionization and the red dashed line is for incomplete ionization.

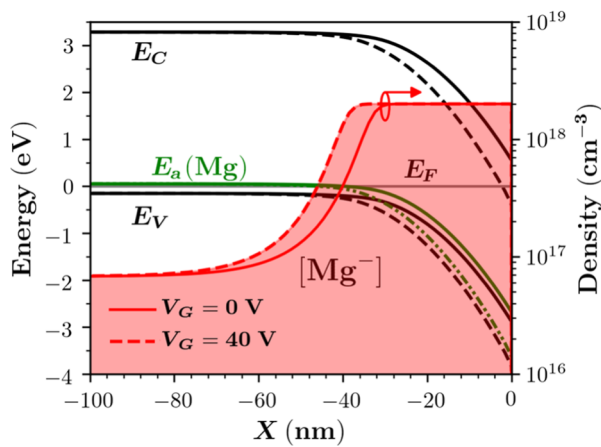


FIG. 7. The calculated magnesium ionization (red regions) near the GaN/SiO₂ interface ($X = 0$) and along the cut line [see Fig. 1(b)] for $V_G = 0$ (solid line) and for $V_G = 40$ V (dashed red line).

created near the interface due to the downward band bending. This layer thickness is approximately 32 nm when the gate voltage is zero and 38 nm at $V_g = 40$ V, which is much thicker than the width of the conduction channel. The presence of this fully ionized region prevents incomplete magnesium ionization from impacting the device transfer characteristics. This study demonstrates the direct use of first-principle calculations to infer macroscopic device behavior. Using knowledge gained, at the atomistic level, from defect studies based on density-functional theory and macroscopic device-simulation models, the charge dynamics at the GaN/SiO₂ interface are investigated. The physics that is responsible for the observed hysteresis clearly emerges from our analysis. Finally, the microscopic physics of the magnesium acceptor ionization is shown not to affect the threshold voltage.

IV. CONCLUSION

In conclusion, using a numerical approach, we investigate the hysteresis effect observed in GaN trench MOS devices and the influence of gate-oxide fixed charges and incomplete magnesium ionization on its transfer characteristic. From analysis of the time-dependent simulation results, we infer that the relatively slow trapping process of C_N is likely responsible for the observed clockwise hysteresis. Hence, purifying the material from such slow acceptor traps will eliminate the observed hysteresis. Based on the C_N trap energy level and the capture cross section, we estimate that the electron-capture process by these sites has a time constant of a few seconds. This causes the trapped-charge dynamics to lag behind the gate-voltage time variation. The presented calculation predicts that maximum hysteresis occurs for a sweep duration

of approximately 30 s. The contribution of the V_N sites to the hysteresis is found to be negligible.

The second issue we address is the inconsistency between the low magnesium ionization in p -GaN bulk, 3.4% for $[\text{Mg}] = 2 \times 10^{18} \text{ cm}^{-3}$, and the observed transfer and breakdown properties in actual devices. We show that, due to the band bending at the GaN/SiO₂ interface, a layer of fully ionized magnesium is created. This layer inhibits the expected effect of the low doping density in the channel resulting from low magnesium ionization.

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