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A Unified Design Theory for Class-E Resonant DC–DC Converter Topologies

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ABSTRACT Resonant and quasi-resonant dc–dc converters have been introduced to increase the operating frequency of switching power converters, with advantages in terms of performance, cost, and/or size. In this paper, we focus on class-E resonant topologies, and we show that about twenty different architectures proposed in the last three decades can be reduced to two basic topologies, allowing the extension to all these resonant converters of an exact and straightforward design procedure that has been recently proposed. This represents an important breakthrough with respect to the state of the art, where class-E circuit analysis is always based on strong simplifying assumptions, and the final circuit design is achieved by means of numerical simulations. The potentialities of the proposed exact methodology are highlighted by realistic circuit-level simulations, where the desired waveforms are obtained in one single step without the need of a time-consuming iterative trial-and-error process.

INDEX TERMS Circuit theory, class-E converters, resonant dc-dc converters.

I. INTRODUCTION

Resonant and quasi-resonant dc-dc converters have been introduced with the aim of reducing switching loss impact at high frequencies. This allows a converter to operate with good efficiency at high frequency ranges (up to the VHF range 30 – 300MHz) thus increasing the system power density [1]–[7]. A higher switching frequency, in fact, paves the way to both size and cost reduction, as well as improved dynamic performance [2].

In this paper we focus on the Class-E converters [2], [5] that are based on the so-called *soft switching* technique and that are specifically designed to overcome the main drawback of conventional class-D (*hard-switching*) topologies given by the frequency dependent loss mechanisms. The soft switching technique has been proposed, to the best of authors' knowledge, by Sokal *et al.* in [1] as a way to improve performance in RF amplifiers [1], [2], [8]. The main concept is the introduction of additional reactive components in order to properly shape voltage and current waveforms. The advantage is to lower (ideally, down to zero) the switching losses [7], [8] with beneficial effects also in terms of reducing EMI emission [7], [9] without the need of additional techniques like spread-spectrum clocking that are becoming popular for class-D converters [9]–[13].

In details, class-E dc-dc converters can be seen as composed of the cascade of a class-E inverter [1], [7], [8], [14] and a class-E rectifier [7], [15], both relying on a soft-switching approach. Sometimes they are called E^2 converters [16]–[18] to distinguish them from converters relaying, as an example, upon a class-E inverter and a class-D rectifier [7]. Soft switching is achieved by ensuring that the voltage (or current) waveform of the controlled switch (in the inverter) and the uncontrolled one (in the rectifier) is smooth. Focusing on the inverter, we refer to *Zero-Voltage Switching (ZVS)* when the voltage across the main switching device is slowly increasing from zero after its turn-OFF instant, and slowly going to zero immediately before its turn-ON instant. Additionally, we refer to *Zero-Voltage-Derivative Switching (ZVDS)* if the voltage is approaching the zero level with zero-time-derivative. *Zero-Current Switching (ZCS)* and *Zero-Current-Derivative Switching (ZCDS)* are referred to

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the current flowing into the main switch device. The same definitions can be applied to the rectifier, even if some authors prefer to indicate these conditions as *low* dv/dt and *low* di/dt [7], [19], [20].

Historically, the soft switching technique is known since many years [1], and the application to dc-dc resonant converters has been first introduced in the early '80s [2]. Nevertheless, the topic is still receiving attention in the Literature [18], [21]–[23]. Due to better performance, all recent papers are focused on the ZVS approach [7], [24]. A few of these works are also focusing on the proposal of new topologies aiming to improve efficiency or reduce device stress [25], [26]. Almost all of these contributions are interested in improving the converter control [27], [28] or the design methodology [14], [18], [25], [27], [29] in already known topologies.

This paper belong to the latter group, i.e., it aims at improving the state of the art in class-E converter design. In particular, we consider the exact and semi-analytic design methodology proposed in [29]. This represents an important step in class-E converters design theory with respect to state-of-the-art alternative methodologies which are based on the sinusoidal approximation typical of RF circuit design and on the subsequent refinement by means of additional, time-consuming SPICE simulations. With respect to [29], we make two important additional steps. First, we improve the methodology by simplifying the approach and by generalizing it, covering two different topologies, both featuring galvanic isolation. Then, we show that these two topologies are actually representative for a large number of class-E dc-dc converters, either isolated or non-isolated. The similarity between the design approaches for many resonant topologies has been already observed in many works, as for example in [19]. The contribution of this work is to show that the innovative design methodology considered here can be actually ***applied as is*** to a number of different converters regardless of the actual circuit topology.

The paper is organized as follows. After a brief review of the class-E state-of-the-art (Section II), we present in Section III the two isolated class-E topologies that are referred to as *canonical* ones in this paper. The exact semi analytic design methodology is also provided. In Section IV the most commonly used non-isolated class-E topologies are presented and related to the canonical ones, showing that all of them share the same design equations (and so the design methodology). The approach is validated by means of realistic SPICE simulations that take into account many possible circuit non-idealities. Finally, we draw the conclusion.

II. STATE-OF-THE-ART

One of the first class-E dc-dc converter proposed in the literature is that depicted in Figure 1 and proposed by Kazimierczuk *et. al.* in [5]. In the schematic, the distinction between the class-E inverter and rectifier stages, connected by means of a properly designed band-pass LC filter, is clearly visible.

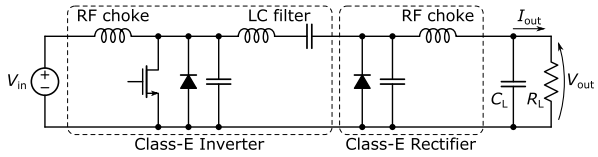


FIGURE 1. Basic schematic of the class-E dc-dc converter proposed by Kazimierczuk *et al.* in [5].

The aim of [5] is to propose a design methodology to achieve ZVS and ZVDS at the MOS switch (ZVS at the diode, or low dv/dt, is always ensured in this topology), realizing the so-called *Optimal Class-E Operation* [8]. Indeed, due to the non-linearity and to the many reactive elements, the design procedure is quite complex and based on the well-known approximations used in RF circuits [1], [2]. In [5], the inverter design is achieved by assuming that *the rectifier is a linear circuit* with a given impedance. Then, the rectifier design is achieved by assuming that *it is driven by an ideal sinusoidal current source* at the same frequency f_s at which the MOS switch is turned ON and OFF. The purpose of the (high loaded quality factor) LC filter is to support these two assumptions and ensure adherence between the actual waveforms and the expected ones. Two large RF choke inductors are also employed to ensure the two additional assumptions of a constant current power source and a constant current load, that further simplify the converter analysis.

With these assumptions, a fully analytic model for the behavior of the converter can be readily obtained, and used to ensure the desired optimal class-E operation. Note that the behavior of resonant converters depends also on the load resistance or on the output current (R_L and I_{out} in Figure 1). In other words, ZVS and ZVDS can be achieved *only for a given operating condition* defined by a value of R_L or I_{out}. Coping with a variable load, or either with a non-precisely known V_{in}, is a complex task and requires a feedback such as a frequency control [2], [30] or an ON-OFF control [27], [31]. As an example, in [5], the converter is designed to achieve the optimal behavior at the maximum output power. At a lighter load, the switching frequency is increased to maintain the same output voltage, but the converter operates under sub-optimum class-E conditions: in fact, the diode antiparallel to the MOS switch turns ON before the MOS is turned ON, thus ensuring ZVS operation, but ZVDS is not achieved anymore. Note that the antiparallel diode, in most of the cases, is just the parasitic body diode present in any discrete MOS, and does not turn ON when the optimal class-E condition is achieved. For the sake of simplicity, even if present as a parasitic device, we will not include the antiparallel diode anymore in the next schematics.

In this work we are interested in methodology ensuring ZVS and ZVDS for a specific operating condition, and we consider control methodologies to be out of scope. Once the class-E design is achieved (for an operating condition that could be, as in the above example, the one ensuring the maximum output power), it is always possible to apply any of the control methodologies presented in the literature.

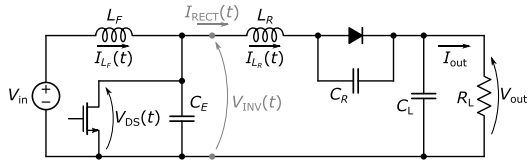


FIGURE 2. Schematic of the class-E boost converter proposed in [27].

So, in the following we will always assume that V_{in} and R_L, or I_{out}, are known and fixed.

The most recent efforts in class-E resonant converter design aimed at removing bulky elements such as the input RF choke inductor and the high-Q LC filter, or replacing them with smaller resonant counterparts. In this way, the converter component count is reduced, enabling overall size and cost reduction. As a consequence, the design methodology has been improved, and more complex design approaches has been proposed in the Literature to cope with the fact that using the sinusoidal approximation without any circuital solution supporting it, would lead to an increased difference between expected and actual waveforms.

To better explain the above considerations, let us consider a numerical example relying on the approach proposed in [27], that is one of the most advanced among those based on the sinusoidal approximation. The design approach has been developed for the boost converter of Figure 2, that can been directly obtained by that of Figure 1 by removing the LC filter, replacing the RF choke inductors with smaller resonant ones, and re-arranging the position of the elements in the rectifier. The analysis of the converter in [27] is based on the observation that the MOS and the diode are non-linear. Due to this, and even considering them as two ideal switching devices, i.e., either equivalent to an open circuit when in the OFF state or to a short circuit in the ON state, there are four different circuit configurations possible to be considered. Additionally, since the converter contains four reactive elements (L_F, C_E, L_R and C_R), the comprehensive mathematical description of the circuit requires four sets of fourth-order differential equations. This is further complicated by the fact that the switching instants of the diode are unknown. According to [27], deriving a complete set of closed-form equations to directly describe the converter is a "cumbersome and unfruitful task".

To cope with this, and following the original notation, the analysis starts from the assumption that the rectifier current is sinusoidal:

$$I_{\text{RECT}}(t) = I_{\text{AC}} \sin(2\pi f_s t + \phi_1) + \frac{P_{\text{out}}}{V_{\text{out}}} \tag{1}$$

Given this assumption, the system describing the inverter circuit evolution can be solved using the five unknown quantities $\omega_0 = 1/\sqrt{L_F C_E}$, $Z_0 = \sqrt{L_F/C_E}$, I_{AC}, ϕ_1 and $I_{L_F}(0)$, defined as the current in L_F at the reference time $t = 0$. By setting the three constraints: *i*) the inverter efficiency is 1, *ii*) the average voltage across L_F in one period is 0, *iii*) the average current through C_E in one period is 0, it is possible to get a non-linear system of three equations that, once numerically solved, gives the optimal values of Z_0, I_{AC} and $I_{L_F}(0)$ when the choice of the two degrees of freedom ω_0 and ϕ_1 has been made, and the design constraints V_{in}, V_{out}, P_{out} and f_s are known. Note that conditions *ii*) and *iii*) ensure both steady-state behavior and ZVS.[1] ZVDS is not considered at this step, but investigated later through the correct choice of the two degrees of freedom.

Once the design of the inverter is obtained, one can get the rectifier design starting on the assumption that its input voltage is sinusoidal and expressed as

$$V_{\text{INV}}(t) = V_{\text{AC}} \sin(2\pi f_s + \phi) + V_{\text{in}}$$

where V_{AC} and ϕ are computed from the inverter analysis as the amplitude and the phase of the first harmonic of the voltage $V_{DS}(t)$ across the MOS. The analysis is based on four unknown quantities: the time instants t_{ON} and t_{OFF} when the diode turn ON and OFF, respectively, $\omega_r = \sqrt{L_R C_R}$, and $Z_r = \sqrt{L_R/C_R}$. Similarly to the inverter case, these unknowns can be achieved by numerically solving the non-linear system one gets by considering the four constraints: *i*) the rectifier efficiency is 1, *ii*) the average voltage across L_R in one period is 0, *iii*) the average current through C_R in one period is 0, *iv*) the phase of the fundamental component of $I_{L_R}(t)$ is ϕ_1, as constrained by (1).

The entire procedure is semi-analytic: all waveforms are expressed in a closed form (even if some coefficients, such as V_{AC} and ϕ, are numerically obtained), but are linked via a system of non-linear equations that needs to be solved numerically. As an example, even if the authors of [27] does not provide any numerical example from applying the proposed methodology,[2] one can follows the described methodology and assume $V_{\text{in}} = 12\,\text{V}$, $V_{\text{out}} = 30\,\text{V}$, $P_{\text{out}} = 7\,\text{W}$, $f_s = 75\,\text{MHz}$. By setting $\omega_0 = 0.6 \cdot 2\pi f_s$, ZVDS is ensured for $\phi_1 = -0.5\,\text{rad}$. With this, the obtained numerical solution is $L_F = 594\,\text{nH}$, $C_E = 21.0\,\text{pF}$, $L_R = 134\,\text{nH}$, $C_R = 23.5\,\text{pF}$. These values are aligned with the ones that can be inferred by looking at the design curves in [27].

However, since the sinusoidal approximation is not supported anymore by a band-pass filter, the achieved solution requires to be refined by means of circuital simulation to perfectly fit the desired behavior. Figure 3 compares the achieved waveform of the voltage $V_{DS}(t)$ across the MOS (dashed line) obtained from a SPICE simulation using ideal models for all devices (including MOS and diode), with the desired one featuring ZVS and ZVDS (solid line) obtained when the rectifier is replaced by the current generator assumed in (1). The difference is remarkable, and also present in the output power, that settles to 7.6 W. We want also to stress that the design methodology does not take into account any non-idealities. As an example, if we consider that L_F and L_R are lossy inductors with, say, a quality factor $Q_L = 100$,

[1] Since for any ideal capacitor $I(t) = CdV(t)/dt$, and considering that the voltage $V(t)$ across the C_E at the beginning and at the end of one clock period is constrained to 0 by the MOS, the average value of $I(t)$ is 0 only if $V(t)$ has no discontinuities, including at the MOS turn ON instant.

[2] The only example proposed in [27] is already refined by SPICE simulation, and no design without refinement is provided.

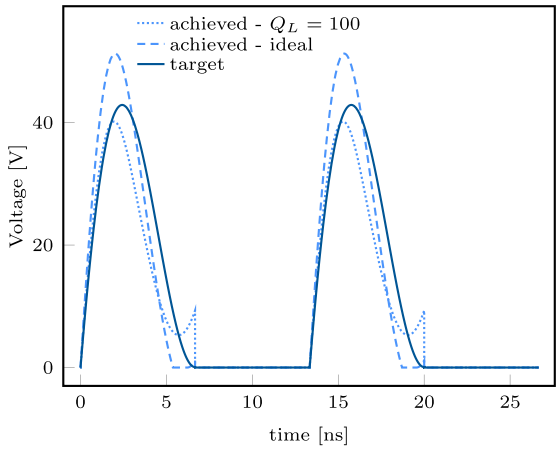


FIGURE 3. Comparison between the desired and the achieved shape of the $V_{DS}(t)$ waveform for the converter of Figure 2 using the procedure proposed in [27].

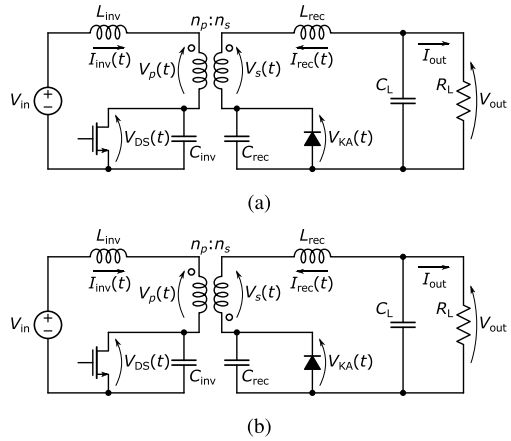


FIGURE 4. Schematic of the canonical isolated class-E converter topologies considered in the paper. (a): in-phase coupling. (b): 180° out-of-phase coupling.

the observed $V_{DS}(t)$ is given by the dotted line of Figure 3, and the power delivered to the load drops to 5.9 W. From this example, it is clear that the procedure proposed in [27] can be effectively used only to get a reasonable starting point in the converter design, and that a refinement of the solution based on lengthy simulations is essential.

A major step forward in the design of class-E dc-dc converters has been made by Bertoni *et al.* in [29]. Authors proposed a suitable way to derive the complete set of closed-form equations that directly describe the converter evolution. As in [27], the entire procedure is semi-analytic, since the design is achieved as the numerical solution of a system of non-linear equations. However, the procedure introduces minor approximations only, and does not need any further refinement. Furthermore, major sources of non-idealities can be taken into account. The procedure is also dimensionless, and so independent of V_{OUT}, P_{OUT} and f_s.

Starting from [29], we show in the following that the design methodology proposed there can be actually extended to a large class of resonant dc-dc converter topologies appeared in the literature in the last three decades. This allows us to propose a more general class-E converter design methodology that, with respect to any solution based on the sinusoidal approximation such as [27], presents three main advantages: *i*) it is dimensionless, i.e., can be applied regardless of the value, for example, of P_{OUT} and f_s, *ii*) can be applied to many different converter regardless of the actual topology, *iii*) can take into account of the main sources of non-idealities.

III. CLASS-E ISOLATED TOPOLOGIES

A. CANONICAL ISOLATED TOPOLOGIES

The two basic resonant converter topologies we will consider are shown in Figure 4. Both topologies consist of two meshes (the inverter and the rectifier one), coupled by means of a transformer to provide galvanic isolation. The inverter has a MOS switch that is externally turned ON and OFF at frequency f_s with duty-cycle D, while the rectifier embeds a diode as a non-controlled switch. The only difference between the two topologies is the coupling method: in the converter of Figure 4(a) the coupling is in-phase, while in that of Figure 4(b) there is a 180° out-of-phase coupling.

Both schematics feature all the characteristics of a class-E converter, as that of Figures 1 and 2. The two capacitors C_{inv} and C_{rec} are placed in parallel with the MOS switch and the diode, respectively, to ensure smooth waveforms. Furthermore, C_{inv} and C_{rec} can also embed the parasitic capacitance of the two switches and, as long as the actual capacitances are much larger with respect to the parasitic ones, can mask both the non-linearity and the non-perfect knowledge of the latter. This ensures that the parasitic of the two switches do not significantly alter the circuit behavior. The inductors L_{inv} and L_{rec} can also embed (or mask) the leakage inductance of the transformer. Along with C_{inv} and C_{rec}, they also set the two resonant frequencies of the inverter and of rectifier meshes, respectively. Note that, since the transformer can be actually seen as an additional (coupled) inductor, and since only two inductances are actually necessary along with the two capacitances to set the resonance properties, one among L_{inv} and L_{rec} can be removed from the circuit. This will become clearer in the next section. To further improve the design approach in [29], we include both the schemes of Figure 4 in the proposed analysis for the maximum generality and flexibility.

The evolution, obtained by means of SPICE simulation, of the considered circuits when designed to achieve optimal class-E operation (i.e., ZVS and ZVDS) is shown in Figure 5(a) for the in-phase coupled and in Figure 5(b) for the 180° out-of-phase coupled circuit. The figures show the most important voltage and current signals of the circuit, i.e., $V_{DS}(t)$ across the MOS switch, $V_{KA}(t)$ across the diode, $I_{\mathrm{inv}}(t)$ flowing into the inverter mesh, $I_{\mathrm{rec}}(t)$ of the rectifier mesh, and the transformer magnetizing current defined as $I_{\mathrm{m}}(t) = I_{\mathrm{inv}}(t) + I_{\mathrm{rec}}(t)$ for the in-phase coupling and $I_{\mathrm{m}}(t) = I_{\mathrm{inv}}(t) - I_{\mathrm{rec}}(t)$ for the 180° out-of-phase coupling. In both cases the $V_{DS}(t)$ mildly reaches the zero level, at the MOS

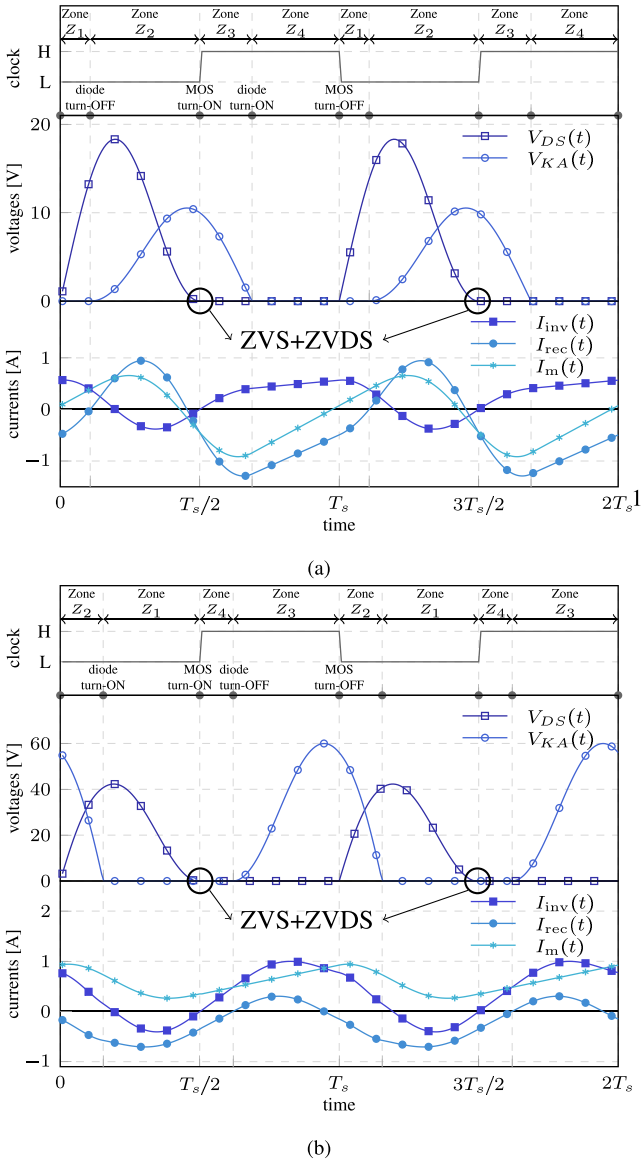


FIGURE 5. Resonant class-E converter typical voltage and current waveforms. (a): In-phase coupling ($\Phi = +1$). (b): 180° out-of-phase coupling ($\Phi = -1$).

turn-ON instants (that are, in the figure, $t = T_s/2$ and $t = 3\ T_s/2$, with $T_s = 1/f_s$ is the clock period length). The most remarkable difference between the two evolutions is that $V_{KA}(t)$ is lagging $V_{DS}(t)$ in Figure 5(a), and leading it in Figure 5(b).

The two circuits are not new and, actually, each one represents more a class of dc-dc converters than a single circuit. For example, it is clear that changing the order of the elements in a mesh does not alter the overall behavior: the rectifier of Figure 6 is perfectly equivalent to that of Figure 4(b).. We refer to the two topologies in Figure 4 as *canonical* ones for the two identified classes.

The 180° out-of-phase coupling configuration is sometimes referred to as the class-E fly-back, due to similarities with the commonly used class-D (i.e., hard-switched) fly-back converter that can be simply obtained from that of

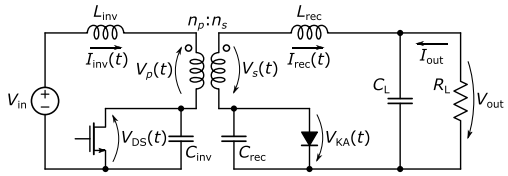


FIGURE 6. Alternative implementation of the inverter loop for the 180° out-of-phase coupling of Figure 4(b).

Figure 4(b). once resonant elements $L_{\rm inv}$, $L_{\rm rec}$, $C_{\rm inv}$ and $C_{\rm rec}$ are removed.

By introducing the schematics of Figure 4, we aim to:

- enhance the design methodology provided in [29], by considering a more general approach. Here, both $L_{\rm inv}$ and $L_{\rm rec}$ are explicitly taken into account, and both the in-phase coupling and the 180° out-of-phase coupling for the transformer are considered;
- show that the 180° out-of-phase coupling converter has similarities with a lot of other resonant (or quasi-resonant) circuits proposed in the last three decades, each one presented with a different analysis and design methodology. All of them could be actually designed by applying the approach proposed here.

For example, in [32] a ZVS fly-back with 180° out-of-phase coupling, more precisely with the coupling as in Figure 6 but without $L_{\rm rec}$ is considered. In [33] some different ZVS converter topologies are analyzed and compared, including that of Figure 4(b) in both configurations where either $L_{\rm inv}$ or $L_{\rm rec}$ is removed. In [34] an analysis of an isolated buck/boost converter with 180° out-of-phase coupling without $L_{\rm rec}$ is provided. In [35] a circuit composed by two interleaved ZVS fly-back circuits as that of Figure 4(b), again without $L_{\rm rec}$, are considered and analyzed.

B. CIRCUITS ANALYSIS

The aim of this section is to describe and enhance the innovative design methodology proposed in [29]. More precisely, while trying to keep the notation as close as possible with respect to the original paper, we introduce a major change in the transformer model. This allows us to simplify the analysis, since considering the equivalent circuit to the primary side is not necessary anymore, and also to cope both with in-phase and with the 180° out-of-phase coupling methods of Figure 4 using a single equations set.

For the sake of simplicity, we neglect at this time all circuit losses, and take them into account only in Section III-D. We consider active devices (the MOS switch and the diode) as ideal switches, i.e., equivalent either to a short circuit or to an open circuit depending on their ON/OFF state. All passive elements are considered ideal, with an infinite quality factor.

In [29], the equivalent circuit at the primary side of the transformer is considered by scaling all elements at the secondary side using the turns ratio n_p/n_s. Instead of using this model (defined by the parameters n_p/n_s, the coupling coefficient k and the total inductance at the primary side L_p), we adopt here the coupled inductors model where, referring

to Figure 4, the two transformer voltages can be written in matrix form as

$$\begin{pmatrix} V_p(t) \\ V_s(t) \end{pmatrix} = \begin{pmatrix} L_p & \Phi M \\ \Phi M & L_s \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_{\text{inv}}(t) \\ I_{\text{rec}}(t) \end{pmatrix} \tag{2}$$

where $\Phi = \pm 1$ is the coupling constant, equal to $+1$ for in-phase coupling and -1 for 180° out-of-phase coupling, M is the mutual inductance, and L_p and L_s represent the inductance at the primary and secondary side, respectively. Switching between the two models is possible by considering that $k = M/\sqrt{L_p L_s}$ and $n_p/n_s = \sqrt{L_p/L_s}$.

This alternative notation allows a quite simply analysis of the converter. The Kirchhoff voltage laws at the inverter and rectifier meshes are written as

$$V_{\text{in}} = (L_{\text{inv}} + L_p)\frac{dI_{\text{inv}}(t)}{dt} + \Phi M \frac{dI_{\text{rec}}(t)}{dt} + V_{DS}(t) \tag{3a}$$

$$V_{\text{out}} = \Phi M \frac{dI_{\text{inv}}(t)}{dt} + (L_{\text{rec}} + L_s)\frac{dI_{\text{rec}}(t)}{dt} + V_{KA}(t) \tag{3b}$$

that, by defining $I_{\text{m}}(t) = I_{\text{inv}}(t) + \Phi I_{\text{rec}}(t)$, can also be rewritten as

$$V_{\text{in}} = (L_{\text{inv}} + L_p - M)\frac{dI_{\text{inv}}(t)}{dt} + M\frac{dI_{\text{m}}(t)}{dt} + V_{DS}(t) \tag{4a}$$

$$V_{\text{out}} = (L_{\text{rec}} + L_s - M)\frac{dI_{\text{rec}}(t)}{dt} + \Phi M\frac{dI_{\text{m}}(t)}{dt} + V_{KA}(t) \tag{4b}$$

where (4b) holds since $\Phi = \pm 1$, so $I_{\text{rec}}(t) = \Phi^2 I_{\text{rec}}(t)$.

Equations (3a) and (3b) are a system of ordinary differential equations (ODEs) that, along with the equations regulating $V_{DS}(t)$ and $V_{KA}(t)$, can be used to get the system evolution as in Figure 5. The missing equations depend on the ON/OFF state of the switching devices. For example, in the inverter loop, when the MOS is ON, the $I_{\text{inv}}(t)$ is all flowing trough it, with $V_{DS}(t)$ equal to zero. When OFF, the $I_{\text{inv}}(t)$ is flowing trough C_{inv} and it is integrated by it thus setting $V_{DS}(t)$. Since there are four possible combinations of the active devices ON/OFF states, we can identify four different working *zones*, referred to as Z_j, $j = 1, \ldots, 4$.

Zone Z_1: the MOS is OFF, while the diode is ON. The $I_{\text{inv}}(t)$ current is flowing through the C_{inv} while the rectifying diode forces the $V_{KA}(t)$ to zero, so

$$\begin{cases} I_{\text{inv}}(t) = C_{\text{inv}} \dfrac{dV_{DS}(t)}{dt} \\ V_{KA}(t) = 0 \end{cases} \tag{5a}$$

The ODE system is a third order one in the variables $I_{\text{inv}}(t)$, $I_{\text{rec}}(t)$ and $V_{DS}(t)$.

Zone Z_2: both the MOS and the diode are in the OFF-state. The $I_{\text{inv}}(t)$ and $I_{\text{rec}}(t)$ are flowing, respectively, through C_{inv} and C_{rec}, so that

$$\begin{cases} I_{\text{inv}}(t) = C_{\text{inv}} \dfrac{dV_{DS}(t)}{dt} \\ I_{\text{rec}}(t) = C_{\text{rec}} \dfrac{dV_{KA}(t)}{dt} \end{cases} \tag{5b}$$

Equations (3a) and (3b) along with (5b), make a forth-order ODE system in $I_{\text{inv}}(t)$, $I_{\text{rec}}(t)$, $V_{KA}(t)$ and $V_{DS}(t)$.

Zone Z_3: the MOS is externally turned ON, while the diode is OFF, so

$$\begin{cases} V_{DS}(t) = 0 \\ I_{\text{rec}}(t) = C_{\text{rec}} \dfrac{dV_{KA}(t)}{dt} \end{cases} \tag{5c}$$

As in zone Z_1, we are dealing with a third-order ODE system. The variables in this case are $I_{\text{inv}}(t)$, $I_{\text{rec}}(t)$ and $V_{KA}(t)$.

Zone Z_4: both active devices are ON, leading to

$$\begin{cases} V_{DS}(t) = 0 \\ V_{KA}(t) = 0 \end{cases} \tag{5d}$$

The associated ODE system is a second-order one in $I_{\text{inv}}(t)$ and $I_{\text{rec}}(t)$.

Any of the four considered systems can be written in matrix form as $\boldsymbol{x}'(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{b}$, where the size of $\boldsymbol{x}(t)$, $\boldsymbol{A}$ and $\boldsymbol{b}$ ranges from 2 to 4 (more precisely, from 2×2 to 4×4 for the matrix $\boldsymbol{A}$). The solution of this system is known, and given by the linear combination of terms $e^{\lambda_j t}$, where the λ_j are the eigenvalues of $\boldsymbol{A}$. In this way, we get an *analytic* expression, even if eigenvalues (and eigenvectors) have to computed numerically for a system whose order is higher than 2. Hence, one can get the converter evolution if:

- the succession of zones is given. Note that this depends on many factors: for example, while the MOS is externally turned ON and OFF with the desired frequency and the desired duty cycle, the diode turn-ON and turn-OFF instants have to be computed, respectively, as the time instants when the $V_{KA}(t)$ turns non-positive and when the $I_{\text{rec}}(t)$ turns non-negative. A numerical computation is required; however, turn-ON and turn-OFF instants can be used as constant in the analytic expressions found. The succession of zone observed in the simulation results of Figure 5 is clearly indicated; interestingly, the in-phase coupled converter and the 180° out-of-phase one show different successions.
- the continuity of all state variables is ensured when switching from one zone to another one. As an example, referring to the in-phase coupling, we can set the reference time $t = 0$ at the beginning of Z_1, with $V_{DS}(0) = 0$ and $V_{KA}(0) = 0$ due to circuit constraints, and where $I_{\text{inv}}(0) = I_{\text{inv}}^{(0)}$ and $I_{\text{rec}}(0) = I_{\text{rec}}^{(0)}$ are unknown variables. Assuming that Z_1 ends at t_1, we get $V_{KA}(t_1) = 0$ due to circuit constraints, and non-null values of $V_{DS}(t_1)$, $I_{\text{inv}}(t_1)$ and $I_{\text{rec}}(t_1)$. These values are to be used as initial conditions for computing the evolution in Z_2. Following a similar procedure also for Z_3 and Z_4, it is possible to get the (semi-)analytic evolution in a clock period as a function of circuit parameters and of the unknown variables $I_{\text{inv}}^{(0)}$ and $I_{\text{rec}}^{(0)}$.

The advantage of this approach with respect to that in [27] is twofold. First, no approximations have been used to get the evolution of the system. Second, by using a normalized time $\theta = 2\pi f_s t$, and by introducing the dimensionless

parameters

$$q_i = \frac{I_{\text{out}}}{2\pi f_s C_{\text{inv}} V_{\text{out}}},\ q_r = \frac{I_{\text{out}}}{2\pi f_s C_{\text{rec}} V_{\text{out}}},\ q_m = \frac{2\pi f_s M I_{\text{out}}}{V_{\text{out}}}$$
$$k_i = \frac{M}{L_{\text{inv}} + L_p},\ k_r = \frac{M}{L_{\text{rec}} + L_s} \tag{6}$$

and the normalized voltage and current signals $\mu = V_{\text{in}}/V_{\text{out}}$, $v_{DS}(\theta) = V_{DS}(2\pi f_s t)/V_{\text{out}}$, $v_{KA}(\theta) = V_{KA}(2\pi f_s t)/V_{\text{out}}$, $i_{\text{inv}}(\theta) = I_{\text{inv}}(2\pi f_s t)/I_{\text{out}}$ and $i_{\text{rec}}(\theta) = I_{\text{rec}}(2\pi f_s t)/I_{\text{out}}$, we get the dimensionless system

$$\mu = \frac{q_m}{k_i}\frac{d\, i_{\text{inv}}(\theta)}{d\,\theta} + q_m \Phi \frac{d\, i_{\text{rec}}(\theta)}{d\,\theta} + (1 - m^{\text{ON}}) v_{DS}(\theta)$$
$$1 = q_m \Phi \frac{d\, i_{\text{inv}}(\theta)}{d\,\theta} + \frac{q_m}{k_r}\frac{d\, i_{\text{rec}}(\theta)}{d\,\theta} + (1 - d^{\text{ON}}) v_{KA}(\theta)$$
$$i_{\text{inv}}(\theta) = \frac{1}{q_i}\frac{d\, v_{DS}(\theta)}{d\,\theta} \quad \text{if } m^{\text{ON}} = 0 \quad (Z_1 \text{ and } Z_2 \text{ only})$$
$$i_{\text{rec}}(\theta) = \frac{1}{q_r}\frac{d\, v_{KA}(\theta)}{d\,\theta} \quad \text{if } d^{\text{ON}} = 0 \quad (Z_2 \text{ and } Z_3 \text{ only}) \tag{7}$$

where the two boolean variables m^{ON} and d^{ON} are accounting, respectively, for MOS and diode ON/OFF state.[3]

Considering (7), we get a solution that is independent of the quantities f_s, V_{in}, V_{out} and I_{out}, and that can be denormalized and applied to any converter identified by the same voltage ratio μ and duty cycle D.[4] This will be clarified by the two examples of the following section.

C. DIMENSIONLESS CIRCUIT DESIGN

The ODE system in (7) can be solved to get the evolution of the converter in one period (i.e., the expressions for $i_{\text{inv}}(\theta)$, $i_{\text{rec}}(\theta)$, $v_{DS}(\theta)$ and $v_{KA}(\theta)$ for $0 \le \theta \le 2\pi$) as a mathematical function of the nine dimensionless quantities

$$\mu, D, k_i, k_r, q_i, q_m, q_r, i_{\text{inv}}^{(0)}, i_{\text{rec}}^{(0)}.$$

where $i_{\text{inv}}^{(0)}$ and $i_{\text{rec}}^{(0)}$ are the normalized counterparts of $I_{\text{inv}}^{(0)}$ and $I_{\text{rec}}^{(0)}$. Assuming that μ and D are given as design specifications, the other seven quantities can be considered variables to tune in order to ensure the optimal class-E operation. The desired behavior is achieved if we can ensure that

1) ZVS: $v_{DS}(\theta) = 0$ immediately before the time instant when the MOS is turned ON;
2) ZVDS: $dv_{DS}(\theta)/d\theta = 0$ immediately before the time instant when the MOS is turned ON;
3) stationary condition: to ensure that the stationary condition is achieved, one must have $i_{\text{inv}}(2\pi) = i_{\text{inv}}^{(0)}$ and $i_{\text{rec}}(2\pi) = i_{\text{rec}}^{(0)}$. Furthermore, neglecting a possible (stationary) output ripple, V_{out} is constant, i.e., the filter capacitance C_L has a zero-mean current. This condition is considered by imposing that the average value of $I_{\text{rec}}(t)$ is $-I_{\text{out}}$ or, in the dimensionless model, that the average value of $i_{\text{rec}}(\theta)$ is -1, i.e.:

$$\frac{1}{2\pi}\int_0^{2\pi} i_{\text{rec}}(\theta) d\theta + 1 = 0 \tag{8}$$

Following this procedure, five mathematical equations must be satisfied by the correct choice of seven unknowns. This is an underdetermined system: two unknowns can be considered free variables to be set by the designer, while the other five are set by this design procedure. Note that it is convenient to allow the procedure to set $i_{\text{inv}}^{(0)}$ and $i_{\text{rec}}^{(0)}$, since their values are not directly related to any circuit element. Conversely, q_i, q_r, q_m, k_i and k_r, once properly denormalized, set the values of C_{inv}, C_{rec}, M, L_{inv} and L_{rec}, respectively.

A natural choice is to allocate k_i and k_r as degrees of freedom, since constraints on inductors are usually tighter with respect to those on capacitors. One could also opt to remove either L_{inv} from the inverter loop (hence $k_i = 1$) or L_{rec} from the rectifying loop ($k_r = 1$) for economical or space reasons. The two degrees of freedom can also be used to tune aspects of the circuit behavior that have been not considered in the optimization. As an example, one can sweep them to look for a minimum in the RMS inverter or rectifier currents for improving the converter efficiency. Another example is the investigation of the duty cycle of the diode, that has not been considered in the optimization, and that should be set to reasonable values (i.e., far enough from 0% or 100%) for optimal performance.

Once k_i and k_r are set, one can get the dimensionless design solution (i.e., the value of q_i, q_m and q_r) and then, denormalize it exploiting (6) using the actual value of V_{out}, I_{out} and f_s, to get the $L_{\text{inv}} + L_p$, $L_{\text{rec}} + L_s$, M, C_{inv} and C_{rec} required to ensure optimal class-E operation. The full set of design solutions for both canonical topologies ($\Phi = +1$ and $\Phi = -1$), considering different values of μ and the two corner cases $k_i = 1$, $k_r < 1$, and $k_i < 1$, $k_r = 1$, is shown in Figure 7.

Two design examples are now presented with the aim of clarifying the procedure. Both are based on ideal elements, including a perfectly coupled transformer with a 1 : 1 turn ratio, for which $L_p = L_s = M$. Examples including realistic models of circuit elements will be presented in the next section.

Design Example 1: Let us consider a dc-dc converter designed according to the class-E topology of Figure 4(a) (i.e. $\Phi = 1$) operating at 15 MHz and $D = 0.5$, with $V_{\text{in}} = 5$ V, $V_{\text{out}} = 3.3$ V and $P_{\text{out}} = 1$ W (so $I_{\text{out}} = 303$ mA). This is a step-down converter with $\mu = 1.51$. Let us also assume the constraints $L_{\text{inv}} = 3M$ and L_{rec} not present in the circuit, so $L_{\text{rec}} = 0$. In terms of dimensionless quantities, we have $k_i = 0.25$ and $k_r = 1$. The values of q_m, q_i, and q_r ensuring optimal class-E operation can be retrieved from the design curves in Figure 7 with $k_r = 1$, $\Phi = +1$, resulting in $q_m = 0.65$, $q_i = 3.65$, $q_r = 0.75$. By using (6) we get the denormalized values for the transformer inductance $L_p = L_s = M = 75$ nH, the inverter loop

[3] We set $m^{\text{ON}}(d^{\text{ON}}) = 1$ when the MOS (diode) is ON and 0 when OFF. Also, please note that the parameter q_m replaces what in [29] authors indicated as q_x.

[4] Despite being usually set to $D = 0.5$, we would like to stress that D can actually be considered a degree of freedom in the converter design.

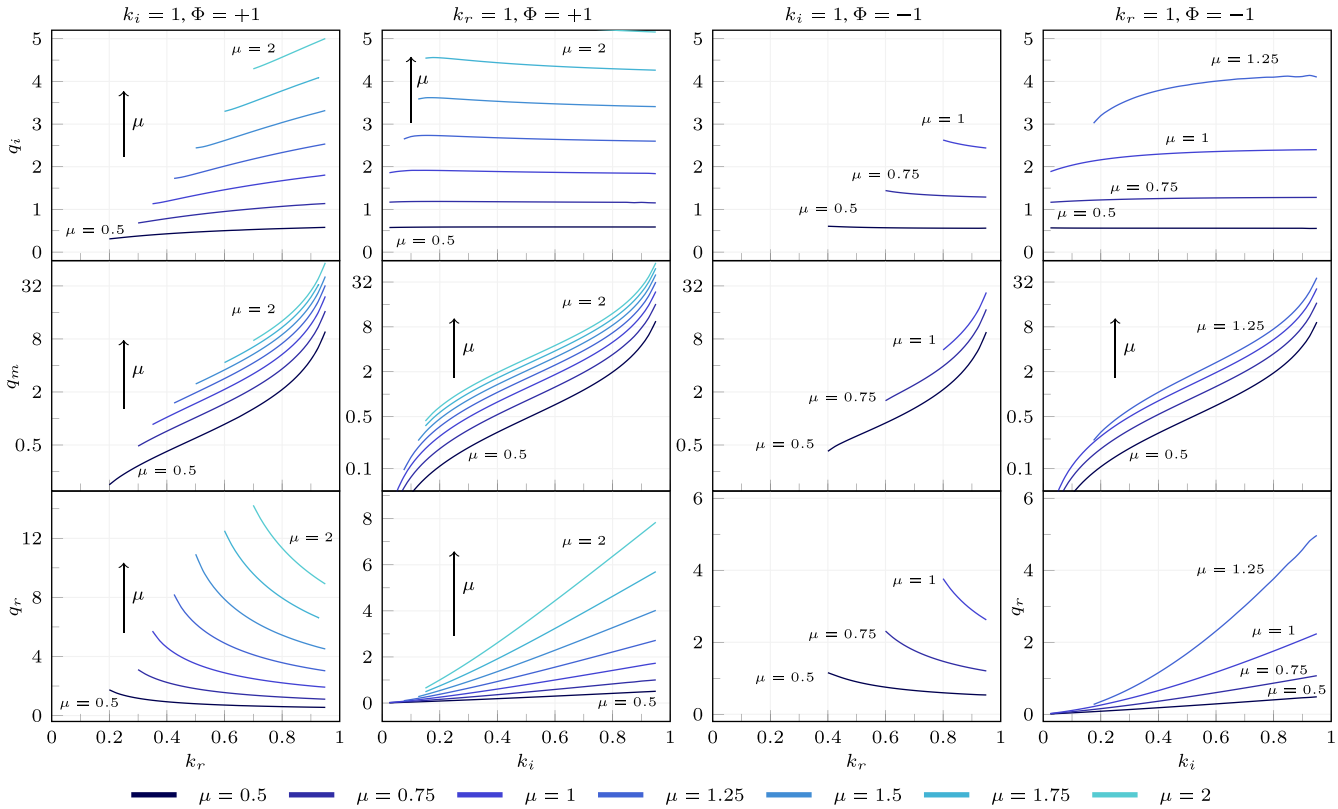


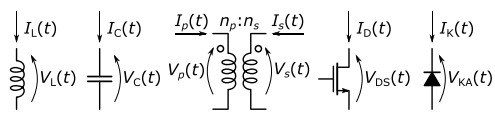
FIGURE 7. Class-E resonant converter design curves when considering ideal circuital elements and with $D = 0.5$, for different values of μ, k_i and k_r. From left to right: In-phase coupling, with $L_{\text{rec}} = 0\,\text{H}$ ($k_i = 1$, $\Phi = +1$); in-phase coupling, with $L_{\text{inv}} = 0\,\text{H}$ ($k_r = 1$, $\Phi = +1$); 180° out-of-phase coupling, with $L_{\text{rec}} = 0\,\text{H}$ ($k_r = 1$, $\Phi = -1$); 180° out-of-phase coupling, with $L_{\text{inv}} = 0\,\text{H}$ ($k_i = 1$, $\Phi = -1$).

inductance $L_{\text{inv}} = 225\,\text{nH}$, and the capacitors $C_{\text{inv}} = 267\,\text{pF}$ and $C_{\text{rec}} = 1.3\,\text{nF}$. The waveforms shown in Figure 5(a) have been achieved from a SPICE simulation using these values.

Design Example 2: Let us consider a 12 V-to-18 V ($\mu = 0.667$) step-up dc-dc converter operating at 75 MHz and $D = 0.5$ with 4.2 W output power ($I_{\text{out}} = 233\,\text{mA}$). Let us also consider a 180° out-of-phase topology (i.e., $\Phi = -1$) without L_{inv} (so $L_{\text{inv}} = 0$) and $L_{rec} = M$, hence $k_i = 1$ and $k_r = 0.5$. According to the design curves in Figure 7 for $k_i = 1$, $\Phi = -1$ we get $q_m = 0.84$, $q_i = 1.09$, $q_r = 1.98$, that leads to $L_{\text{rec}} = M = 137\,\text{nH}$, $C_{\text{inv}} = 25.2\,\text{pF}$ and $C_{\text{rec}} = 13.9\,\text{pF}$. These values have been used for the simulation shown in Figure 5(b).

D. LOSSY CIRCUIT DESIGN

It is possible to include major sources of losses in (7) as long as the device models are linear. Let us consider, for all elements in the circuit, a series resistance expressed by means of a quality factor for passive elements (inductors, capacitors, and transformer) or an on-state resistance for switches (R_{DS}^{ON} for the MOS and R_D^{ON} for the diode), and a voltage drop V_D^{ON} for the diode, as summarized in Figure 8. Let us also refer to the quality factors of L_{inv}, L_{rec}, C_{inv}, and C_{rec} as $Q_{L_{\text{inv}}}$, $Q_{L_{\text{rec}}}$, $Q_{C_{\text{inv}}}$ and $Q_{C_{\text{rec}}}$, respectively. With this, it is possible to recompute (7) as (9), as shown at the bottom of the next page, where we have set the additional dimensionless



$$V_L(t) = L\frac{dI_L(t)}{dt} + L\frac{2\pi f_s}{Q_L}I_L(t)$$

$$V_C(t) = \frac{1}{C}\int I_C(t)dt + \frac{1}{2\pi f_s C Q_C}I_C(t)$$

$$\begin{pmatrix} V_p(t) \\ V_s(t) \end{pmatrix} = \begin{pmatrix} L_p & \Phi M \\ \Phi M & L_s \end{pmatrix} \frac{d}{dt}\begin{pmatrix} I_p(t) \\ I_s(t) \end{pmatrix} + 2\pi f_s \begin{pmatrix} L_p/Q_{L_p} & \pm M/Q_M \\ \pm M/Q_M & L_s/Q_{L_s} \end{pmatrix}\begin{pmatrix} I_p(t) \\ I_s(t) \end{pmatrix}$$

$$\begin{cases} V_{\text{DS}}(t) = R_{\text{DS}}^{\text{ON}} I_D(t), & m^{\text{ON}} = 1 \\ I_D(t) = 0, & m^{\text{ON}} = 0 \end{cases}$$

$$\begin{cases} V_{\text{KA}}(t) = -V_D^{\text{ON}} + R_{\text{D}}^{\text{ON}} I_K(t), & d^{\text{ON}} = 1 \\ I_K(t) = 0, & d^{\text{ON}} = 0 \end{cases}$$

FIGURE 8. Device models used for including major sources of losses in the converter analysis.

factors

$$g_{DS}^{\text{ON}} = \frac{V_{\text{out}}}{I_{\text{out}}}\frac{1}{R_{DS}^{\text{ON}}}, \quad g_D^{\text{ON}} = \frac{V_{\text{out}}}{I_{\text{out}}}\frac{1}{R_D^{\text{ON}}}, \quad v_d^{\text{ON}} = \frac{V_D^{\text{ON}}}{V_{\text{out}}}$$

and where, for a more compact notation, we have defined

$$\frac{1}{Q_{\text{inv}}} = \frac{1}{L_{\text{inv}} + L_p - M}\left(\frac{L_{\text{inv}}}{Q_{L_{\text{inv}}}} + \frac{L_p}{Q_{L_p}} - \frac{M}{Q_M}\right)$$

$$\frac{1}{Q_{\text{rec}}} = \frac{1}{L_{\text{rec}} + L_s - M}\left(\frac{L_{\text{rec}}}{Q_{L_{\text{rec}}}} + \frac{L_s}{Q_{L_s}} - \frac{M}{Q_M}\right)$$

The only approximation used in computing (9) is to neglect the effects of the C_{inv} and of the C_{rec} when the MOS and the diode are ON, respectively.

By computing $i_{\text{inv}}(\theta)$, $i_{\text{rec}}(\theta)$, $v_{DS}(\theta)$ and $v_{KA}(\theta)$ using (9), and replacing the obtained expression in the approach described in Section III-C, it is possible to get a design that keeps into account many sources of losses in the circuit design. The examples considered in the next section are based on this approach.

Of course, this design approach holds as long as the model for the considered devices is valid. Taking into account some non-linear effects, a more complex model, or other effects (such as a non-negligible reverse recovery time for the diode, that can strongly affect the design at particularly high operating frequencies) is not possible. Indeed, we do not consider this a limitation of the approach, as it will affect in the same way any other design approach. Nevertheless, in presence of a strong non-linearity, this design strategy can be still be used to get a very good starting design point (i.e., better with respect to what can be obtained with any other design approach proposed in the Literature), to be refined by further SPICE simulations.

IV. CLASS-E NON-ISOLATED TOPOLOGIES

Despite being useful in many applications, galvanic isolation is not always required. In this case, a simpler and cheaper non-isolated implementation can be achieved by considering the architectures in Figure 4(a) and (b) and replacing the coupling transformer with an inductor whose inductance value is $M = L_p = L_s$, the quality factor $Q_M = Q_{L_p} = Q_{L_s}$, and the current flowing into it is I_{m}.

Even considering a possible different circuit layout, the design approach described in Section III can still be applied if

- the circuit evolution is still described by (7), or by (9) if the lossy design is to be taken into account;
- the constraints to achieve ZVS, ZVDS and the stationary condition are still expressed as in III-C.

In [29] this approach has been followed, and authors presented a non-isolated class-E dc-dc converter whose schematic is derived from that of Figure 4(a) by directly replacing the transformer with an inductor M. Yet, this approach has the disadvantage that, in the achieved circuit, input and output voltages do not share the same ground reference.

In the following we present how to conveniently rearrange the two presented canonical topologies to obtain a resonant class-E buck-boost dc-dc converter with common ground reference. Similarly, we also show how the scheme of Figure 4(b) can be turned either into an equivalent buck (step-down) or boost (step-up) resonant converter. All these non-isolated topologies can be designed by means of the curves proposed in Figure 7.

In order to simplify the notation, it is convenient to define the quantity ν computed as the average value of the normalized inverter mesh current

$$\frac{1}{2\pi}\int_0^{2\pi} i_{\text{inv}}(\theta)d\theta = \nu \tag{10a}$$

In a lossless converter, it is $\nu = 1/\mu$, while it is $\nu > 1/\mu$ considering the lossy analysis of Section III-D. The average value of the $I_{\text{inv}}(t)$ (i.e., the converter input current for the topologies of Figure 4) can be denormalized as νI_{out}. Note that ν can also be used to compute the converter efficiency: for both topologies of Figure 4, the efficiency is given by $\eta = V_{\text{out}}I_{\text{out}}/(\mu V_{\text{out}}\nu I_{\text{out}}) = 1/(\mu\nu)$. Furthermore, since $i_{\text{m}}(t) = i_{\text{inv}}(t) + \Phi\, i_{\text{rec}}(t)$, we get

$$\frac{1}{2\pi}\int_0^{2\pi} i_{\text{m}}(\theta)d\theta = \nu - \Phi \tag{10b}$$

so that the average value of the $I_{\text{m}}(t)$ can be denormalized as $(\nu - \Phi)I_{\text{out}}$.

A. BUCK-BOOST CONFIGURATION

The circuit depicted in Figure 9(a) comes directly from that of Figure 4(a) when the transformer is replaced by M and circuit elements are rearranged (e.g., the MOS and the diode are connected to the input and the output node, respectively) to ensure a common ground reference for V_{in} and V_{out}. The drawback is that the MOS source terminal is not connected anymore to the ground reference, so either a N-MOS with a bootstrap circuit (as implicitly assumed), or a P-MOS device, is required. We refer to this topology as the non-inverting buck-boost, since it is capable to act either as a step-up ($V_{\text{out}} > V_{\text{in}}$, $\mu < 1$) or a step-down converter ($V_{\text{out}} < V_{\text{in}}$, $\mu > 1$). However, it is worth noting that, once designed, the resonant converter is constrained to operate either in

$$\begin{aligned}
\mu &= \frac{q_m}{k_i}\frac{di_{\text{inv}}(\theta)}{d\theta} + \Phi\, q_m\frac{di_{\text{rec}}(\theta)}{d\theta} + \left(\frac{1-k_i}{k_i}\frac{q_m}{Q_{\text{inv}}} + \frac{q_m}{Q_M} + \frac{\left(1-m^{\text{ON}}\right)q_i}{Q_{C_{\text{inv}}}} + \frac{m^{\text{ON}}}{g_{DS}}\right) i_{\text{inv}}(\theta) + \Phi\,\frac{q_m}{Q_M} i_{\text{rec}}(\theta) + \left(1-m^{\text{ON}}\right) v_{C_{\text{inv}}}(\theta) \\
1 &= \Phi\, q_m\frac{di_{\text{inv}}(\theta)}{d\theta} + \frac{q_m}{k_r}\frac{di_{\text{rec}}(\theta)}{d\theta} + \Phi\,\frac{q_m}{Q_M} i_{\text{inv}}(\theta) + \left(\frac{1-k_r}{k_r}\frac{q_m}{Q_{\text{rec}}} + \frac{q_m}{Q_M} + \frac{\left(1-d^{\text{ON}}\right)q_r}{Q_{C_{\text{rec}}}} + \frac{d^{\text{ON}}}{g_D^{\text{ON}}}\right) i_{\text{rec}}(\theta) \\
&\quad + \left(1-d^{\text{ON}}\right) v_{C_{\text{rec}}}(\theta) - d^{\text{ON}} v_D^{\text{ON}} \\
i_{\text{inv}}(\theta) &= \frac{1}{q_i}\frac{dv_{C_{\text{inv}}}(\theta)}{d\theta} \quad (Z_1 \text{ and } Z_2 \textit{ only}), \qquad i_{\text{rec}}(\theta) = \frac{1}{q_r}\frac{dv_{C_{\text{rec}}}(\theta)}{d\theta} \quad (Z_2 \text{ and } Z_3 \text{only})
\end{aligned} \tag{9}$$

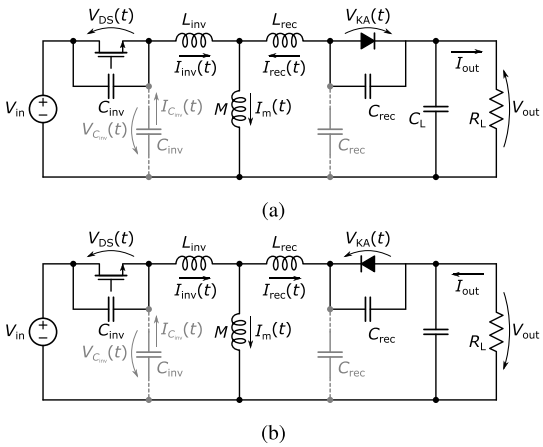


FIGURE 9. Comparison between buck-boost topologies. (a) non-inverting class-E resonant buck-boost converter. (b) inverting class-E resonant buck-boost converter.

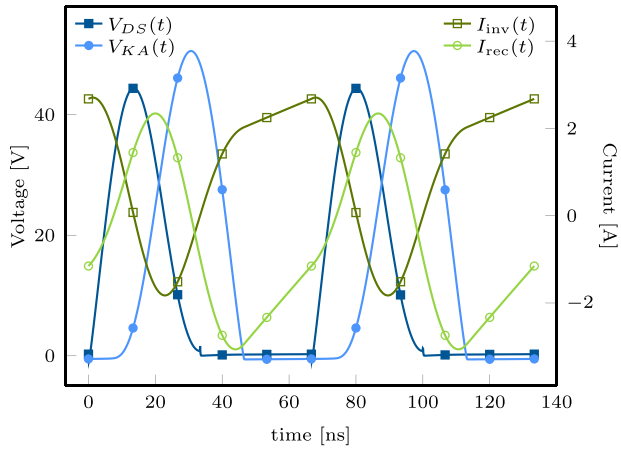


FIGURE 10. Waveforms in the non-inverting buck-boost design example proposed in Section IV-A.

buck or boost mode and, in order to preserve the desired ZVS/ZVDS behavior, the ratio μ between the input and the output voltages should not change.

In this circuit the same inverter and a rectifier meshes as in the circuits of Figure 4 are clearly identifiable. Being $I_m(t) = I_{inv}(t) + I_{rec}(t)$, the meshes are still described by the two equations in (4) assuming $\Phi = +1$. In conclusion, there is a perfect equivalence between the equations regulating the behavior of this circuit, and the one considered in Section III-B. Since it is easy to see that (8) still holds, this circuit can be designed through the curves in Figure 7, either with $k_i = 1$, $\Phi = +1$ (when $L_{inv} = 0$) or $k_r = 1$, $\Phi = +1$ (when $L_{rec} = 0$).

A buck-boost converter equivalent to the 180° out-of-phase coupling topology is depicted in Figure 9(b). Here, $I_m(t) = I_{inv}(t) - I_{rec}(t)$, so $\Phi = -1$. This converter can be designed through the curves in Figure 7 with $k_i = 1$, $\Phi = -1$ (when $L_{inv} = 0$) or with $k_r = 1$, $\Phi = -1$ (when $L_{rec} = 0$) and it is actually an inverting buck-boost topology, since the output voltage node is at a negative potential with respect to the common ground reference.

Note that, in both schematics of Figure 9, both C_{inv} and C_{rec} can be connected either in their standard position (i.e., in parallel to the MOS and the diode), or in an alternative position directly connected to ground as shown in light gray the figure. Focusing on C_{inv}, the current flowing into it when it is connected in the alternative position, under the assumption of an ideal model for the capacitor and a perfectly constant V_{in}, can be computed with the MOS OFF as

$$I_{C_{inv}}(t) = C_{inv}\frac{dV_{C_{inv}}}{dt} = C_{inv}\frac{d\left(V_{DS}(t) - V_{in}\right)}{dt} = C_{inv}\frac{dV_{DS}(t)}{dt}$$

that is the same current one get assuming that the C_{inv} is in the standard position. So, in both configurations, the contribution of C_{inv} to the $I_{inv}(t)$ is the same.

Yet, when introducing a lossy model, the perfect equivalence is lost. Nevertheless, it is very easy to find capacitors with very high quality factors, so the difference between the two configurations is expected to be limited, and both of them are indeed found in the literature.

Design Example 3: let us consider the design of a 10 W, 12 V-to-15 V class-E converter with the buck-boost topology of Figure s-E converter with the buck-boost topology, operating at 15 MHz with $D = 0.5$. Let us also assume that $L_{inv} = L_{rec} = M$ (so that $k_i = 0.5$ and $k_r = 0.5$). The design parameters are $V_{in} = 12$ V, $V_{out} = 15$ V, and $\mu = 0.8$. Furthermore, $I_{out} = 667$ mA. Let us assume that $Q_{L_{inv}} = Q_{L_{rec}} = Q_M = 80$, and that the capacitors C_{inv} and C_{rec} has an infinite quality factor.[5] Let us also choose a Si2392ADS MOS from Vishay (modeled with $R_{DS}^{ON} = 0.1\,\Omega$) and a Nexperia PMEG6030ELP Schottky barrier rectifier diode (modeled with $V_D^{ON} = 0.55$ V and $R_D^{ON} = 0.1\,\Omega$). The solution we get from the dimensionless system is $q_i = 0.887$, $q_r = 0.685$ and $q_m = 0.314$, that leads to $L_{inv} = L_{rec} = M = 75$ nH, $C_{inv} = 420$ pF and $C_{rec} = 560$ pF. Note that a straightforward application of (6) would lead to slightly higher values of C_{inv} and of C_{rec}; the values proposed here have been decreased by 110 pF and 130 pF, respectively, to compensate the parasitic capacitance of the MOS and of the diode. The waveforms observed in a SPICE simulation that takes into account the semiconductor device models supplied by the producer can be seen in Figure 10. The optimal class-E operation is visibly achieved, and the output power, that is evaluated in 10.3 W, settles to a value very similar to the desired one.

B. BUCK CONFIGURATION

The circuit shown in Figure 11 is a resonant buck converter. Similar resonant or quasi-resonant topologies appeared many times in the recent literature. Authors in [32] proposed a ZVS buck converter with non-resonant rectifier (i.e., without C_{rec}) and where the L_{rec} is not used. In [33] authors presented an overview of different ZVS converter topologies, including that of Figure 11 in the two alternatives where only one inductor among L_{inv} and L_{rec} is present. In [36] a buck converter is

[5] Ceramic capacitors with C0G dielectric ensure extremely high performance (quality factor > 1000) so that they can be assumed ideal.

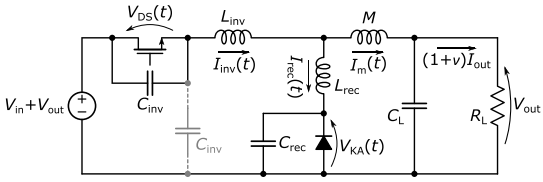


FIGURE 11. Class-E resonant buck converter.

proposed based on the schematic of Figure 11 without the rectifier inductance L_{rec}. In [30] a 15 MHz converter with the same schematic in the latter configuration is analyzed and designed.

Let us refer to the design of a companion converter according to the isolated canonical topology with 180° out-of-phase coupling (i.e., $\Phi = -1$), and let us indicate with V_{in}, V_{out} and I_{out} as the input voltage, output voltage and output current of this design. As clarified below, the behavior of the converter in Figure 11 is the same of the companion one assuming that we indicate with $V_{in} + V_{out}$ its input voltage level, and with V_{out} its output voltage level, with $\mu = V_{in}/V_{out}$. Note that, with this, the output voltage is compelled to be always smaller than the input one independently of μ.

Then, as assumed in previous designs, capacitors C_{inv} and C_{rec} if large enough may mask, respectively, the parasitic capacitances of the MOS and the diode; M replaces the transformer with $I_m = I_{inv}(t) - I_{rec}(t)$ and $L_p = L_s = M$. Hence, if we consider the Kirchhoff voltage law at the outer mesh, we get

$$V_{in} + V_{out} = V_{DS}(t) + L_{inv}\frac{dI_{inv}(t)}{dt} + M\frac{dI_m(t)}{dt} + V_{out}$$

that is the same as (4a), while the equation of the rectifier mesh

$$V_{out} = V_{KA}(t) + L_{rec}\frac{dI_{rec}(t)}{dt} - M\frac{dI_m(t)}{dt}$$

is (4b). Finally, the output current of the converter of Figure 11 is given by the average value of $I_m(t)$. Let us indicate with I_{out} the output current of the companion converter, and assume that its design has been obtained using (8). According to (10b) the output current of the buck converter is given by $(\nu + 1)I_{out}$.

In conclusion, with the introduced notation, all equations regulating the evolution of the canonical topology with $\Phi = -1$ hold also for the buck topology, that can be so designed by means of the curves in Figure 7.

Design Example 4: let us consider a 2.5 W, 8 V-to-5 V class-E buck converter working at 2 MHz with $D = 0.5$. We target a design where $L_{inv} = 0$, and $L_{rec} = M$, so we set the two degrees of freedom $k_i = 1$ and $k_r = 0.5$. Due to the buck topology, we have $V_{in} + V_{out} = 8$ V, $V_{out} = 5$ V and $(1 + \nu)I_{out} = 500$ mA. In order to get the converter design, we should consider a companion 180° out-of-phase coupled converter with $V_{in} = 3$ V, $V_{out} = 5$ V and $\mu = 0.6$, while I_{out} is not know yet since we do not have an estimation of ν yet. By considering $Q_{L_{rec}} = Q_M = 40$, assuming that the capacitors C_{inv} and C_{rec} have an infinite quality factors,

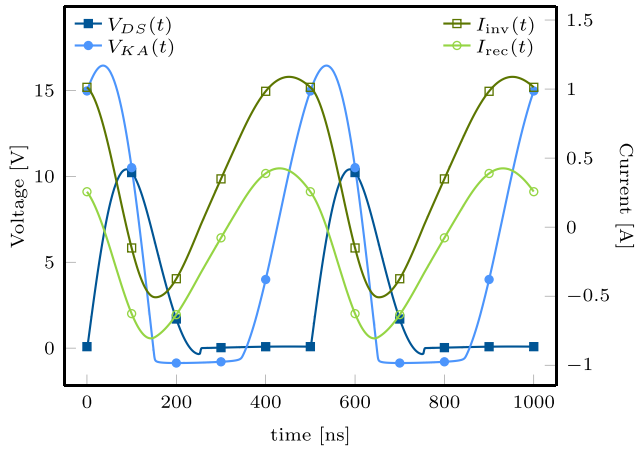


FIGURE 12. Waveforms in the buck design example proposed in Section IV-B.

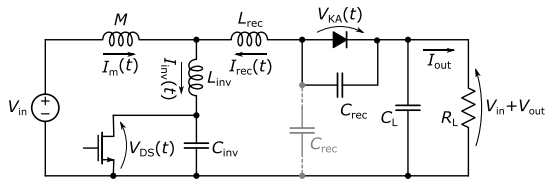


FIGURE 13. Class-E resonant boost converter.

and that the MOS and the diode are a IRLML0030TRP from International Rectifier (modeled with $R_{DS}^{ON} = 0.1\,\Omega$) and a ES1B from Diodes Incorporated (modeled with $V_D^{ON} = 0.75$ V and $R_D^{ON} = 0.15\,\Omega$), the optimal design is achieved with the dimensionless parameters $q_i = 0.456$, $q_r = 0.635$, $q_m = 0.552$. The lossy dimensionless system has $\nu = 2.61$, that allows us to estimate the current of the canonical companion converter as $I_{out} = 138$ mA. Using these values, we can denormalize the solution in $L_{rec} = M = 1.59\,\mu$H, $C_{inv} = 4.8$ nF and $C_{rec} = 3.5$ nF. Being the C_{inv} and C_{rec} much larger than the MOS and the diode parasitic capacitances, no correction on their values have been applied. The observed waveforms from a SPICE simulation based on the semiconductor models developed by the producer can be seen in Figure 12, and show that the optimal class-E operation is well achieved. The output power is evaluated in 2.51 W.

C. BOOST CONFIGURATION

The circuit in Figure 13 represents a resonant boost converter. This topology, in the two alternative implementations with $L_{inv} = 0$ or $L_{rec} = 0$, is actually one of the most commonly used in the literature due to its simplicity.[6] In their overview of different ZVS converter topologies in [33], authors included both implementations. In [37] a ZVS boost converter without L_{rec} and with a non-resonant rectifier (i.e., without C_{rec}) is proposed. In [38] a particular circuit, indicated as Φ_2 converter, has been introduced. This is basically a boost converter like that in Figure 13 with $L_{inv} = 0$, whose peculiarity is to present an additional LC resonant

[6] As an example, in the schematic of Figure 13 there is no need for any bootstrap circuit.

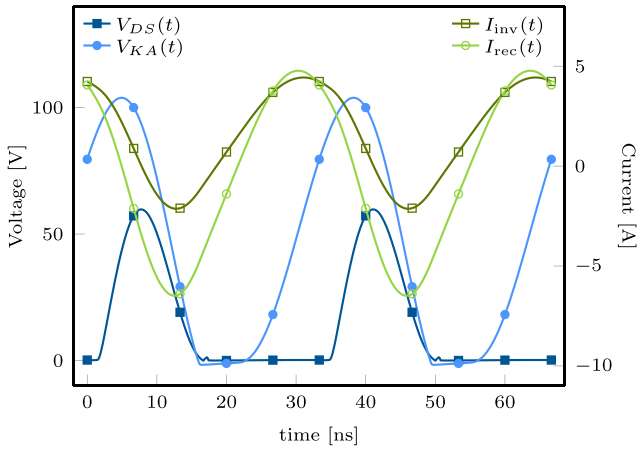


FIGURE 14. Waveforms in the boost design example proposed in Section IV-C.

circuit whose aim is to reduce the peak value of the voltage $V_{DS}(t)$ across the main switch. The dc-dc converter in [39] is a boost circuit presenting a small variation with respect to that of Figure 13, where only the L_{rec} is present. The converter proposed in [27] by Burkhart *et al.* is fully resonant boost converter featuring ZVS. The converter topology is that of Figure 13 where only the L_{rec} has been considered, while $L_{inv} = 0$.

As in the previous case, also the boost converter of Figure 13 is perfectly described by the equations regulating the behavior of the canonical 180° out-of-phase coupled converter. To see this, let us indicate with V_{in} the input voltage level and with $V_{in} + V_{out}$ the voltage at the output node. Let also be I_{out} the output current, and $\mu = V_{in}/V_{out}$. The capacitor C_{rec}, either connected in canonical or in the alternative position, is capable to mask diode parasitic capacitance. Then, the equation regulating the inverter mesh

$$V_{in} = M\frac{dI_m(t)}{dt} + L_{inv}\frac{dI_{inv}(t)}{dt} + V_{DS}(t)$$

is (4a), while the equation of the outer mesh

$$V_{out} + V_{in} = V_{KA}(t) + L_{rec}\frac{dI_{rec}(t)}{dt} - M\frac{dI_m(t)}{dt} + V_{in}$$

is equal to (4b) under the assumption that $\Phi = -1$ and $L_p = L_s = M$. Furthermore, according to the figure, we get $I_m(t) = I_{inv}(t) - I_{rec}(t)$. Finally, the output current is given by the average value of $-I_{rec}(t)$, and since (8) holds, is simply given by I_{out}. In conclusion, as in the previous case, all equations regulating the behavior of the canonical circuit with $\Phi = -1$ hold, so the circuit design can be achieved by means of the design curves in Figure 7.

Design Example 5: consider a 16 V-to-60 V class-E boost converter working at 30 MHz with $D = 0.5$ and with a 25 W output power. We target a design where $L_{rec} = 0$, and $L_{inv} = M$. To ensure this, the two degrees of freedom are set to $k_i = 0.5$ and $k_r = 1$. Relying on a boost topology, we have $V_{in} = 16$ V, $V_{in} + V_{out} = 60$ V. Parameters of the companion canonical system are $\Phi = -1$ (i.e., 180° out-of-phase coupling), $V_{in} = 16$ V, $V_{out} = 44$ V and $I_{out} = 417$ mA, with $\mu = 0.364$. Here we consider $Q_{L_{inv}} = Q_M = 70$ and that C_{inv} and C_{rec} have an infinite quality factor. The MOS is a STL4N10F7, and the diode a STPSC406, both from ST semiconductors, modeled with $R_{DS}^{ON} = 50\,\text{m}\Omega$, $V_D^{ON} = 1.0$ V and $R_D^{ON} = 0.5\,\Omega$. The solution of the dimensionless system is $q_i = 0.206$, $q_r = 0.102$, $q_m = 0.217$, that can be denormalized in $L_{inv} = M = 122$ nH, $C_{inv} = 110$ pF and $C_{rec} = 450$ pF. The values of C_{inv} and C_{rec} have been reduced by 130 pF and 40 pF in order to compensate the parasitic capacitance introduced by the MOS and the diode. The observed waveforms from a SPICE simulation based on the semiconductor models provided by ST can be seen in Figure 14. The output power in the simulation is evaluated in 23.9 W.

Note that this example is the most critical one, mainly due to the very high operating frequency. In particular, the adherence of the output power with the desired one is the lowest among all proposed examples. This is due to the fact that the lossy model assumed in Section III-D has reached its limit, since the non-linear parasitic capacitances of the active devices are not anymore negligible with respect to the C_{inv} and C_{rec}. Indeed, the simulation still shows more than acceptable performance.

V. CONCLUSION

In this paper many resonant and quasi resonant converter architectures proposed in the literature in the last three decades have been taken into account. We have shown that, despite presenting different implementation, and even different topologies (fly-back, buck-boost, buck or boost), all of them can be described by the same mathematical equations. As a result, all considered converters can be divided into two groups, one of them perfectly equivalent to an isolated topology with a transformer featuring in-phase coupling, and the other to the same isolated topology with 180° out-of-phase coupling. A comprehensive analysis and design theory for the two canonical topologies is provided, that can be considered as a unified design theory for the whole family of resonant architectures.

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