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***Abstract*—In this paper, we present an automated strategy for extracting behavioral small-signal macromodels of biased nonlinear circuit blocks. We discuss in detail the case study of a Low DropOut (LDO) voltage regulator, which is an essential part of the power distribution network in electronic systems. We derive a compact yet accurate surrogate model of the LDO, which enables fast transient power integrity simulations, including all parasitics due to the specific layout of the LDO realization. The model is parameterized through its DC input voltage and its output current and is thus available as a SPICE netlist. Numerical experiments show that a speedup up to 700X is achieved when replacing the extracted post-layout netlist with the surrogate model, with practically no loss in accuracy.**

I. Introduction

The design and testing of highly integrated systems is one of the most challenging steps in the development of smart devices and IoT technologies. The need for continuous miniaturization and performance improvement forces designers to perform repeated simulation-based verifications of system compliance, both in a pre-layout phase where the concept is developed, and especially in a post-layout phase, when the influence of all parasitics due to non ideal material properties and electromagnetic coupling can be precisely assessed. The main issue of a post-layout numerical verification is the potentially huge complexity of the numerical simulation problem, both at the electromagnetic field and at the circuit level.

Among the various analysis types that are required, Power Integrity (PI) verification is one of the most challenging steps. A complete Power Distribution Network (PDN) simulation deck must include an accurate representation of the large-scale interconnects at chip, package and board levels, which are responsible for the various resonances that may trigger voltage droops in various frequency ranges. Accurate models for decoupling capacitors are also required, in order to assess their performance in lowering the overall PDN impedance. A realistic transient current profile as would be drawn by logic blocks in real operation completes the simulaton problem description, together with models of the Voltage Regulators (VR) that are inserted in various locations for stabilizing the supply voltage of each power domain.

This work concentrates on the latter voltage regulators, which pose a numerical simulation challenge due to their intrinsic nonlinear characteristics. In fact, interconnects behave as large-scale linear systems, whose response can be derived either in time or frequency domain. Several Model Order Reduction (MOR) approaches are available for characterizing PDN interconnects through compact models, including classical reduction [1], [2] and data-driven reduction through, e.g., Vector Fitting (VF) of frequency responses combined with passivity characterization and enforcement [3], [4]. The presence of nonlinear circuit blocks such as voltage regulators impairs a complete system-level description in the frequency domain, and a transient PI verification is thus necessary. Simplified linear VR models can be used and are widely adopted [5], but the inherent approximations due to such linearization may compromise the reliability of the simulation results, especially in low power systems where the nominal supply voltage levels are reduced to a minimum, thus increasing system sensitivity to power noise. The reliability of a linearized model of a nonlinear circuit block is only granted around the linearization point. When such bias point changes, the model inevitably looses accuracy and needs to be recomputed. This fact occurs systematically for VR, due to possible variations in the DC output voltage (which may be lowered to save battery time or increased to boost system performance), and especially load current.

In this work, we propose a strategy for the characterization of nonlinear VR circuit blocks, in particular Low DropOut (LDO) voltage regulators, through compact and reduced-order behavioral models that reproduce their small-signal frequency response. We parameterize these small-signal models explicitly as functions of the nominal supply voltage and nominal load current, so that the linearized model can adapt automatically to variations of the linearization point. As a result, the parameterized macromodels can seamlessly replace the corresponding full-detail nonlinear circuit blocks in any system-level simulation. Since the proposed strategy can be applied also in a post-layout setting, we are able to demonstrate in such scenario up to $700\times$ speedup in transient simulation, thanks to the reduced-order nature of the parameterized macromodels.

The proposed parameterized macromodeling approach leverages on recent developments in model structure definition and fitting [6], [7], and especially uniform stability enforcement [8], [9]. We are able to guarantee that the poles of the small-signal model remain in the stable region as they move in the complex plane when bias parameters are changed. This fact guarantees model robustness in transient simulation, by avoiding spurious instabilities. Of course, the standard practice of enforcing model passivity [4] is not necessary for this application, since the small-signal responses of active devices do not comply with passivity conditions. With respect to alternative approaches for behavioral modeling of nonlinear

devices [10], [11], which may be adequate for particular structures or topologies and/or excitation types (e.g. harmonic or polyharmonic), the proposed approach is general and can be fully automated.

II. A Case Study

This paper provides a proof of concept by discussing in detail a specific case study. We consider a low-quiescent (IQ) Only-MOS low-dropout (LDO) regulator, originally presented in [12]. This LDO is comprised by high slew-rate amplifier with push-pull output control, which enables an ultra-low IQ with reasonable transient responses. Based on the specifications of [12], we designed the LDO as illustrated in Fig. 1, by realizing an implementation in a 40 nm standard CMOS process. The final layout occupies around 0.0045 mm^2. The LDO regulator can deliver 10 mA load current I_L at a minimum 0.9 V V_{DD} supply voltage. Fig. 1 summarizes the main features, including circuit schematic, a high-level layout snapshot, and the main parameters.

III. Circuit Linearization

A nonlinear circuit block such as the LDO under investigation can be described by the following nonlinear state equations

$$\begin{aligned}\dot{\mathbf{x}}(t) &= F(\mathbf{x}(t), \mathbf{u}(t)) \\ \mathbf{y}(t) &= G(\mathbf{x}(t), \mathbf{u}(t))\end{aligned} \tag{1}$$

where $\mathbf{u}, \mathbf{y} \in \mathbb{R}^P$ denote the input and output port quantities (voltages and currents) in a given representation (impedance, admittance or hybrid) and $\mathbf{x}, \dot{\mathbf{x}} \in \mathbb{R}^N$ are the system state vector and its time derivative. These state variables correspond to the dynamic elements in the network, including a large amount of parasitic capacitances and inductances as extracted from a post-layout realization.

We are interested in the circuit behavior under small-signal assumptions. These assumptions are verified in the adopted case study due to the nature of the VR, which aims at guaranteeing that the regulated voltage fluctuations are small with respect to the nominal value. Under small-signal operation, all involved signals can be written as

$$\begin{aligned}\mathbf{u}(t) &= \bar{\mathbf{u}} + \tilde{\mathbf{u}}(t) \\ \mathbf{y}(t) &= \bar{\mathbf{y}} + \tilde{\mathbf{y}}(t) \\ \mathbf{x}(t) &= \bar{\mathbf{x}} + \tilde{\mathbf{x}}(t)\end{aligned} \tag{2}$$

where $\bar{\mathbf{u}}, \bar{\mathbf{y}}, \bar{\mathbf{x}}$ are the constants DC terms and $\tilde{\mathbf{u}}(t), \tilde{\mathbf{y}}(t), \tilde{\mathbf{x}}(t)$ are small amplitude time varying components. Small signal dynamics is readily described by means of circuit linearization. When $\tilde{\mathbf{u}}(t)$ is turned off, the presence of $\bar{\mathbf{u}}$ at the circuit terminals leads to the steady state quantities $\bar{\mathbf{y}}, \bar{\mathbf{x}}$ for states and output, provided that the circuit works around a unique, stable operating point. As a consequence, response of the system to $\tilde{\mathbf{u}}(t)$ is described by a first-order Taylor approximation of (1)

$$\begin{aligned}\dot{\tilde{\mathbf{x}}}(t) &\approx \mathbf{A}(\bar{\mathbf{u}})\tilde{\mathbf{u}}(t) + \mathbf{B}(\bar{\mathbf{u}})\tilde{\mathbf{u}}(t) \\ \tilde{\mathbf{y}}(t) &\approx \mathbf{C}(\bar{\mathbf{u}})\tilde{\mathbf{u}}(t) + \mathbf{D}(\bar{\mathbf{u}})\tilde{\mathbf{u}}(t)\end{aligned} \tag{3}$$

where $\mathbf{A}(\bar{\mathbf{u}}) \in \mathbb{R}^{N\times N}$, $\mathbf{B}(\bar{\mathbf{u}}) \in \mathbb{R}^{N\times P}$, $\mathbf{C}(\bar{\mathbf{u}}) \in \mathbb{R}^{P\times N}$, $\mathbf{D}(\bar{\mathbf{u}}) \in \mathbb{R}^{P\times P}$. The dependency of the state space matrices on $\bar{\mathbf{x}}$ is dropped, since the operating point is assumed to be unique for a given $\bar{\mathbf{u}}$. It is easily shown by means of the superposition principle, that when fed with the complete input defined in (2), the linearized state space model (3) will reproduce the true response of the non-linear circuit only up to a constant offset. This simple consideration is the main guideline for the development of the modeling framework, discussed next.

IV. Modeling flow

Our objective is to build an equivalent circuit able to replace (1) during on-line transient analysis: when fed with a generic input $\bar{\mathbf{u}} + \tilde{\mathbf{u}}(t)$ including both bias and small-signal terms, this circuit must return an accurate approximation of the output $\bar{\mathbf{y}} + \tilde{\mathbf{y}}(t)$ of the original CB. The proposed modeling strategy is twofold: in a first step, a reduced-order parameterized approximation of (3) is achieved, by embedding in a closed form the dependence on $\bar{\mathbf{u}}$ within its range of variation according to the current design. This first step provides an accurate approximation of the small-signal component $\tilde{\mathbf{y}}(t)$ of the output. Then, the proper DC output of the original non-linear circuit is recovered by off-setting the model response through a bias-dependent correction.

A. Modeling Small-Signal Dynamics

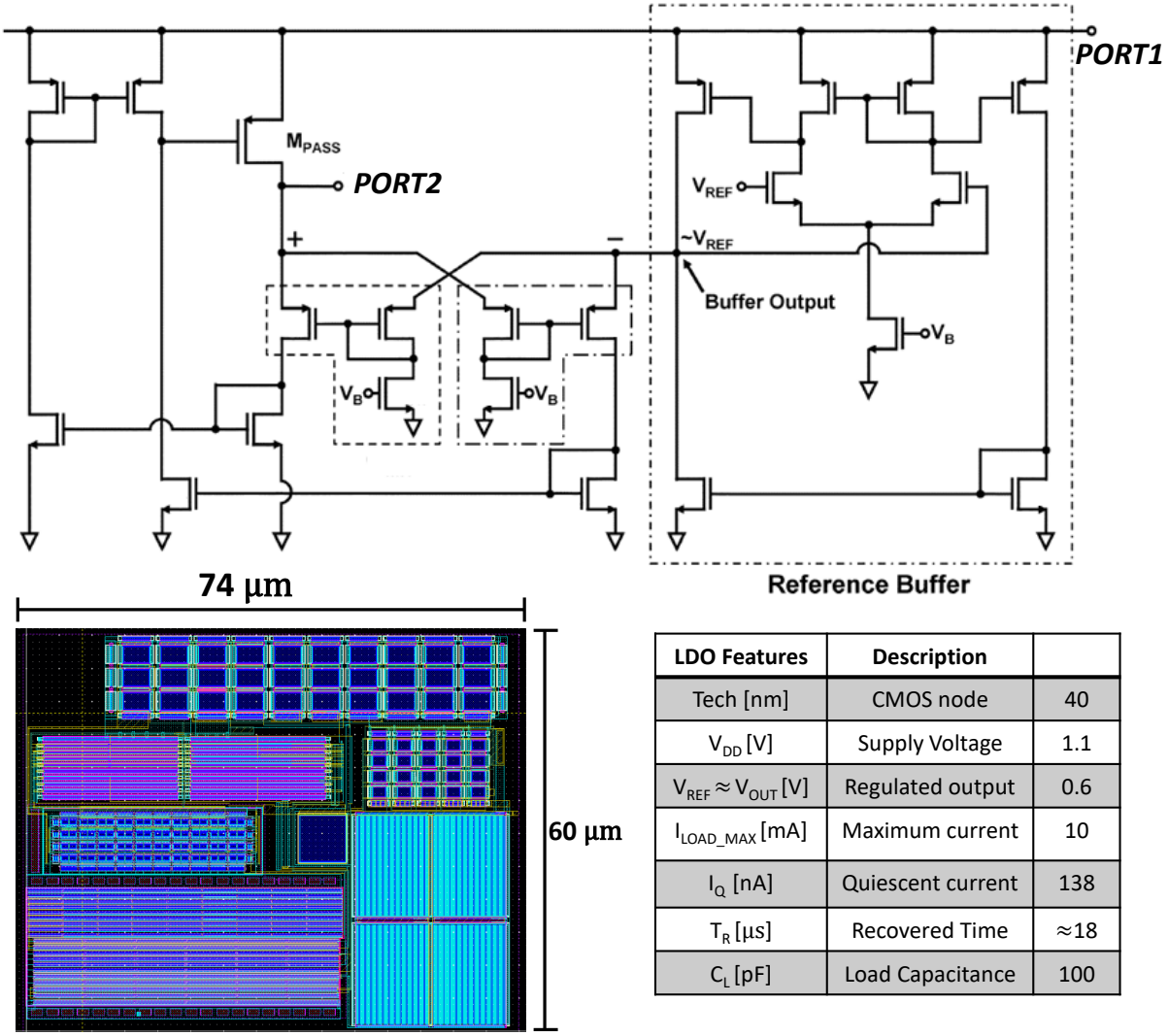
In most cases, the explicit formulation of (1) is not avalaible, since embedded in the circuit description that is adopted by the CAD software suite being used to carry out the design. Therefore, it is not possible to derive the exact circuit linearization for any given operating point by explicitly evaluating the Jacobians of (1). For this reason, we work in a purely black-box behavioral setting. A reduced-order state-space macromodel (3) is obtained as in standard data-driven macromodeling techniques [3], [4], starting from a sweep of small-signal frequency (AC) responses throughout the bias range.

The components of $\bar{\mathbf{u}} = [\bar{u}^1, \bar{u}^2, ..., \bar{u}^P]^T$ are the external parameters that we want to embed in closed-form in the behavioral model (3). Here we assume that DC components of the input at every port, $\bar{u}^p$, are allowed to vary within a closed continuous interval, which is defined by circuit design specifications. Thus, $\bar{\mathbf{u}} \in \mathcal{U} \subset \mathbb{R}^P$, where $\mathcal{U}$ is a compact domain, which we call the bias space. For any given value of $\bar{\mathbf{u}} \in \mathcal{U}$, the corresponding small-signal responses are computed through an AC analysis of the adopted circuit solver, applied to the full LDO model. We thus obtain a set of "virtual measurements"

$$breve{\mathbf{H}}_{k,m} = \breve{\mathbf{H}}(\mathrm{j}\omega_k; \bar{\mathbf{u}}_m) \quad k = 1, 2, ..., K, \quad m = 1, 2, .., M \tag{4}$$

where $\omega_k \in \Omega$ is the frequency range of interest. The above set constitutes the raw data from which we extract the reduced-order model. The discrete samples $\bar{\mathbf{u}}_m \in \mathcal{U}$ correspond to specific bias configurations for which the response is computed and result from a bias space sampling process, which can be static (e.g., a multiple nested linear sweep), or adaptive [13].

The frequency samples (4) are subjected to a multivariate rational approximation process within the framework of the



LDO Features	Description	
Tech [nm]	CMOS node	40
V_{DD} [V]	Supply Voltage	1.1
$V_{REF} \approx V_{OUT}$ [V]	Regulated output	0.6
I_{LOAD_MAX} [mA]	Maximum current	10
I_Q [nA]	Quiescent current	138
T_R [µs]	Recovered Time	≈18
C_L [pF]	Load Capacitance	100

Fig. 1: Schematic diagram, layout, and main parameters of the LDO under investigation.

Parameterized Sanathanan Koerner (PSK) algorithm [6], [14], [15], which returns a model of the form

$$\mathbf{H}(s;\bar{\mathbf{u}}) = \frac{\mathbf{N}(s;\bar{\mathbf{u}})}{D(s;\bar{\mathbf{u}})} = \frac{\sum_{n=0}^{\bar{n}} \sum_{\ell=1}^{\bar{\ell}} \mathbf{R}_{n,\ell}\, \xi_\ell(\bar{\mathbf{u}})\, \varphi_n(s)}{\sum_{n=0}^{\bar{n}} \sum_{\ell=1}^{\bar{\ell}} r_{n,\ell}\, \xi_\ell(\bar{\mathbf{u}})\, \varphi_n(s)} \quad (5)$$

where $\varphi_n(s)$ is a set of fixed partial fraction basis as in VF [3], and $\xi_\ell(\bar{\mathbf{u}})$ is a family of multivariate basis functions in P variables, identified by a global index ℓ. These functions implicitly parameterize poles and zeros of the model through the constant coefficients $\mathbf{R}_{n,\ell} \in \mathbb{R}^{P\times P}$ and $r_{n,\ell} \in \mathbb{R}$. In this work, we use multivariate Chebychev polynomials as $\xi_\ell(\bar{\mathbf{u}})$, although other kinds of functions have been proposed [7]. We remark that a standard realization process can be applied to (5) to cast it as a parameter-dependent state-space system in form (3). The latter is readily converted and synthesized as an equivalent SPICE netlist, as discussed in [8].

The stability of the model over the entire bias space is guaranteed by construction, by imposing positive realness of the denominator

$$\Re\{D(\mathrm{j}\omega;\bar{\mathbf{u}})\} > 0, \quad \forall \bar{\mathbf{u}} \in \mathcal{U}, \quad \forall \omega. \quad (6)$$

When this condition is verified, all zeros of $D(s;\bar{\mathbf{u}})$ are automatically constrained to the left half of the complex plane. Since these zeros coincide with the poles of $\mathbf{H}(s;\bar{\mathbf{u}})$, uniform stability conditions are met. The practical enforcement of (6) is obtained by embedding it as a constraint through the various iterations of the PSK algorithm. For technical and implementation details, the Reader is referred to [8], [9].

B. DC Output Correction

Let us assume that a DC steady-state analysis is performed on the model (5), by feeding its ports with constant signals having values corresponding to a given bias configuration $\bar{\mathbf{u}}_i$. The resulting DC response is obtained as

$$\hat{\mathbf{y}}_i = \mathbf{H}(0;\bar{\mathbf{u}}_i)\bar{\mathbf{u}}_i \quad (7)$$

and is in general different from the true DC response $\bar{\mathbf{y}}$ of the original nonlinear CB when subjected to the same DC excitation. Therefore, a direct replacement of the nonlinear CB with the small-signal macromodel (5) would lead to a wrong DC output, and a (parameterized) DC correction $\mathbf{\Delta}(\bar{\mathbf{u}})$ is required so that

$$\bar{\mathbf{y}} = \mathbf{H}(0;\bar{\mathbf{u}})\bar{\mathbf{u}} + \mathbf{\Delta}(\bar{\mathbf{u}}) \quad \forall \bar{\mathbf{u}} \in \mathcal{U}. \tag{8}$$

Such DC correction is here obtained as follows. First, we run a set of nested DC sweeps on the original CB by computing a discrete set of DC responses

$$\breve{\mathbf{y}}_i = G(\bar{\mathbf{x}}_i;\bar{\mathbf{u}}_i) \quad i = 1,2,...I, \quad \bar{\mathbf{u}}_i \in \mathcal{U} \tag{9}$$

where the bias configurations $\bar{\mathbf{u}}_i$ are determined so that the DC response behavior over the full set $\mathcal{U}$ is well characterized. The corresponding DC model offset at these discrete points is computed as

$$\breve{\mathbf{\Delta}}_i = \breve{\mathbf{y}}_i - \hat{\mathbf{y}}_i \tag{10}$$

Each component of $\breve{\mathbf{\Delta}}_i$ provides a sample of a hypersurface in a P-dimensional space corresponding to the coordinates of $\mathbf{u}_i$. We then parameterize all components of $\mathbf{\Delta}(\bar{\mathbf{u}})$ through the approximation

$$\mathbf{\Delta}(\bar{\mathbf{u}}) = \sum_{c=1}^{C} \mathbf{p}_c \, \xi_c(\bar{\mathbf{u}}) \tag{11}$$

where $\xi_c(\bar{\mathbf{u}})$ are multivariate Chebychev polynomials. The vector-valued coefficients $\mathbf{p}_c$ are determined by solving the following linear regression problem

$$\mathbf{\Delta}(\bar{\mathbf{u}}_i) \approx \breve{\mathbf{\Delta}}_i \quad \forall i \tag{12}$$

in least squares sense. Finally, the DC correction (11) is applied in form of parameterized DC sources connected at the output ports of a circuit realization of the small-signal macromodel (3). See also [16], [17].

V. Results

We validate the proposed behavioral modeling flow on the LDO test case presented in Sec. II and Fig. 1. All simulations that follow were computed using Cadence 6.1.7-64b + Spectre 18.1.0-64b enviroment into a HP Proliant DL580 Server featuring 72-parallel-CPU Intelš Xeonš Gold 6140M and 128G RAM.

The original CB is characterized through its two-port ($P = 2$) small-signal hybrid matrix $\mathbf{H}$, so that

$$\begin{pmatrix} i_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ i_2 \end{pmatrix} \tag{13}$$

where port 1 denotes the supply (non-regulated voltage) port and port 2 the output (regulated voltage) port . Therefore, with reference to the notation used in the paper, the input components are $u_1 = v_1$ and $u_2 = i_2$. Correspondingly, the two parameters upon which the model depends are the nominal bias voltage $\bar{u}_1 = \bar{v}_1 = V_{DD} \in [0.9, 1.1]$ V and the output load current $\bar{u}_2 = \bar{i}_2 = -I_L$ with $I_L \in [0, 10]$ mA.

A small-signal model (3) was obtained with the proposed stability-constrained parameterized SK algorithm using $K = 125$ data points logarithmically spaced over a frequency band $\Omega = [0, 10]$ GHz, in order to demonstrate full-band model accuracy with respect to the original CB. The raw frequency data used for model identification were obtained through repeated AC sweeps applied to the post-layout netlist with 625 different bias configurations, obtained as a Cartesian product of independent sweeps on $\bar{u}_1$ (25 points) and $\bar{u}_2$ (25 points). Only a subset of $M = 208$ points were used for model identification, leaving the other points for model self-validation. An accurate fit required $\bar{n} = 9$ parameter-dependent model poles, with polynomial orders $(\bar{\ell}_1, \bar{\ell}_2) = (4, 4)$ in the model numerator and $(\bar{\ell}_1, \bar{\ell}_2) = (3, 3)$ in the model denominator for parameters $\bar{u}_1$ and $\bar{u}_2$, respectively.

Figure 2 compares the four frequency responses of the small-signal model with the corresponding raw data. In the left panels the bias current is fixed to $I_L = 10$ mA and different values of bias voltage are swept within its range $[0.9, 1.1]$ V. In the right panels the bias voltage is fixed to $V_{DD} = 1$ V and different values of load current are swept within its range $[0, 10]$ mA. From the response H_{21}, which represents the voltage regulation properties of the LDO, we see that for small values of V_{DD} the LDO looses effectiveness. A resonance is clearly visible around 100 kHz, which delimits the regulation bandwidth. All these plots confirm the uniform accuracy of the model with respect to the small-signal responses of the original CB. Note that all raw responses are depicted in the figure, including both fitting and validation responses.

Figure 3 reports the parameter-dependent DC correction on the output port 2. Top panel compares the discrete points $\breve{\mathbf{\Delta}}_i$ computed on the raw data as in (10), which are used to fit the parameterized DC correction model (11), depicted by a colored surface. Both surfaces are in good agreement and are hardly distinguishable on this plot. Bottom panel reports the parameter-dependent (absolute) error on the correction term resulting from the least squares fit (12), which is below 10^{-3} in the bias space except for small regions at its corners.

A full model validation including both DC correction and small-signal components is demonstrated in Fig. 4, where the model transient response is compared to the same response of the original post-layout LDO. In this scenario, we used a nominal bias configuration $V_{DD} = 1$ V and $I_L = 5$ mA. Then, we applied on top of this bias a transient voltage excitation at port 1, consisting of two tones at 866 Hz and 1414 Hz, both having 60 mV amplitude. From this figure, we note that the LDO behaves as expected, by reducing a peak-to-peak noise of more than 100 mV down to about 6 mV. Second, we see no difference between model responses and nonlinear LDO responses. The figure only depicts a snapshot of 20 ms out of the computed 100 ms span. The simulation of the original post-layout LDO required 258 s, whereas the behavioral model required only 362 ms, with a speedup factor larger than 700×. We remark that both full-size LDO netlist (more than 30 MB netlist size) and behavioral model (few kB netlist size) were instantiated and solved using the same hardware/software environment, so that runtimes are directly comparable.

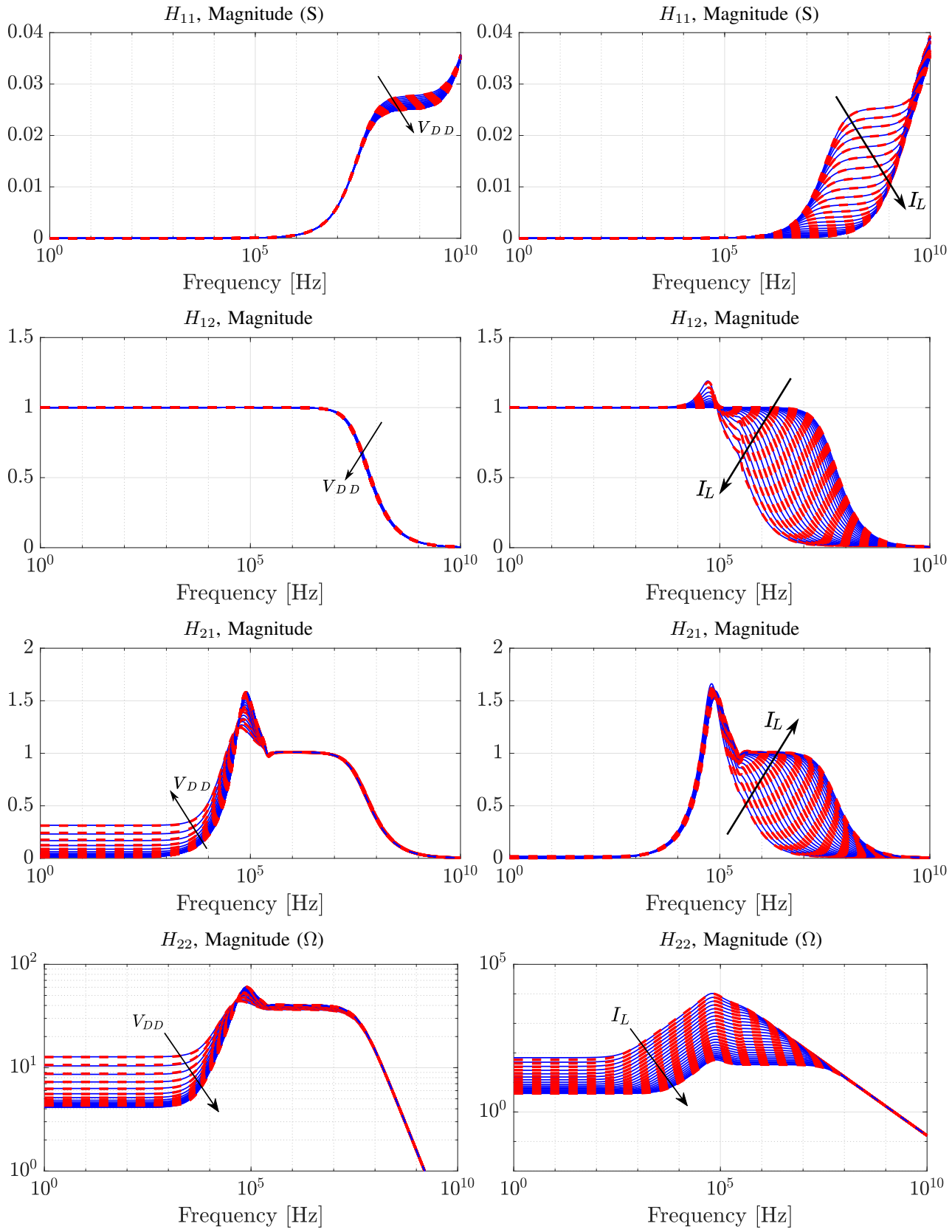


Fig. 2: Comparison between model responses (dashed red lines) and raw data (blue solid lines). Left panels: fixed bias current $I_L = 10$ mA and different values of bias voltage within its range $[0.9, 1.1]$ V. Right panels: fixed bias voltage $V_{DD} = 1$ V and different values of load current within its range $[0, 10]$ mA.

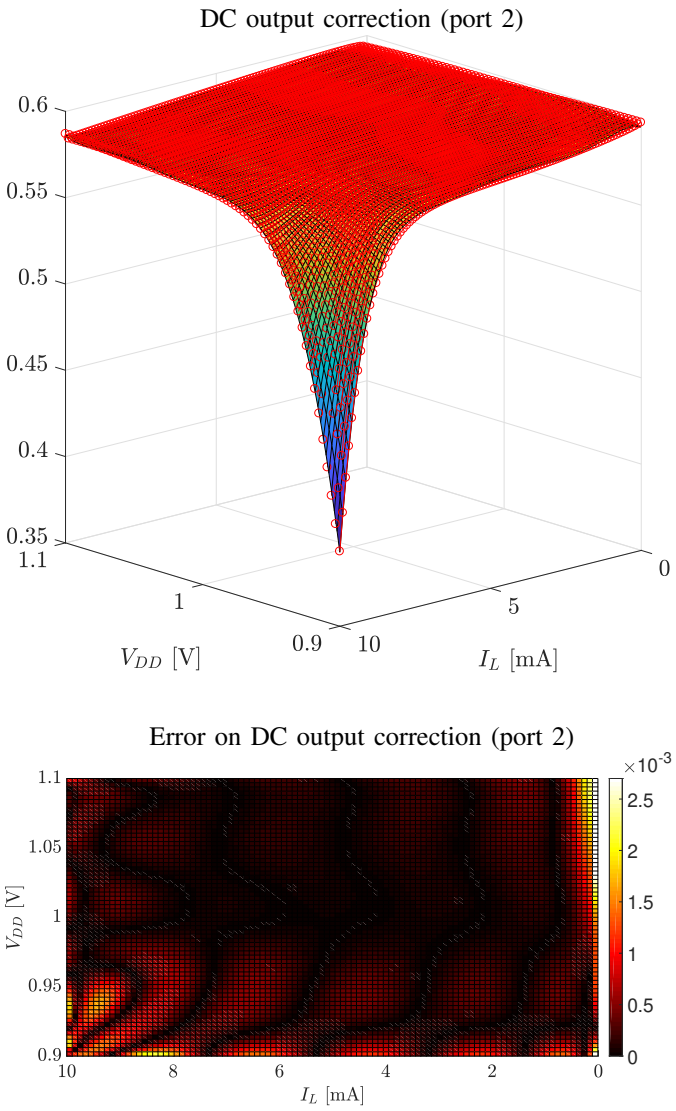


Fig. 3: Top: DC correction model (solid surface plot) compared to raw identification points (red dots) used for its estimation. Bottom: parameter-dependent error of the DC correction model.

VI. Conclusions

We have presented a behavioral modeling approach that automatically produces parameterized surrogate models that can replace complex nonlinear circuit blocks at practically no accuracy loss. The results obtained by applying proposed method to an LDO voltage regulator demonstrate a speedup of almost three orders of magnitude in transient analysis with respect to a post-layout extracted netlist. Therefore, this approach may become a key enabling factor for fast power integrity transient verification, including monte-carlo and statistical assessments.

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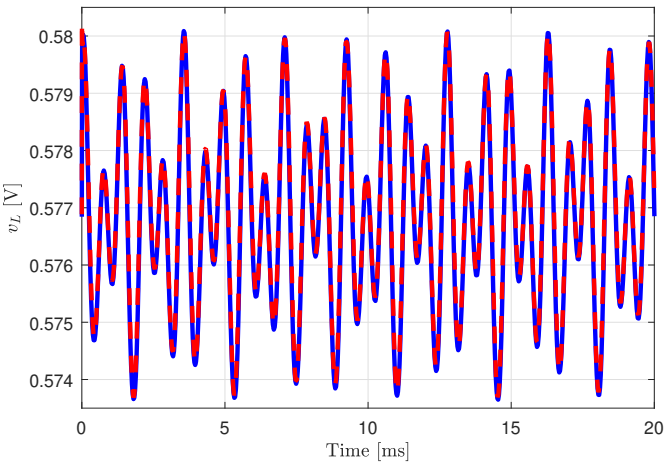

Fig. 4: Simulated output voltage output of model (dashed red line) and post-layout LDO netlist (blue solid line).

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