Constructive Signal Approximations for Fast Transient Simulation of Coupled Channels

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***Abstract*—This paper addresses the problem of fast transient simulation of high-speed coupled channels driven by transceivers that include Transmitter Feed-Forward Equalization (TX-FFE). Practical circuit hardware implementations of such drivers may not be correctly represented by industry standard algorithmic modeling interfaces, which are usually based on ideal digital finite impulse response filters. In particular, slow transients may arise when aggressive FFE is activated and particular switching sequences significantly stress local voltage regulators integrated in the output buffers. In this paper, we model this effect using a constructive hierarchical approximation of the analog waveforms that form a linearized vector Thevenin or Norton representation of the driver. This representation enables the accurate simulation of coupled channels including both differential and common-mode signals. Analog waveforms at the receiver input are readily obtained by standard time-frequency transformations, while including channel characteristics and any additional linear equalization block, if present. This proposed framework is compatible with industry-standard Algorithmic Modeling Interfaces (AMI), extending their scope to coupled channels with non-ideal TX-FFE circuit blocks. Eye diagrams and transient waveforms corresponding to millions of bits are computed in few seconds using a non-optimized software implementation. Random jitter and crosstalk are seemlessly included as in standard AMI frameworks. The results of various numerical experiments on commercial transceivers are reported in this paper, confirming both the accuracy and the efficiency of the proposed framework.**

***Index Terms*—Modeling, digital integrated circuits, LVDS buffers, differential drivers, signal integrity, high-speed signaling, equalization, pre-emphasis, de-emphasis, feed-forward equalization.**

I. Introduction

The design of high performance electronic equipment, such as smartphones, tablets and PCs, requires a careful characterization of the non-ideal behavior of the entire end-to-end electrical interconnects, in order to evaluate any detrimental effect on the overall system reliability. This is even more important in the most recent and modern devices, whose high-speed wired communication interfaces (e.g., between the application processors and other specialized integrated circuits or pheripherals) have been constantly improved over the years in order to support higher and higher data rates. Faster signaling inevitably leads to more likely and stronger distortion effects due to interconnect nonidealities, like losses, attenuation, dispersion, impedance mismatches and return path discontinuities, to name just a few. Such effects can significantly affect the reliability of hardware implementations, whose first-pass quality has become a must in order to comply with very short time-to-market requirements.

In this context, a key role is played by full-channel analog simulations, aimed at assessing the link signal and power integrity [1], [2]. For data rates in Gb/s range (e.g., 8, 10, 16 Gb/s or more), attenuation and dispertion introduced by interconnets can be partly compensated using equalizers in high-speed transceivers. For these devices, macromodel-based simulations have been proven to be the only viable solution, since the computational burden required by a full-detail transistor-level description cannot be handled in realistic simulation times. Macromodels avoid this problem by replacing the detailed models with much more compact and efficient surrogates, without significant loss in accuracy.

In the past twenty years many efforts have been spent by both industry and academia to provide efficient macromodeling solutions with tunable accuracy, ranging from the standard approach based on the Input/Output Buffer Information Specification (IBIS) [3], [4] to more elaborate techniques based on either circuit-inspired equivalents of blind black-box representations [5]–[12]. For the latter set, more recent enhancements and applications are available in [13]–[18].

All the above approaches, however, share the same limitation of dealing with nonlinear model representations and even if the proposed surrogates are more the one order of magnitude times faster than transistor-level models, the efficiency improvement is not enough to process millions of bits in a reasonable amount of time. The only available solution widely recognized by the industry and which has been successfully implemented in most of the commercial state-of-the-art tools is represented by the Algorithmic Modeling Interface (AMI) extension of IBIS. IBIS-AMI offers a linear modeling and simulation tool where Transmitter Feed-Forward Equalization (TX-FFE) is accounted for by a suitable post-processing of the differential signal flowing through the communication channel. Even if the simulation speed allowed by this technique is appropriate for modern CAD flows, the limited accuracy in reproducing the rich dynamical effects of recent transceivers, including the common-mode signal in coupled channels, demand for improvements.

This paper extends the preliminary results presented in [19] and discusses a novel high-speed serial link simulation method based on a different linear modeling framework. The proposed

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approach aims at evaluating the transient waveforms at the receiver side of the channel, for arbitrarily long bit sequences, and in just a few seconds. Both differential- and common-mode waveforms are predicted with a tunable accuracy depending on the number of hierarchical basis functions, which are introduced in the model to account for possible broadband and even long-term memory effects caused by switching mechanisms within the transceiver circuits. This phenomenon may be hard to model within the IBIS-AMI framework, which relies on time invariance since based on weighted precursors and postcursors that are just rescaled versions of the same elementary pulse. The proposed signal representation overcomes this limitation through successive hierarchical refinements that are shown to converge to the reference responses.

The proposed signal construction process is nonlinear and adaptive, depending on the particular binary sequence being transmitted. However, linear superposition fits in the analog part of the signal processing flow, thus enabling to compute the transient responses via either frequency-domain (e.g., Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT)) or time-domain approaches (e.g., recursive convolution). We adopt the former frequency-domain approach, which naturally plugs into the existing IBIS-AMI framework by suitably extending its scope and applicability.

The paper is then organized as follows. Section II derives the proposed model representation for differential transceivers from the well known nonlinear model structures used so far in the literature. Section III presents the step-by-step procedure for model generation, via a set of simple simulations of the reference transistor-level models of devices connected to predefined loads. Model extension involving the above mentioned hierarchical bases for TX-FFE representation is illustrated in Sec. IV. Section V discusses the fast channel simulation via a mixed time and frequency-domain approach and Sec. VI collects the numerical results based on the application of the proposed technique to two commercial devices, demonstrating its feasibility and strength. Final remarks and conclusions are given in Section VII.

II. Modeling multiport transceivers

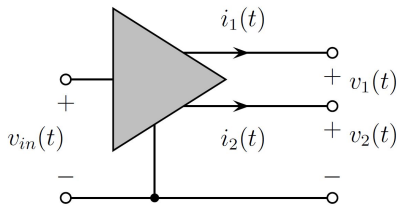

Fig. 1. Typical structure of a differential driver with its relevant port variables.

Our proposed modeling framework is based on a generic multiport (differential) driver structure, as depicted in Fig. 1, where the individual single-ended output currents $i_{1,2}$ and voltages $v_{1,2}$ are defined. These are readily converted, if desired, into differential and common-mode quantities, as

$$v_d = v_1 - v_2, \quad v_c = \frac{v_1 + v_2}{2}. \tag{1}$$

Similarly, conversion to single-ended and/or differential scattering representations in terms of incident and reflected transient wave signals can be considered too, leading to a pure scattering formulation as in [22]. In the following, we base our derivations to single-ended voltages and currents for simplicity of illustration, but any other representation that can be linearly related to such variables can be adopted as a starting point as well. Our numerical implementation is based on single-ended scattering variables for improved numerical robustness.

With reference to Fig. 1, we propose the following model structure

$$\boldsymbol{i}(t) = -\boldsymbol{G}\boldsymbol{v}(t) + \boldsymbol{j}(t) + \boldsymbol{g}(\boldsymbol{v}(t)) \tag{2}$$

where vectors $\boldsymbol{i} = [i_1, i_2]^T$ and $\boldsymbol{v} = [v_1, v_2]^T$ collect the port variables. In (2) we recognize various terms as follows:

- the static behavior of the output port currents is captured by a constant conductance matrix $\boldsymbol{G}$;
- the dynamic behavior of the driver when excited at its output by the voltages $\boldsymbol{v}$ is represented by a dynamical Linear Time-Invariant (LTI) submodel $\boldsymbol{g}$;
- the time-varying source term $\boldsymbol{j}(t) = [j_1(t), j_2(t)]^T$ represents the switching activity of the driver as a time-varying analog waveform. This switching activity results from the particular bit pattern imposed by the inner stages of the driver, which are represented in Fig. 1 by the voltage $v_{in}(t)$.

The model structure (2) is indeed a particular case of two well-established formats for behavioral transceiver representation, namel the IBIS standard and the MpiLog framework [4], [6], [8], [17], see also [23]. We recall that basic Mpilog models are written as time-varying combinations of two-piece dynamical submodels as

$$\boldsymbol{i}(t) = \boldsymbol{w}_H(t)\boldsymbol{F}_H(\boldsymbol{v}(t)) + \boldsymbol{w}_L(t)\boldsymbol{F}_L(\boldsymbol{v}(t)) \tag{3}$$

where $\boldsymbol{F}_\nu$ with $\nu \in \{H, L\}$ are nonlinear dynamical multivariate relations accounting for the static and the dynamic behavior of the driver in fixed logic states, and $\boldsymbol{w}_\nu$ are time varying switching functions. A very similar structure holds for IBIS [4], with some simplifications. The proposed model structure (2) can be readily derived from (3) under the following assumptions:

- the two switching functions describing the analog transitions $L \to H$ and $H \to L$ are constrained to be symmetric through $\boldsymbol{w}_H(t) = 1 - \boldsymbol{w}_L(t)$, which effectively represents switching behavior through a single time-domain signal;
- the $\boldsymbol{F}_\nu$ submodels, which can be highly nonlinear and dynamic in some applications [6], [9], [10], are here approximated by LTI compact models through

$$\boldsymbol{F}_\nu(\boldsymbol{v}) = -\boldsymbol{G}_\nu\boldsymbol{v} + \boldsymbol{I}_\nu + \boldsymbol{g}_\nu(\boldsymbol{v}), \quad \nu \in \{H, L\} \tag{4}$$

  where the conductance matrices $\boldsymbol{G}_\nu$ and the static bias current vectors $\boldsymbol{I}_\nu$ define linear multivariate static characteristics (in Norton form) approximating the static behavior of the device in each logic state (see Fig. 2 (top panel), which considers the behavior of a commercial 90-nm low-power driver available as a transistor-level encrypted netlist [21]); we denote with $\boldsymbol{g}_\nu$ the two LTI

submodels that reproduce the dynamical response of the device.

Using the two above simplifications in (3) leads to

$$\begin{aligned} \boldsymbol{i}(t) &= w_H(t)\left[-\boldsymbol{G}_H\boldsymbol{v}+\boldsymbol{I}_H+\boldsymbol{g}_H(\boldsymbol{v})\right]+ \\ &+(1-w_H(t))\left[-\boldsymbol{G}_L\boldsymbol{v}+\boldsymbol{I}_L+\boldsymbol{g}_L(\boldsymbol{v})\right] \end{aligned} \tag{5}$$

Introducing now the additional assumption that the driver is symmetric in both its static and dynamic parts, the representation in (5) can be recast as in (2), where:

$$\boldsymbol{G}=\boldsymbol{G}_H=\boldsymbol{G}_L, \quad \boldsymbol{g}=\boldsymbol{g}_H=\boldsymbol{g}_L \tag{6}$$

and

$$\boldsymbol{j}(t)=\left[w_H(t)\boldsymbol{I}_H+(1-w_H(t))\boldsymbol{I}_L\right]. \tag{7}$$

Assumption (6) may appear overly restrictive, but extensive numerical tests on various benchmark cases demonstrated that the accuracy loss is negligible when modeling high-speed differential drivers. In particular, this assumption is crucial for ensuring computational efficiency.

III. Constructing Transceiver Models

Model parameters can be readily obtained via a simple estimation procedure based on a set of Transistor-Level (TL) simulations. Specifically, the 2×2 matrix $\boldsymbol{G}$ and the vectors $\boldsymbol{I}_\nu$, defining the approximated linear static characteristics are computed via simple least-squares fits from the real static multivariate surfaces of the device response when operating in a fixed logic state. These responses are extracted by a set of double DC sweeps computed, e.g., in SPICE. The proposed linear approximation corresponds to two planes, depicted for a test driver in Fig. 2 (top panel) in gray solid color. Note that these two planes corresponding to H and L static characteristics are parallel, since we enforce $G_H=G_L=G$, while the DC current offsets I_H and I_L define the reference bias levels of each logic state. The figure shows that the approximation of the actual DC characteristics with parallel planes is excellent, as highlighted by the error surfaces shown in the bottom panel of Fig. 2. The error in magnitude turns out to be always less than $0.5\,\mathrm{mA}$ in the full considered region of the port voltages v_1 and v_2. In particular, the above mentioned error is one order of magnitude less (i.e., $<50\,\mu\mathrm{A}$) in the zone explored during normal operation of the device (see the black stars in the top panel), thus enabling the proposed modeling assumption.

The switching sources $\boldsymbol{j}(t)$ are instead computed from (2) from a set of current and voltage responses of the driver switching on a given load, according to the setup in the top panel of Fig. 3. The device is driven to produce a set of complete transition events, i.e., a "010" bit pattern, allowing to generate the basic switching sources associated to the corresponding up or down transitions. The load is chosen to cancel the effects of the dynamical contribution $\boldsymbol{g}$. For the $i-v$ representation (2), the above mentioned load corresponds to two ideal short circuits connected between the positive and negative output terminals of the device and ground, forcing $v_1=0$ and $v_2=0$. For the scattering representation which is indeed adopted in the present work, two single-ended $50\,\Omega$ resistors are considered instead. The switching term $\boldsymbol{j}(t)$ plays in our framework the same role of the weighting functions $\boldsymbol{w}_\nu(t)$ in standard IBIS/Mpilog models, providing in particular an effective behavioral representation of the TX-FFE blocks.

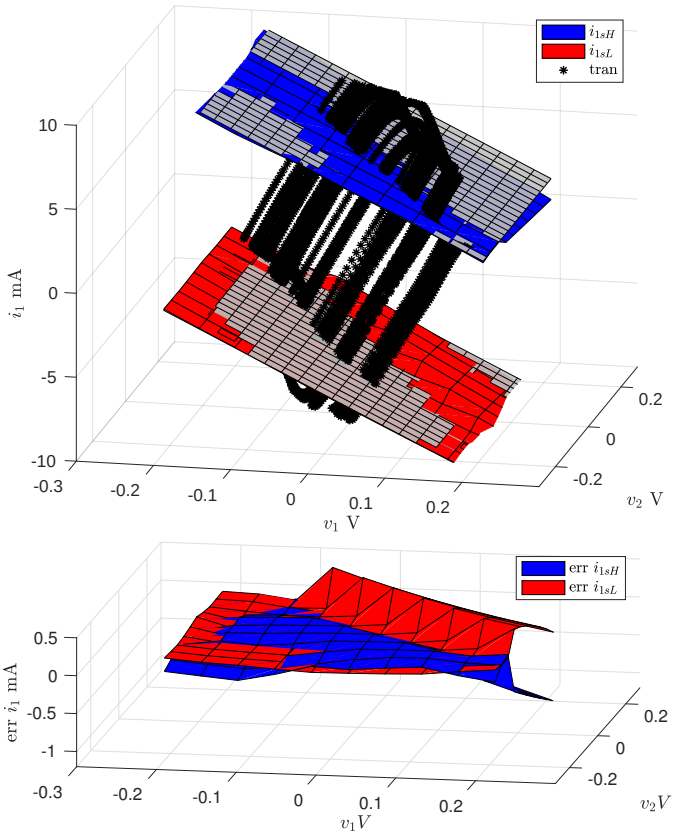

Fig. 2. Top Panel: trajectory of the current response $i_1(t)$ of an example driver during a real simulation test with a lossy channel (black stars). The trajectory is superimposed to the real and the approximated static characteristics of the driver in the fixed logic H or L states, i.e., i_{sH} and i_{sL}, respectively (gray color corresponds to the planes of the linear approximation). Bottom panel: error computed between the actual and the approximated static characteristics at the H (blue surface) and L (red surface) fixed logic state.

For the dynamical submodel $\boldsymbol{g}$, a multiport state-space structure is assumed, with parameters computed through a Time-Domain Vector Fitting (TDVF) process [20] applied to the transient responses of the currents $i_1(t)$ and $i_2(t)$ and voltages $v_1(t)$ and $v_2(t)$, collected when the driver switches on a transmission line load (see the testbench shown in the bottom panel of Fig. 3, where the far-end load consists of two resistors connected to an ideal voltage source forcing the nominal common mode voltage $V_{C,nom}$). We remark that the TDVF algorithm is able to identify a LTI system from its transient responses excited by arbitrary inputs. This feature is particularly useful here, since both inputs and outputs used for the identification of submodel $\boldsymbol{g}$ are known only implicitly and are obtained by extracting port voltages and currents from the results of a dedicated transient analysis testbench. As an example, Fig. 4 shows the transient voltages and current $i_1(t)$ for the above mentioned test case. Model prediction is included as well, highlighting its good accuracy in reproducing the rich dynamical behavior of the driver.

Differently from IBIS and Mpilog [4], [17], the proposed

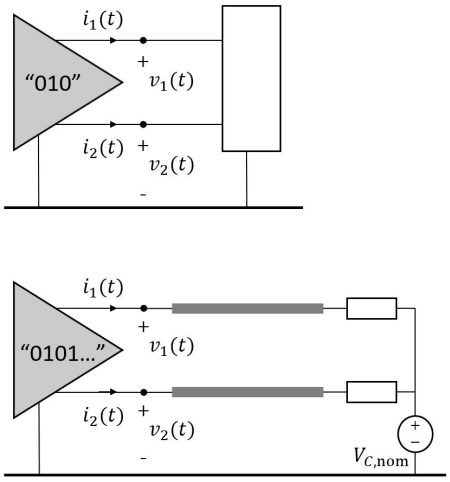

Fig. 3. Testbenches used for the collection of device responses required for model parameters estimation. Top panel: .TRAN analysis used for the computation of the switching terms $\boldsymbol{j}(t) = [j_1(t), j_2(t)]^T$; bottom panel: .TRAN analysis used for the computation of the dynamical submodel $\boldsymbol{g}$. See text for details.

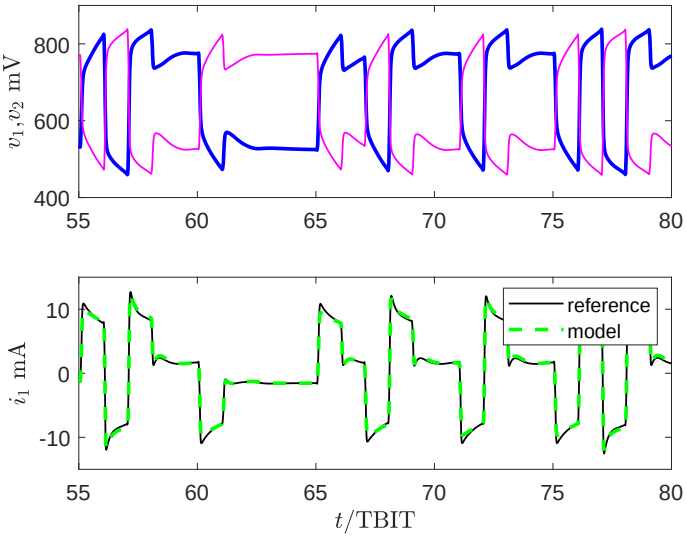

Fig. 4. Top panel: example transient responses of the voltages $v_1(t)$ and $v_2(t)$ collected when the driver switches on a transmission line load (see Fig. 3). Bottom panel: dynamical part of the response of the current $i_1(t)$ for the same test case, compared with the response of the dynamical submodel $\boldsymbol{g}$ for the first terminal current. The above waveforms, toghether with the companion response of $i_2(t)$ are used for the identification of $\boldsymbol{g}$.

model is completely linear, thus enabling frequency-domain methods for fast simulation. Differently from the widely-adopted IBIS-AMI standard (which is also based on linearity), the proposed model is better grounded in circuit theory and natively multivariate, thus allowing for an accurate representation of both the differential and the common mode signals.

IV. Modeling Long-Term Memory Effects of TX-FFE Blocks

We now consider embedding an appropriate representation of FFE blocks in the proposed driver model structure. Essentially, TX-FFE circuitry boost the driver strength when

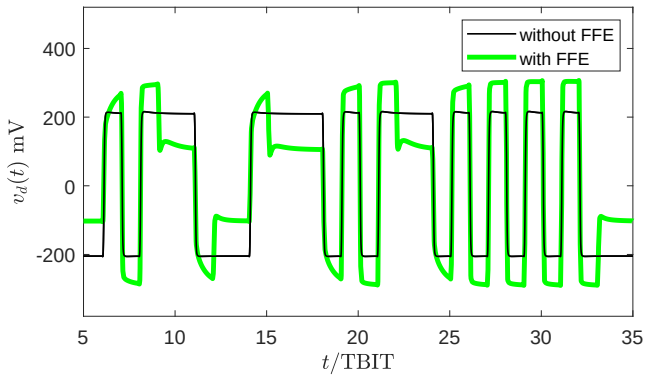

Fig. 5. Switching pattern of the differential voltage $v_d(t) = v_1(t) - v_2(t)$ with and without FFE for the example driver.

switching occurs, in order to induce a high-pass behavior that should compensate the inevitable low-pass characteristic of the channel due to metal and dielectric losses. Modern CAD tools for channel simulation and eye diagram construction embed effective and simple-to-use FFE blocks, which are commonly represented as Finite-Impulse-Responses (FIR) filters. Given a single-bit pulse $p(t)$ that would be applied without FFE activated, the enhanced pulse with FFE is represented as

$$\tilde{p}(t) = \sum_{r=-\underline{r}}^{\bar{r}} \alpha_r p(t - rT_B), \tag{8}$$

where T_B is the bit time, α_r are suitable weights used to design the FIR frequency response, and $\underline{r}, \bar{r}$ denote the number of *precursors* and *postcursors*, expressed as translated and rescaled identical replicas of the main pulse $p(t)$. When the boosted elementary pulse $\tilde{p}(t)$ is used for transmitting a given bit pattern $\{B_k \in \{0,1\}, k = 1, 2, \dots\}$, the resulting analog waveform is still expressed as a superposition of *identical* replicas of the initial pulse $p(t)$,

$$\sum_k B_k \tilde{p}(t - kT_B) = \sum_k \sum_{r=-\underline{r}}^{\bar{r}} B_k \alpha_r p(t - (r+k)T_B) \tag{9}$$

as a consequence of the assumed translation invariance.

Evidence collected from several numerical experiments challenges the above representation of the pre-emhpasis behavior. Let us consider Fig. 5, where the switching patterns of the example driver is depicted with and without its (1-tap) FFE activated. The analog waveform without FFE is well-described by a superposition of switching events with the same analog rising and falling fronts and can thus be represented as a weighted superposition of successive translations of a single and well-define pulse shape $p(t)$. Conversely, when FFE is enabled, we observe that the expected boosting effect is characterized by some slow transients: the maximum peak-to-peak amplitude of the waveforms is obtained after a few successive switchings, with a slow dynamic saturation effect. This effect makes each individual switching front different from each other, based on the number of earlier consecutive switching events. This effects has a well-defined extent in time, which can be estimated in Fig. 5 to last for about 4–5 bit times T_B for this particular device. We conclude that

a linear FIR approximation as in (8) is not adequate for this driver, since the shape of the switching fronts is not translation-invariant. What is instead required is a nonlinear description of the TX-FFE block, which is able to reproduce the switching front dependence on the number of immediately preceding consecutive switchings.

A. Hierarchical functions for FFE representation

The non-linear and adaptive representation of analog switching fronts that depend on the particular bit pattern is here obtained by a simple constructive approximation process. The main idea shares a common background with widely adopted adaptive approximation framework as those enabled by wavelet decompositions or image and video compression. An initial coarse-level approximation is derived, which provides a gross approximation of the response. Successive details are then added where a correction is required, in order to refine approximation. Corrections are added hierarchically through *levels*, until a sufficiently small approximation error is attained. The main enabling factor for proposed approach is the finite memory length in time of the TX-FFE analog behavior (see Fig. 5), which in turn induces sparsity, so that corrections need to be applied only locally and with a sparsity pattern that increases with increasing hierarchical levels.

Let us consider each of the two driver source components ($n = 1, 2$) in (7), which we detrend from their initial condition as $\xi_n(t) = j_n(t) - j_n(0)$, and which we represent through the following sparse hierarchical superposition

$$\xi_n(t) = \sum_{\ell=0}^{L} \Big[\sum_{k \in \Omega_{n,u}^{(\ell)}} \varphi_{n,u}^{(\ell)}(t - kT_B) + \sum_{k \in \Omega_{n,d}^{(\ell)}} \varphi_{n,d}^{(\ell)}(t - kT_B) \Big]. \tag{10}$$

The signal $\xi_n(t)$ is expressed as a superposition of individual $L \to H$ and $H \to L$ transitions, denoted respectively with the subscripts u, d. In (10), the index ℓ ranges through hierarchical approximation levels, up to a maximum level L. The construction of these levels is discussed below.

Let us first assume that no FFE is applied, so that no successive approximations are required. In such case, we set $L = 0$ (index ℓ is removed). The signal $\xi_n(t)$ is thus constructed as a sequence of individual transitions $L \to H$ and $H \to L$, centered respectively at time instants $k \in \Omega_{n,u}^{(0)}$ and $k \in \Omega_{n,d}^{(0)}$. The rising and falling fronts are represented through dedicated basis functions $\varphi_{n,u}^{(0)}(t)$ and $\varphi_{n,d}^{(0)}(t)$, respectively. If translation-invariance holds, then these two basis functions are sufficient to reconstruct all switching events. For instance, a single-bit pulse $p(t)$ can be represented with only two switching events as

$$p(t) = \varphi_{n,u}^{(0)}(t) + \varphi_{n,d}^{(0)}(t - T_B) \tag{11}$$

Consider now the case where FFE is activated, so that the shape of a switching event at $t = kT_B$ changes depending on the presence of another switching event at the *immediately* preceding time $t = (k-1)T_B$. We collect in sets $k \in \Omega_{n,u}^{(1)}$ and $k \in \Omega_{n,d}^{(1)}$ such switching instants. It is clear that

$$\Omega_{n,\nu}^{(1)} \subset \Omega_{n,\nu}^{(0)}, \quad \nu \in \{u, d\}, \tag{12}$$

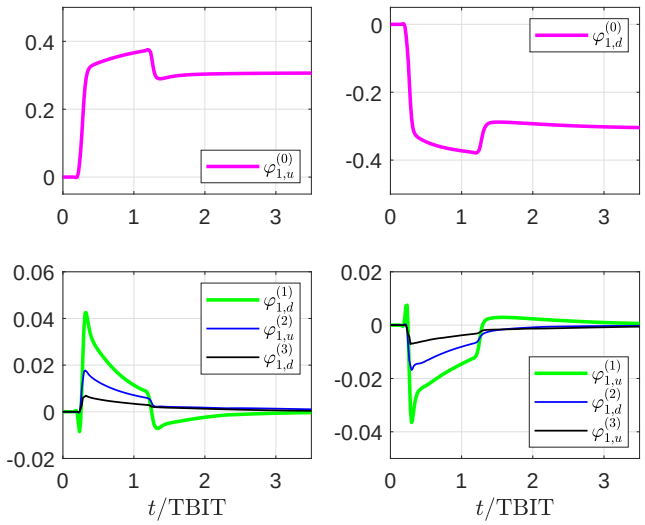

Fig. 6. Basis functions $\varphi_{n,u}^{(\ell)}(t)$ and $\varphi_{n,d}^{(\ell)}(t)$, for $n = 1$ and $\ell = \{0, 1, 2, 3\}$.

since there are switching events that are preceded by at least two non-switching intervals. We define two level-1 basis functions $\varphi_{n,u}^{(1)}(t)$ and $\varphi_{n,d}^{(1)}(t)$ as the local corrections that need to be applied to the level-0 approximation, in order to account for the difference in switching waveforms due to the presence of an immediately preceding switching event. We use these basis functions, centered at kT_B with $k \in \Omega_{n,u}^{(1)}$ and $k \in \Omega_{n,d}^{(1)}$, respectively, to obtain a refined approximation.

The process is then iterated through levels $\ell = 2, \ldots, L$, by identifying the index sets $k \in \Omega_{n,u}^{(\ell)}$ and $k \in \Omega_{n,d}^{(\ell)}$ corresponding to switchings that are preceded by at least ℓ *consecutive* switchings. Approprate basis functions $\varphi_{n,u}^{(\ell)}(t)$ and $\varphi_{n,d}^{(\ell)}(t)$ are used to represent the correction that is required locally at those instants. As a result, the hierarchical approximation (10) is obtained, where less and less basis functions are needed when the level ℓ increases, since by construction

$$\Omega_{n,\nu}^{(\ell)} \subset \Omega_{n,\nu}^{(\ell-1)}, \quad \nu \in \{u, d\}, \ \ell = 1, \ldots, L. \tag{13}$$

In addition to sparsity, the signal representation (10) has another very convenient feature. As depicted in Fig. 6, the amplitude of such basis functions decreases with increasing levels ℓ. This makes the proposed hierarchical representation more and more accurate as the levels increase, in a predictable and controllable manner. It is expected that uniform convergence holds to the exact signals, provided of course that no other sources of errors is present (e.g., the driver behaves exactly as a linear structure, which is not true in general).

As already mentioned, the size of the index sets $\Omega_{n,u}^{(\ell)}$ and $\Omega_{n,d}^{(\ell)}$ decreases when increasing ℓ, since the probability of occurrence of consecutive ℓ switching events decreases. These index sets are determined by a digital preprocessing of the logic bit sequence and they are exact, so that the computatioal complexity in the construction of the hierarchical approximation (10) is known in advance. Therefore, the signal construction is based on a nonlinear and adaptive approximation, which is however based on a sequence of iterative (through levels) linear superpositions of known basis functions.

B. Estimation of hierarchical basis functions

We now consider the construction of the basis functions $\varphi_{n,u}^{(\ell)}(t)$ and $\varphi_{n,d}^{(\ell)}(t)$. These are estimated for each level ℓ through a recursive peeling procedure, starting from a training response pair $\hat{\xi}_{n,u}^{(\ell)}$ and $\hat{\xi}_{n,d}^{(\ell)}$ computed using the reference TL driver model excited respectively by a pair of bit sequences $\mathcal{S}_u^{(\ell)}$, $\mathcal{S}_d^{(\ell)}$ that include all combinations of required switching patterns. Estimation is performed via incremental subtraction, while truncating the duration of transient sequences (the basis functions) at a time $\bar{T}_\ell$, determined when the expected steady-state is reached. In particular:

- at level $\ell = 0$, only isolated switching events are used to define the basis functions as

$$\mathcal{S}_u^{(0)} = \{\texttt{0,1,1,1,...}\}$$
$$\varphi_{n,u}^{(0)}(t) = \hat{\xi}_{n,u}^{(0)}(t)$$

  for the $\nu = u$ transition and

$$\mathcal{S}_d^{(0)} = \{\texttt{1,0,0,0,...}\}$$
$$\varphi_{n,d}^{(0)}(t) = \hat{\xi}_{n,d}^{(0)}(t)$$

  for the $\nu = d$ transition.
- at level $\ell = 1$, two consecutive switching events are used to define the basis functions as

$$\mathcal{S}_u^{(1)} = \{\texttt{0,1,0,0,0,...}\}$$
$$\varphi_{n,u}^{(1)}(t) = \hat{\xi}_{n,u}^{(1)}(t) - \varphi_{n,u}^{(0)}(t) - \varphi_{n,d}^{(0)}(t - T_B)$$

  for the $\nu = u$ transition and

$$\mathcal{S}_d^{(1)} = \{\texttt{1,0,1,1,1,...}\}$$
$$\varphi_{n,d}^{(1)}(t) = \hat{\xi}_{n,d}^{(1)}(t) - \varphi_{n,d}^{(0)}(t) - \varphi_{n,u}^{(0)}(t - T_B)$$

  for the $\nu = d$ transition.
- at level $\ell = 2$, three consecutive switching events are used to define the basis functions as

$$\begin{aligned}\mathcal{S}_u^{(2)} &= \{\texttt{0,1,0,1,1,1,...}\}\\ \varphi_{n,u}^{(2)}(t) &= \hat{\xi}_{n,u}^{(2)}(t)\\ &\quad - \varphi_{n,u}^{(0)}(t) - \varphi_{n,d}^{(0)}(t - T_B) - \varphi_{n,u}^{(0)}(t - 2T_B)\\ &\quad - \varphi_{n,u}^{(1)}(t) - \varphi_{n,d}^{(1)}(t - T_B)\end{aligned}$$

  for the $\nu = u$ transition and

$$\begin{aligned}\mathcal{S}_d^{(2)} &= \{\texttt{1,0,1,0,0,0,...}\}\\ \varphi_{n,d}^{(2)}(t) &= \hat{\xi}_{n,d}^{(2)}(t)\\ &\quad - \varphi_{n,d}^{(0)}(t) - \varphi_{n,u}^{(0)}(t - T_B) - \varphi_{n,d}^{(0)}(t - 2T_B)\\ &\quad - \varphi_{n,d}^{(1)}(t) - \varphi_{n,u}^{(1)}(t - T_B)\end{aligned}$$

  for the $\nu = d$ transition.
- at higher levels $\ell > 2$, the process is iterated by considering $\ell + 1$ consecutive switching events and defining the basis functions by removing all contributions required by the approximation of the training signals based on the basis functions at levels up to $\ell - 1$.

A graphical illustration of the estimated basis functions spanning four levels $\ell = 0, 1, 2, 3$ for the example driver of Fig. 5 is provided in Fig. 6.

V. Complete channel simulation and results

Once all basis functions $\varphi_{n,\nu}^{(\ell)}(t)$ are estimated from suitable identification signals, and the index sets $\Omega_{n,\nu}^{(\ell)}$ in the hierarchical approximation (10) are available for a given bit pattern, the transient switching waveforms $\boldsymbol{j}(t)$ of the driver model (2) are completely determined. The driver model is then completed with the static conductance $\boldsymbol{G}$ and DC biasing terms $\boldsymbol{I}_\nu$, as discussed in Sec. III.

We can now use this model to establish a fast transient simulation framework for a complete high-speed link, including a complete channel description together with the analog input impedance of the receiver (also assumed to behave as a LTI system) and its Continuous-Time Linear Equalization (CTLE) block, if present. As Fig. 7 shows, the entire system from driver up to the analog receiver part is a LTI system subject to a transient input $\boldsymbol{j}(t)$. Let us then consider the desired output (voltage) waveforms $\eta_m(t) = v_m(t) - v_m(0)$, where also in this case a DC shift by the initial operating point has been applied to setup a transient simulation with zero initial conditions. Due to linearity, the transfer function $H_{mn}(j\omega)$ between the n-th input component $j_n(t)$ and the m-th output component $\eta_m(t)$ can be determined by a standard frequency-domain analysis, by suitably cascading all frequency-dependent characterizations of the various blocks. This setup is the same as in standard AMI tools.

We now exploit the linear superposition in (10). Although this model is obtained as an adaptive nonlinear approximation, the latter is predetermined and statically computed once the bit pattern to be simulated is known. Therefore, we can consider (10) as a superposition of known elementary transient waveforms, one for each of the $2(L + 1)$ basis functions. A standard Fast Fourier Transform (FFT) processing is then applied to evaluate the response at the output due to a single individual basis function, which is expressed as

$$\psi_{mn,\nu}^{(\ell)}(t) = \mathcal{F}^{-1}\left\{H_{mn}(j\omega) \cdot \mathcal{F}\left\{\varphi_{n,\nu}^{(\ell)}(t)\right\}\right\} \qquad (14)$$

where $\mathcal{F}$ is the discrete Fourier operator (see Fig. 8). Thanks to superposition, the received voltages are then expressed as

$$\eta_{mn}(t) = \sum_{\ell=0}^{L}\Big[\sum_{k\in\Omega_{n,u}^{(\ell)}} \psi_{mn,u}^{(\ell)}(t - kT_B) + \sum_{k\in\Omega_{n,d}^{(\ell)}} \psi_{mn,d}^{(\ell)}(t - kT_B)\Big] \qquad (15)$$

Note that this expression is identical to (10) but uses different (known and predetermined) basis functions. In particular, it inherits sparsity due to the hierarchical multilevel expansion. The index sets $\Omega_{n,\nu}^{(\ell)}$ are unchanged.

The constructive approximation at the receiver is illustrated in Fig. 9. The top panel shows the received voltages at the end of a coupled lossy channel driven by the driver of Fig. 5 with FFE enabled. The different curves demonstrate the increasing approximation quality as the number of levels is augmented. When only level $\ell = 0$ is included, only single and isolated switching events are correctly represented. Including also level $\ell = 1$ provides an accurate representation of any pair of bits that are consecutively switching. Adding more levels leads to convergence for all possible switching sequences.

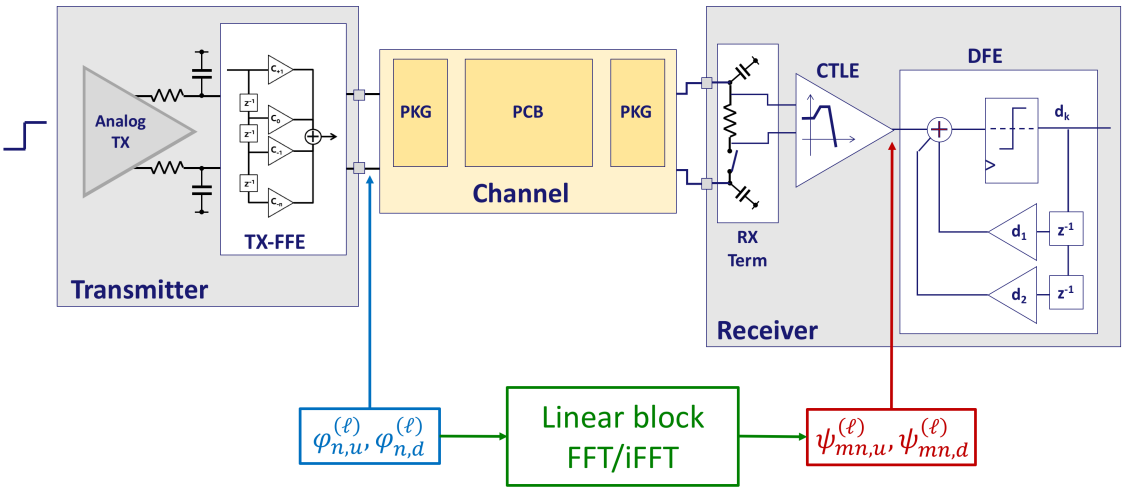

Fig. 7. Channel response computation.

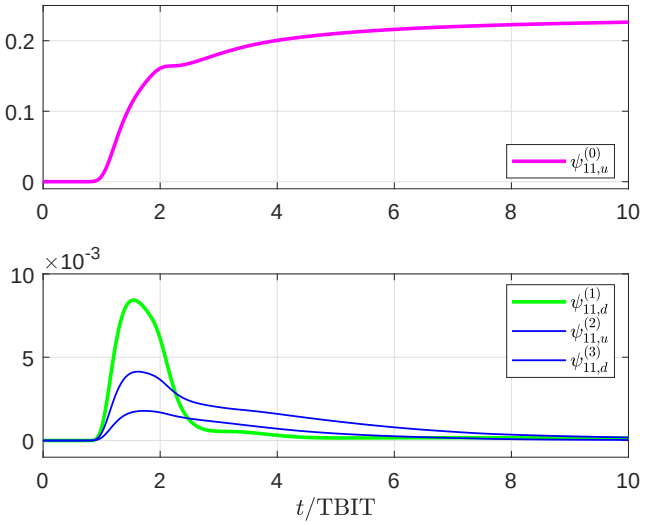

Fig. 8. Subset of individual basis functions $\psi^{(\ell)}_{mn,u}(t)$ and $\psi^{(\ell)}_{mn,d}(t)$, for $m = n = 1$ and $\ell = \{0, 1, 2, 3\}$ reproducing the received signal at the far end of the channel, obtained by FFT/IFFT processing of the corresponding basis functions $\varphi^{(\ell)}_{n,u}(t)$ and $\varphi^{(\ell)}_{n,d}(t)$ depicted in Fig. 6.

We conclude this Section with a few remarks. First, the proposed constructive approximation is able to estimate also common-mode signals in coupled channels, an example will be provided in next section. Second, nothing prevents application to multiconductor channels with more than two coupled signals, as far as adequate coupled models are available for all system parts. Finally, since the proposed constructive approximation aims at releasing the translation-invariance of the algorithmic TX-FFE part typical of the IBIS-AMI framework, it is expected that with minimal (and possibly no) modifications, the same approach can approximate well the responses of drivers operating in overclocking conditions, where similar effects due to single bit pulse responses extending beyond bit time are observed. A detailed analysis of this scenario is left to a future report.

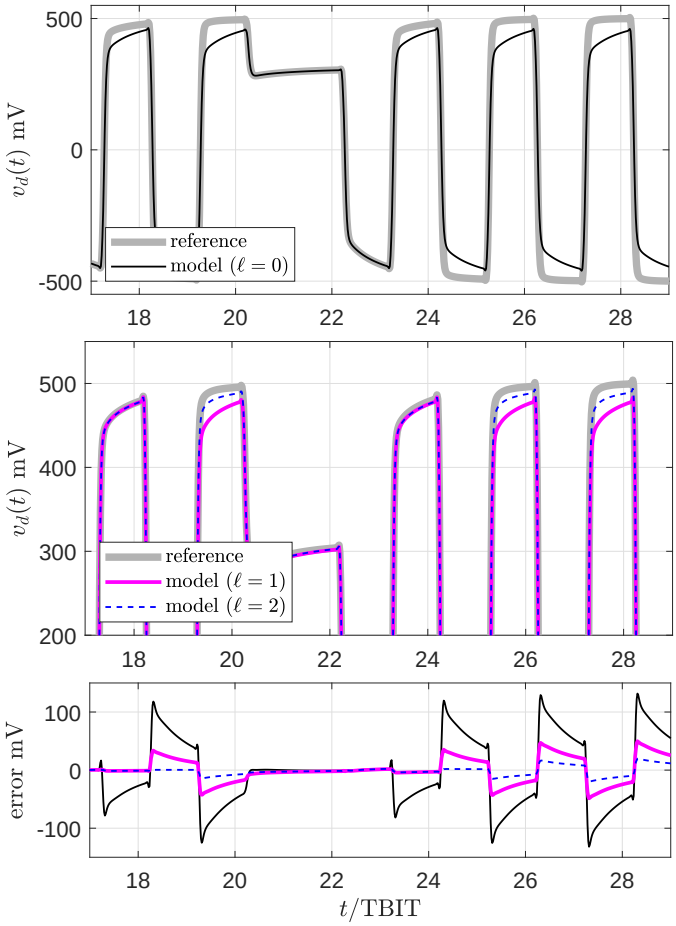

Fig. 9. Received voltages computed through superposition of increasing hierarchical levels (top) and error (bottom).

VI. Results

All numerical results presented in this section were obtained using a Workstation equipped with an Intel Core i9-7900X CPU @ 3.30 GHz and 32 GB RAM. For the same example driver considered in the previous sections (henceforth testcase #1) transmitting at a data rate of 3.125 Gbps and a real channel, Figure 10 compares the received differential and common-mode voltages computed using the true TL driver model with the results predicted by the proposed approach and the standard IBIS-AMI model. The responses predicted by the proposed linear model in (2) are obtained by post-processing the received waveforms (15), which are conveniently converted into the corresponding transient responses. This comparison highlights the superior accuracy introduced by the proposed approach. The bottom panel of Fig. 10 lacks the prediction for the common-mode voltage from the IBIS-AMI simulation, since this waveform is not supported by the current IBIS-AMI model structure. The common-mode voltage prediction of proposed approach is instead fairly accurate, with an approximation error that is likely due to the residual nonlinearity of the driver, which is here approximated as a pure LTI system.

Figure 11 shows the eye diagram (including jitter and crosstalk) obtained for a PRBS-31 pattern of one million bits (this bit stream was selected just to avoid any periodic repetition in the bit pattern). Thanks to linearity, common approaches for inclusion of deterministic and random jitter, as well as crosstalk, can be used in a post-processing phase, as in standard IBIS-AMI flows. Our prototypal non-optimized MATLAB implementation provided this result in 24 seconds. This performance should be compared to a state-of-the-art IBIS-AMI solver, when applied to the same testcase. The IBIS-AMI was simulated on the same hardware used to run the proposed model. The cumulative runtime was 1.7 seconds for the statistical simulation (which is not comparable in scope with our full transient simulation). Conversely, the bit-by-bit simulation (one million bits) with the IBIS-AMI solver required 49 seconds. These times include parsing and all pre-processing steps by the adopted commercial solver. Therefore, we see that the full transient simulation based on the proposed approach is even faster than a high-end commercial software, with the additional advantages of common mode estimation and accurate prediction of non-ideal TX-FFE effects.

In terms of accuracy, both the IBIS-AMI model and the proposed hierarchical solver are seen to underestimate Eye Width (EW) and Height (EH) with respect to the TL results. However, the relative errors of proposed method (10% and 17%, respectively on EW and EH) are significantly smaller than what is achieved by IBIS-AMI (30% and 42%). We remark that these errors are exceedingly large for allowing reliable use of such models in channel qualification, and should be regarded as a worst-case scenario due to the particularly strong non-ideal TX-FFE behavior of this particular TL device. The above results are thus a clear indication that any model should be used only within its limits of applicability.

As a second validation, Fig. 12 and Fig. 13 collect similar comparisons for a more recent commercial 40-nm low-power driver [21] transmitting at a data rate of 2.5 Gbps, denoted as

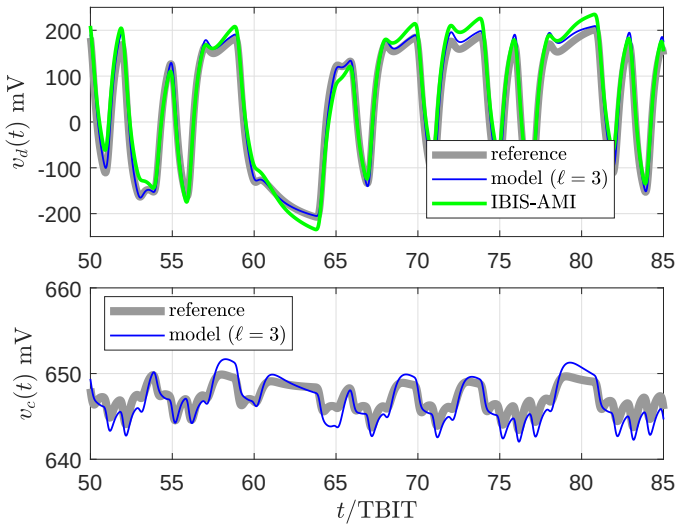

Fig. 10. Test case #1. Received differential (top) and common-mode (bottom) voltages, computed by different models.

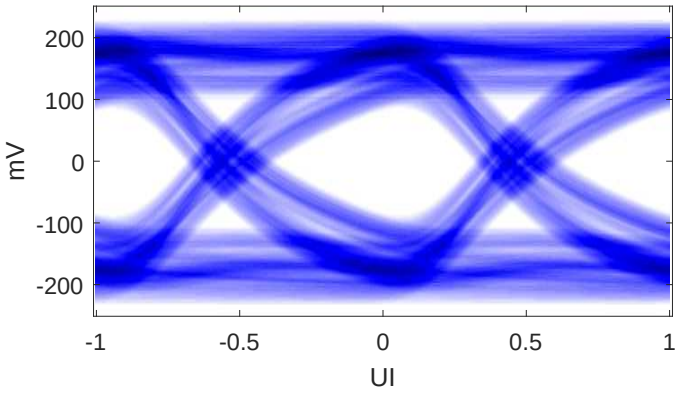

Fig. 11. Test case #1. Eye pattern obtained by processing a 10^6 bit stream.

testcase #2. Both figures report a comparison of the proposed approach with a reference TL simulation and with a prediction achieved by a nonlinear Mpilog macromodel [6]. This second test further confirms the excellent accuracy of the proposed approach in reproducing the rich dynamical behavior of the device. Concerning the simulation times, the TL simulation takes 1146 seconds to simulate 4500 bits, the Mpilog model takes 739 seconds, whereas the same simulation based on the proposed hierarchical linear model requires less than 1 second. For this driver, the eye pattern shown in Fig. 13 exhibits a wider opening and reduced dynamical effects with respect to the one obtained for the previous and older device (see Fig. 11). Similar to the previous testcase, the CPU-time required for the eye diagram construction with one million bits is about 27 seconds with proposed method, and about 50 seconds with the IBIS-AMI bit-by-bit solver. In terms of accuracy, the proposed solver allows estimating the EW and EH with a relative error of 6% and 8%, respectively, which is comparable to the accuracy achieved by the IBIS-AMI model (i.e., 5% and 9%) and it is exactly the same of the one provided by the Mpilog model (i.e., 6% and 8%). Thus, we see that all models are nearly equivalent in the estimation

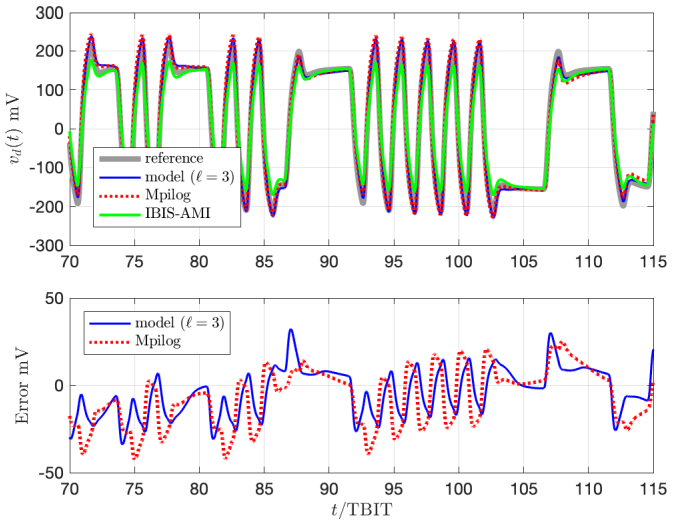

Fig. 12. Test case #2. Received differential voltages (top), computed by a reference transistor-level model, the proposed hierarchical simulator, an Mpilog [6] model and by IBIS-AMI. Bottom panel reports the transient error waveforms of the two macromodel-based simulations with respect to the TL reference signals.

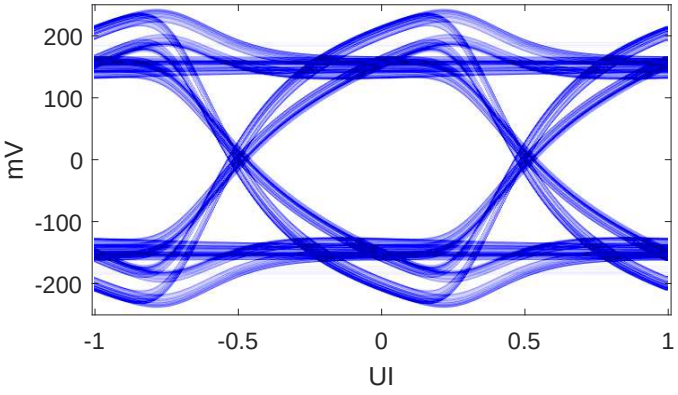

Fig. 13. Test case #2. Eye pattern obtained by processing a 10^6 bit stream.

of eye diagram metrics, although Fig. 12 clearly illustrates that, for the displayed bit sequence, the IBIS-AMI waveforms appear less accurate than those obtained by Mpilog and by proposed hierarchical solver.

Summarizing, the proposed hierarchical linear model structure performs in all cases with a similar accuracy as the fully nonlinear Mpilog model but requiring simulation times that are comparable to the IBIS-AMI framework, albeit with some small overhead due to the implementation of the constructive hierarchical superposition.

VII. Conclusions

This paper presented an improved modeling and simulation methodology for the fast simulation of high-speed transmission over differential channels. On one hand, the state-of-the-art and de facto industrial standard IBIS-AMI is extended by proposing a compact linear macromodel of a differential driver which embeds the TX-FFE mechanism via an ad hoc hierarchical-based expansion of its source terms. The proposed model allows the accurate modeling of both the differential and common mode device responses and a tunable accuracy which depends on the number of basis functions accounted for. On the other hand, channel simulation is done in a mixed time and frequency domain, yielding reduced simulation times and allowing to compute eye patterns for millions of bits in few seconds. This is accomplished net of any code optimization, using a simple prototypal MATLAB implementation.

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