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A Dynamic Greedy Test Scheduler for Optimizing Probe Motion in In-Circuit Testers

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***Abstract*—The test of a printed-circuit board assembly often includes in-circuit test, which mainly aims at checking whether the different components have been correctly soldered. A tester may adopt either the bed of nails, or the flying probes architecture. In the latter case, probes move to contact test points on each side of the board to perform the required tests. In order to minimize the test time, the sequence of movements of the probes should be optimized, taking into account the tester capabilities, the board layout, and the several constraints coming from the environment and the customer. In this paper we describe the approach developed for optimizing tests on the SPEA 4080, which exploits the new hardware available to combine reduced test time with short test-generation time. Experimental results show the effectiveness of the proposed solution.**

I. INTRODUCTION AND PROPOSED APPROACH

Manufacturing Printed Circuit Boards (PCBs) is a complex process which requires extensive testing to guarantee acceptable levels of quality. Several test phases are typically implemented, often starting already at intermediate steps during the manufacturing process.

In this scenario a key role is played by In-Circuit Test (ICT), which checks the electrical properties of the target connections by applying/reading voltages and currents. ICT is implemented by resorting to probes which contact specific points on the boards (*test points*) and perform the required tests. With the emergence of new kinds of device packages (e.g., BGA), some points on the boards could not be accessed any more, and ICT can be complemented by Boundary Scan (BS). However, ICT continues to play a major role in PCBA testing, due to the huge number of connections which can be accessed by the probes and are not controllable/observable via BS (e.g., because they are related to passive or non BS components). ICT equipment are divided in two groups: *Bed-of-nails* and *Flying-probes.*

In the last years, flying-probes testers improved significantly, increasing the number of probes, the speed and precision of their movements, while reducing their size, thus allowing to exactly contact very small test points. This trend allowed to reduce the comparative benefits of bed-of-nails, and made flying-probes testers interesting even for mass production of complex PCBAs. The mechanics and the architecture of Flying Probes tester is continuously improved: for example, the SPEA 4080 tester [1] is equipped with 8 probes moving on the two sides of the board under test at unprecedented speed (up to 160 touches per second), and able to contact extremely small pads (down to 50μm). This new generation of In-Circuit Testers may allow to widely extend the range of application of the flying-probe testers to PCBA mass-production.

Clearly, the duration of the whole test can be minimized not only by increasing the number of probes working in parallel and the speed of their movements, but also minimizing the list of tests to be performed to achieve the target quality [2]. Moreover, the sequence according to which tests are performed significantly affects the total duration of the ICT process, since it allows minimizing the number of movements of the probes and their duration. Some early works on this problem were reported in [3]. However, such a kind of solutions does not scale with the size and complexity of current products, which easily include hundreds of components and tens of thousands of test points. Also traditional branch-and-bound algorithms can hardly be exploited, since they might not be able to scale with the size of the faced problem. Moreover, the optimization of the probe movements requires taking into account not only the minimization of the path to be followed, but also a number of other constraints, such as those coming from the fact that multiple probes may be on the fly at a given time and any contact between them must be avoided, or those related to the pressure they create on the two sides of the board, or due to the presence of special components over which the probes cannot fly (*no-fly zones*).

This work outlines the techniques developed for optimizing the flying probes movements in the new SPEA 4080 test equipment. We propose an optimization algorithm based on a dynamic greedy procedure that selects the optimal sequence of tests. In each step, the set of tests that will be performed in the subsequent measure is incrementally built by adding the one that would introduce the smallest delay given the current position of the probes. However, all the alternative probe positionings compatible with the tests to be performed are considered concurrently, as a set of possible implementations of the selected tests. The size of such a set increases in the beginning of the search process and slowly shrinks down to a single element as adding new tests increases the constraints, reducing the degree of freedom.

The greedy algorithm guarantees a linear number of steps on the number of required tests, while considering a set of alternatives in concurrently enhances the explorations and helps avoiding local minima. Moreover, the complexity of each step is bounded by a

user parameter and does not depend on the size of the problem.

Concerning the complexity of the algorithm, the number of steps of the optimization process increases linearly with the number of tests. Anyhow, during the optimization, all tests need to be selected; for each of them, the weight of all the remaining ones must be recalculated, and the heuristic adopted needs to scan all test points on the board. Let n_t be the number of tests and n_p be the number of test points, the theoretical complexity of the procedure may therefore be approximated as $\mathcal{O}(n_t^2 n_p)$. When large boards are considered, the heuristic procedure only considers a subset of the test points.

II. EXPERIMENTAL RESULTS

The algorithm was implemented in about 5,000 lines in C++. For the sake of comparison, we also report the performances of FP2012, the algorithm previously used on SPEA ATEs.

It should be noted, however, that FP2012 was designed and optimized for the type of boards tested on the machines of the previous generation, and its performances are sub-optimal when the number of tests and test points is high. Moreover, the older algorithm did not target the hardware available on the SPEA 4080.

TABLE I. BOARD CHARACTERISTICS

Board	Physical		Test plan
	Size [cm]	Test points	Tests
Board 1	25.59 x 18.30	134	1,252
Board 2	24.89 x 23.63	143	591
Board 3	11.95 x 13.53	167	855
Board 4	19.14 x 16.11	360	2,003
Board 5	14.51 x 13.94	528	2,791
Board 6	28.44 x 15.28	680	5,931
Board 7	27.46 x 25.41	704	1,915
Board 8	20.67 x 11.00	950	64,428
Board 9	31.33 x 27.86	996	4,022
Board 10	35.36 x 23.79	1,849	17,820
Board 11	12.24 x 13.07	2,267	12,317
Board 12	49.18 x 46.47	11,950	48,759

Results are reported in Table II on a dozen of boards where the SPEA 4080 is used, with different characteristics in terms of test points and tests, and different dimensions (see Table I). Some boards are internal testbenches, while other correspond to real products. The comparison takes into account both the computational time required to optimize the test plan (Opt) and the time required to execute it (Exe).

FP2018 is more efficient optimizing the test plan, with an average increment in performance of 80%, and a peak of 98% on Board 11, where an optimization time of 11 minutes is reduced to a mere 13 seconds. It is important to underline that the optimization time remains within a reasonable range of values (i.e., minutes) even for the largest and most complex boards.

TABLE II. TIME REQUIRED FOR THE OPTIMIZATION AND THE EXECUTION OF THE TEST PLAN

Board	FP2012		FP2018	
	Opt [s]	Exe [s]	Opt [s]	Exe [s]
Board 1	12	12	1	10
Board 2	9	2.5	1	2
Board 3	52	23	3	8
Board 4	119	29	6	27
Board 5	61	45	13	28
Board 6	70	58	16	29
Board 7	55	32	28	24
Board 8	1,890	1,348	308	1,056
Board 9	72	42	20	36
Board 10	1,167	168	194	133
Board 11	660	244	13	88
Board 12	510	819	320	489

The test plans optimized by the new algorithm are also more effective, and require less time to be executed. Improvements range from a 7% on Board 4 (from 29 seconds to 27), to a 65% on Board 3 (from 23 second to 8), with an average reduction of 32%. The performance of the proposed algorithm does not seem to degrade with either the number of test points or tests.

III. CONCLUSIONS

Experimental results gathered on a set of different boards show that the proposed solution is able to take full advantage of the new architecture of the SPEA 4080 system. The computational time required to optimize the test plan remains within an acceptable range of values, while the execution time is significantly reduced, thus widening the set of scenarios where flying-probes ICTs can be effectively adopted.

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