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A 0.6 V Current Reference Based on the MOSFET Forward-Body-Biased ZTC Condition

Luis Henrique Rodovalho*, Pedro Toledo†‡
*Integrated Circuits Laboratory, Federal University of Santa Catarina, Brazil
†Graduate Program on Microelectronics - UFRGS - Porto Alegre, RS, Brazil
‡Politecnico di Torino - Polito - Turin, Italy
{luis.henrique.rodovalho@posgrad.ufsc.br, pedro.leitecorreia@polito.it}

Abstract—This work presents a self biased current reference circuit based on the MOSFET Zero Temperature Coefficient (ZTC) condition. To achieve lower supply voltage ($V_{DD}$) operation, the proposed circuit employs forward body biasing technique to decrease the MOSFET ZTC biasing point. In addition, a body-driven pseudo differential Operational Transconductance Amplifier (OTA) is used to further reduce the minimum supply voltage. From transistor-level simulations, the current reference is predicted to have an Effective Temperature Coefficient ($TC_{EB}$) of 65 ppm/°C from -55 to 125 °C and a fabrication sensitivity of $\sigma/\mu = 6.5\%$, including process and mismatch variability. The power supply sensitivity is around 0.75 %/V for this new reference.

I. INTRODUCTION

Being an essential building block for analog designs, current references work as a biasing reference for many other circuits. To suit the recent nanoscale CMOS technology low voltage supply ($V_{DD}$) constraints [1] and/or the requirements of low power applications [2]–[4], several current references have been proposed [5]–[8]. Among them, it can readily be seen that the usage of the MOSFET Zero Temperature Coefficient (ZTC) condition has been showing itself as a good approach mainly due to its programmability [9]–[12] and its availability in advanced MOSFETs technologies, such as UTBB SOI and FinFET devices [13].

As a new alternative, this work presents a novel ZTC based current reference circuit which uses forward body biasing technique to decrease the MOSFET ZTC bias point. In addition, to further improve the circuit performance in low $V_{DD}$ operation, a bulk-driven pseudo differential Operational Transconductance Amplifier (OTA) [14], [15] within proposed current reference is used.

The paper has the following structure. In Section II, the forward body biasing technique applied in the ZTC operating point is described. In Section III, the self-biased CMOS current reference is analysed and designed. The transistor level simulation results are presented in Section IV, followed by comparisons to other references proposed in the literature. Finally, in section V, the concluding remarks are drawn.

II. MOSFET FORWARD-BODY-BIASED ZTC CONDITION

The ZTC condition comes from the mutual cancellation of the mobility and threshold voltage dependencies on temperature [5]. Fig. 1 shows the drain current w.r.t. the gate-source voltage ($V_{GS}$) of a saturated long-channel 10 $\mu$m width by 10 $\mu$m length 180nm process NMOS transistor, simulated under $-40^\circ$C, $27^\circ$C and $85^\circ$C temperatures, for both the gate and forward-body-biased diode-connected configurations. The ZTC operation points can be seen around $V_{GB} \approx 570\text{mV}$ and $V_{GB} \approx 450\text{mV}$ for the gate and forward-body-biased diode-connected configurations, respectively. In these bias points, the currents are tolerant to temperature variation.

In [5], MOSFET ZTC and its vicinity conditions have been modeled and expressed by (1) and (2). Which explain the lower voltages for the ZTC behavior in the the forward-body-biased configuration (negative $V_{SB}$).

\[ V_{GS}(T) \approx V_{GZ} - \frac{\alpha_{V_T} \Delta i_f T}{2i_f z} \]  
(1)

where

\[ V_{GZ} = V_{T0}(T_0) + (n - 1)V_{SB} - \alpha_{V_T0} T_0 \]  
(2)

$V_{GS}$ is the gate-source voltage, $V_{GZ}$ is the ZTC gate-source voltage, $\beta_z$ is the ZTC slope, $\Delta i_f$ indicates how far the transistor is biased from the ZTC operating point, $i_f$ is the forward inversion level, $i_{fb}$ is the ZTC forward inversion level, $T$ is the temperature, $V_{T0}(T_0)$ is the threshold voltage at room temperature, $n$ is the slope factor, $V_{SB}$ is the source-bulk voltage and $\alpha_{V_{T0}}$ is the thermal coefficient of the threshold voltage.
III. PROPOSED SELF BIASED CURRENT REFERENCE

Figure 2 shows a self-biased current reference based on the MOSFET ZTC operation condition, as presented in [5]. The MOSFET device $M_{ZTC}$, while in diode configuration (in this case, forward-body-biased connected), if biased properly with a specific $V_{GS}$ gate-source voltage, outputs a drain current tolerant to temperature variations. The main idea of this current reference topology is to use ZTC vicinity of a MOSFET transistor to compensate the thermal drift of a polysilicon reference resistor $R_{REF}$, resulting on an equilibrium bias point with small temperature dependence. The Eqs. (3) and (4) describe how to size $R_{REF}$ and $M_{ZTC}$ aspect ratio properly [5].

$$R_{REF} \approx \frac{V_{GZ}}{I_{REF}(1 - \alpha_1 T_0)}$$

$$= \frac{V_{T0}(T_0) + (n - 1)V_{SB} - \alpha V_{TP} T_0}{I_{REF}(1 - \alpha_1 T_0)}$$

(3)

$$\frac{(W/L)_{ZTC}}{\mu_n(T_0)T_0^2C^\prime_{ox}} = \frac{2n}{T_{REF}} \left( \frac{-2\alpha_{SB}}{\alpha V_{TP}} + 1 \right) - 1$$

(4)

where $\alpha_1$ is poly resistor thermal dependence, $C^\prime_{ox}$ is the gate capacitance per unit of area and $I_{REF}$ is the output reference current.

The minimum supply voltage required by this topology is limited either by the $M_{ZTC}$ biasing voltage or by the OTA. Figure 3a shows a version of the previous circuit using conventional OTA. This OTA is composed of three stacked transistors which must be in the saturation region in order the circuit functions properly.

The circuit shown in Figure 3b uses a body input OTA, which is composed by two stacked transistors and can possibly function with a lower supply voltage. However, the use of the body terminal as input has its drawbacks. The forward biased body-source junction works as a forward biased diode and draws current from the input source. More importantly, the input impedance varies greatly with temperature, which can interfere in the reference transistor $M_{ZTC}$ biasing point. As the reference transistor $M_{ZTC}$ gate and body terminals are shorted in order to lower its ZTC biasing point, $V_D$ is then lowered and the current drawn by the differential pair parasitic diode is decreased, as can be seen in Fig. 1. The same technique is used in the current mirror composed of the transistors $M_{1A-D}$ to decrease their inversion levels and, consequently, their saturation voltages.

Also, the body-drain small signal transconductance $g_{mb}$ is a fraction of the gate-drain transconductance $g_{mg}$ so that the OTA has a reduced voltage gain compared to the conventional gate input OTAs. To mitigate this, the transistors $M_{1A-D}$ and $M_{2A-B}$ are replaced by composite transistors [16], which can
be made equivalent to single transistors with larger output impedance.

IV. SIMULATION RESULTS

To validate the proposed current reference, three versions have been designed using the same forward-biased ZTC transistor and polyresistor with the Silterra IoT 0.18 $\mu$m PDK. All simulation results herein presented are at transistor level using Cadence Virtuoso™ software and BSIM4.5 MOSFET models.

The three versions differ only by the OTA, as shown in Figure 3, and the transistor sizes are shown in Table I.

<table>
<thead>
<tr>
<th></th>
<th>$k \times m \times W/L$</th>
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<tbody>
<tr>
<td>$M_{A,F}$</td>
<td>16 x 4 x 700 nm / 360 nm</td>
</tr>
<tr>
<td>$M_{A,B}$</td>
<td>16 x 4 x 700 nm / 360 nm</td>
</tr>
<tr>
<td>$M_{A,D}$</td>
<td>16 x 4 x 700 nm / 360 nm</td>
</tr>
<tr>
<td>$M_{A,B}$</td>
<td>16 x 1 x 700 nm / 2.82 $\mu$m</td>
</tr>
<tr>
<td>$M_{B}$</td>
<td>16 x 1 x 700 nm / 2.82 $\mu$m</td>
</tr>
<tr>
<td>$M_{C}$</td>
<td>16 x 1 x 700 nm / 2.82 $\mu$m</td>
</tr>
<tr>
<td>$M_{ZTC}$</td>
<td>1 x 1 x 10.0 $\mu$m / 10.0 $\mu$m</td>
</tr>
<tr>
<td>$R_{REF}$</td>
<td>24 x 450 $\mu$m / 7.75 $\mu$m</td>
</tr>
<tr>
<td>$C_M$</td>
<td>1 x 20 $\mu$m / 50 $\mu$m</td>
</tr>
</tbody>
</table>

**TABLE I: Transistor dimensions**

Figure 4 shows how each circuit version compares to each other in several performance aspects. Figure 4a shows the reference current $I_{REF}$ versus power supply. All circuits were designed at the same biasing point and output a 690 nA reference current, but they differ at the power supply sensitivity and minimum operational supply voltage. The gate input OTA, body input OTA and enhanced body input OTA versions have a minimum operational voltage of approximately 0.7 V, 0.6 V and 0.6 V, and 0.02 %/V, 3.00 %/V and 0.75 %/V supply voltage sensitivity respectively.

Figure 4b depicts $I_{REF}$ temperature sensitivity. The gate input OTA has Effective Temperature Coefficient ($T_{C_{eff}}$) of approximately 80 ppm/°C, over a temperature range from -40 to 85°C. On the other hand, the body input OTA versions have a $T_{C_{eff}}$ of approximately 65 ppm/°C over the temperature range from -55 to 125°C. It is worthwhile to mention that the body input versions were optimized for temperature range and the same biasing point was used for the gate bias version so that they would output the same reference at typical conditions.

Figure 4c depicts $I_{REF}$ power supply rejection ratio of each circuit version at a 700 mV supply voltage operation. As can be noticed, the enhanced body input OTA version exhibits a better DC PSRR than simple bulk input OTA version, but they exhibit almost the same behavior at higher frequencies. The gate OTA version has a similar DC PSRR at this supply voltage operation point, yet it has a better performance at higher frequencies, due to transistor gate-drain transconductances being considerably higher than body transconductances.

**Fig. 5: Monte Carlo simulation including process and mismatch**

Figure 4d shows a transient simulation depicting the start-up time and circuit stability with a 1 $\mu$s rise time 700 mV supply voltage pulse signal. All circuits use a compensation capacitor $C_M$ to ensure stability, but only the OTA version needs a start-up circuit, as shown in Figure 2.

Figure 5 shows the enhanced body input current reference version $I_{REF}$ and $T_{C_{eff}}$ spread from 1000 monte carlo runs, including process variation and mismatch. Fig. 5a shows the reference current spread with a $\sigma/\mu = 6.5\%$. While Fig. 5b presents a $T_{C_{eff}}$ spread with 99 % of samples below the 300 ppm/°C. In order to correct the process variability undesired effects, a calibration scheme, such as digitally trimmed reference resistors [18] could be used.

Table II presents a summary of our topologies and com-
Table II: Comparison of CMOS current references

<table>
<thead>
<tr>
<th></th>
<th>This Work**</th>
<th>[5]**</th>
<th>[6]*</th>
<th>[7]**</th>
<th>[17]*</th>
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<tr>
<td></td>
<td>(a)</td>
<td>(b)</td>
<td>(c)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
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<tr>
<td>Temperature range (°C)</td>
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<td>-55 to 125</td>
<td>-55 to 125</td>
<td>-40 to 85</td>
<td>-70 to 100</td>
</tr>
<tr>
<td>Minimum Power Supply (V)</td>
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<td>0.6</td>
<td>0.6</td>
<td>1.4</td>
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<tr>
<td>$I_{REF} (\mu A)$</td>
<td>0.690</td>
<td>0.690</td>
<td>0.690</td>
<td>5.0</td>
<td>0.042</td>
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<tr>
<td>Total current (\muA)</td>
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<td>2.76</td>
<td>196</td>
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<td>Power (\muW)</td>
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<td>1.65</td>
<td>1.65</td>
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<td>-</td>
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<tr>
<td>Power Supply Sensitivity (%/V)</td>
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<td>3.00</td>
<td>0.75</td>
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<td>2.5</td>
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<td>Temperature coefficient (ppm/°C)</td>
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<td>65</td>
<td>65</td>
<td>15</td>
<td>3000</td>
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<tr>
<td>PSRR (dB)</td>
<td>45.8</td>
<td>36.8</td>
<td>48.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Start-Up Time (\mu s)</td>
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<td>2.0</td>
<td>3.0</td>
<td>0.008</td>
<td>0.010</td>
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<tr>
<td>Area mm²</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.010</td>
<td>0.025</td>
</tr>
</tbody>
</table>

* Measured results ** Simulated results

Fig. 6: Enhanced Bulk Driven OTA version self biased current reference layout

Comparison of published current references in similar process technologies. The main advantage of the proposed solution is its low supply voltage requirement.

V. CONCLUSION

Forward body biasing lowers the MOSFET ZTC condition and this technique can be used to decrease the minimum supply voltage, as it has been demonstrated in the proposed self-biased current reference. A body input OTA has also been used to further reduce the minimum supply voltage and composite transistors were implemented to improve the OTA voltage gain. Transistor-level simulation results have shown $T_C_{eff}$ of 65 ppm/°C from -55 to 125 °C and a fabrication sensitivity of $\sigma/\mu = 6.5 \%$, with 0.75 %/V of power supply sensitivity.

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REFERENCES