A 0.6 V Current Reference Based on the MOSFET Forward-Body-Biased ZTC Condition

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***Abstract*—This work presents a self biased current reference circuit based on the MOSFET Zero Temperature Coefficient (ZTC) condition. To achieve lower supply voltage ($V_{\rm DD}$) operation, the proposed circuit employs forward body biasing technique to decrease the MOSFET ZTC biasing point. In addition, a body-driven pseudo differential Operational Transconductance Amplifier (OTA) is used to further reduce the minimum supply voltage. From transitor-level simulations, the current reference is predicted to have an Effective Temperature Coefficient ($TC_{\rm eff}$) of 65 ppm/^{o}C from -55 to 125 ^{o}C and a fabrication sensitivity of σ/μ = 6.5 $\%$, including process and mismatch variability. The power supply sensitivity is around 0.75 $\%/$V for this new reference.**

I. Introduction

Being an essential building block for analog designs, current references work as a biasing reference for many other circuits. To suit the recent nanoscale CMOS technology low voltage supply ($V_{\rm DD}$) constraints [1] and/or the requirements of low power applications [2]–[4], several current references have been proposed [5]–[8]. Among them, it can readily be seen that the usage of the MOSFET Zero Temperature Coefficient (ZTC) condition has been showing itself as good approach mainly due to its programability [9]–[12] and its availability in advanced MOSFETs technologies, such as UTBB SOI and FinFET devices [13].

As a new alternative, this work presents a novel ZTC based current reference circuit which uses forward body biasing technique to decrease the MOSFET ZTC bias point. In addition, to further improve the circuit performance in low $V_{\rm DD}$ operation, a bulk-driven Operational Transconductance Amplifier (OTA) [14], [15] within proposed current reference is used.

The paper has the following structure. In Section II, the forward body biasing technique applied in the ZTC operating point is described. In Section III, the self-biased CMOS current reference is analysed and designed. The transistor level simulation results are presented in section IV, followed by comparisons to other references proposed in the literature. Finally, in section V, the concluding remarks are drawn.

II. MOSFET Forward-Body-Biased ZTC Condition

The ZTC condition comes from the mutual cancellation of the mobility and threshold voltage dependencies on temperature [5]. Fig. 1 shows the drain current w.r.t. the gate-source voltage (V_{GS}) of a saturated long-channel 10 μm width by 10 μm length 180nm process NMOS transistor, simulated

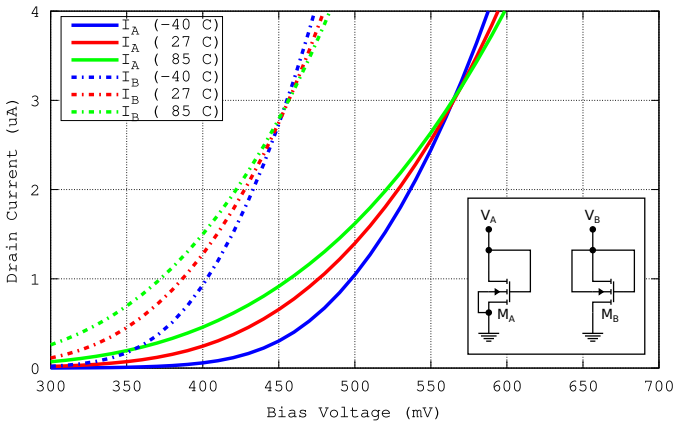


Fig. 1: NMOSFET ZTC condition in diode configuration: (a) Gate connected and (b) Forward-Body-Biased connected

under -40^oC, 27^oC and 85^oC temperatures, for both the gate and forward-body-biased diode-connected configurations. The ZTC operation points can be seen around $V_{GB} \approx 570$mV and $V_{GB} \approx 450$mV for the gate and forward-body-biased diode-connected configurations, respectively. In these bias points, the currents are tolerant to temperature variation.

In [5], MOSFET ZTC and its vicinity conditions have been modeled and expressed by (1) and (2). Which explain the lower voltages for the ZTC behavior in the the forward-body-biased configuration (negative $V_{\rm SB}$).

$$V_{GS}(T) \approx V_{GZ} - \frac{\alpha_{V_{T0}} \Delta i_f}{2 i_{fz}} T \tag{1}$$

where

$$V_{GZ} = V_{T0}(T_0) + (n-1)V_{SB} - \alpha_{V_{T0}} T_0 \tag{2}$$

$V_{\rm GS}$ is the gate-source voltage, $V_{\rm GZ}$ is the ZTC gate-source voltage, β_z is the ZTC slope, $\Delta i_{\rm f}$ indicates how far the transistor is biased from the ZTC operating point, i_f is the forward inversion level, $i_{\rm fz}$ is the ZTC forward inversion level, T is the temperature, $V_{\rm T0}(T_0)$ is the threshold voltage at room temperature,n is the slope factor, $V_{\rm SB}$ is the source-bulk voltage and $\alpha_{\rm V_{T0}}$ is the thermal coefficient of the threshold voltage.

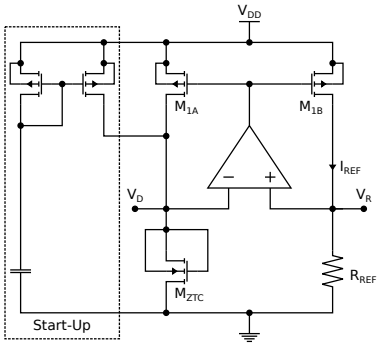


Fig. 2: Self-biased CMOS current reference concept based on the forward-body-biased ZTC operation condition [5].

III. Proposed Self Biased Current Reference

Figure 2 shows a self-biased current reference based on the MOSFET ZTC operation condition, as presented in [5]. The MOSFET device M_{ZTC}, while in diode configuration (in this case, forward-body-biased connected), if biased properly with a specific V_{GS} gate-source voltage, outputs a drain current tolerant to temperature variations. The main idea of this current reference topology is to use ZTC vicinity of a MOSFET transistor to compensate the thermal drift of a polysilicon reference resistor R_{REF}, resulting on an equilibrium bias point with small temperature dependence. The Eqs. (3) and (4) describe how to size R_{REF} and M_{ZTC} aspect ratio properly [5].

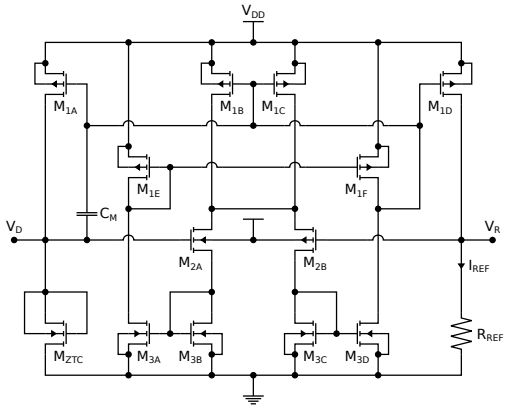
$$R_{REF} \approx \frac{V_{GZ}}{I_{REF}(1-\alpha_1 T_0)} = \frac{V_{T0}(T_0) + (n-1)V_{SB} - \alpha_{V_{T0}} T_0}{I_{REF}(1-\alpha_1 T_0)} \tag{3}$$

$$(W/L)_{ZTC} = \frac{2n\left(\frac{-2\alpha_1}{\alpha_{V_{T0}}} R_{REF} + \frac{1}{I_{REF}}\right)^{-1}}{\mu_n(T_0) T_0^2 C'_{ox} \alpha^2_{V_{T0}}} \tag{4}$$

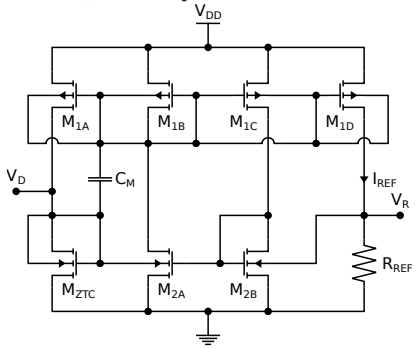
where α_1 is poly resistor thermal dependence, C'_{ox} is the gate capacitance per unit of area and I_{REF} is the output reference current.

The minimum supply voltage required by this topology is limited either by the M_{ZTC} biasing voltage or by the OTA. Figure 3a shows a version of the previous circuit using conventional OTA. This OTA is composed of three stacked transistors which must be in the saturation region in order the circuit functions properly.

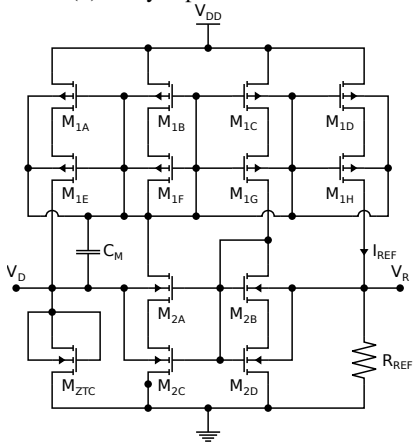
The circuit shown in Figure 3b uses a body input OTA, which is composed by two stacked transistors and can possibly function with a lower supply voltage. However, the use of the body terminal as input has its drawbacks. The forward biased body-source junction works as a forward biased diode and draws current from the input source. More importantly, the input impedance varies greatly with temperature, which can interfere in the reference transistor M_{ZTC} biasing point. As the reference transistor M_{ZTC} gate and body terminals



(a) Gate input OTA version



(b) Body input OTA version

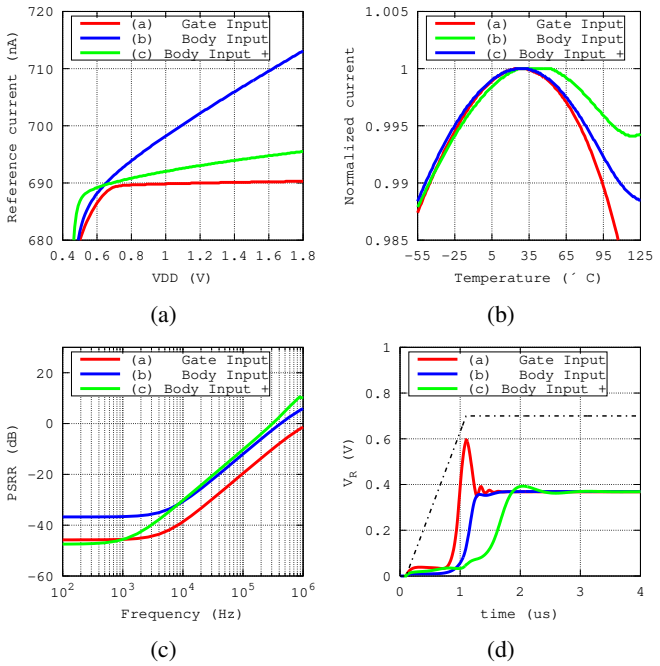


(c) Body input OTA enhanced version

Fig. 3: Current reference circuits with OTA variations

are shorted in order to lower its ZTC biasing point, V_D is then lowered and the current drawn by the differential pair parasitic diode is decreased, as can be seen in Fig. 1. The same technique is used in the current mirror composed of the transistors M_{1A-D} to decrease their inversion levels and, consequently, their saturation voltages.

Also, the body-drain small signal transconductance g_{mb} is a fraction of the gate-drain transconductance g_{mg} so that the OTA has a reduced voltage gain compared to the conventional gate input OTAs. To mitigate this, the transistors M_{1A-D} and M_{2A-B} are replaced by composite transistors [16], which can



(a) (b) (c) (d)

Fig. 4: Current reference comparison: (a) Output current reference power supply sensitivity, (b) Normalized current reference temperature sensitivity, (c) Power Supply Rejection and (d) Start-Up Time

be made equivalent to single transistors with larger output impedance.

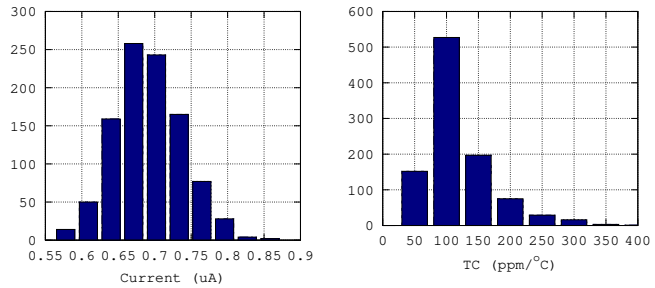
IV. Simulation Results

To validate the proposed current reference, three versions have been designed using the same forward-biased ZTC transistor and polyresistor with the Silterra IoT 0.18 μm PDK. All simulation results herein presented are at transistor level using Cadence Virtuoso ™software and BSim4.5 MOSFET models. The three versions differ only by the OTA, as shown in Figure 3, and the transistor sizes are shown in Table I.

	$k \times m \times W/L$
	Gate Input OTA
M_{1A-F}	16 × 4 × 700 nm / 360 nm
M_{2A-B}	16 × 4 × 700 nm / 360 nm
M_{3A-D}	16 × 4 × 700 nm / 360 nm
	Body Input OTA
M_{1A-D}	16 × 1 × 700 nm / 2.82μm
M_{1A-B}	16 × 1 × 700 nm / 2.82μm
	Enhanced Body Input OTA
M_{1A-D}	16 × 1 × 700 nm / 2.82μm
M_{1E-H}	16 × 4 × 700 nm / 360 nm
M_{1A-B}	16 × 4 × 700 nm / 360 nm
M_{1C-D}	16 × 1 × 700 nm / 2.82μm
M_{ZTC}	1 × 1 × 10.0μm / 10.0μm
R_{REF} (535 kΩ)	24 × 450 nm / 7.75 μm
C_M (1 pF)	1 × 20 μm / 50 μm

TABLE I: Transistor dimensions

Figure 4 shows how each circuit version compares to each other in several performance aspects. Figure 4a shows the



(a) (b)

Fig. 5: Monte Carlo simulation including process and mismatch: (a) Output current reference mismatch and (b) Temperature coefficient mismatch

reference current I_{REF} versus power supply. All circuits were designed at the same biasing point and output a 690 nA reference current, but they differ at the power supply sensitivity and minimum operational supply voltage. The gate input OTA, body input OTA and enhanced body input OTA versions have a minimum operational voltage of approximately 0.7 V, 0.6 V and 0.6 V, and 0.02 %/V, 3.00 %/V and 0.75 %/V supply voltage sensitivity respectively.

Figure 4b depicts I_{REF} temperature sensitivity. The gate input OTA has Effective Temperature Coefficient (TC_{eff}) of approximately 80 ppm/°C, over a temperature range from -40 to 85°C. On the other hand, the body input OTA versions have an TC_{eff} of approximately 65 ppm/°C over the temperature range from -55 to 125°C. It is worthwhile to mention that the body input versions were optimized for temperature range and the same biasing point was used for the gate bias version so that they would output the same reference at typical conditions.

Figure 4c depicts I_{REF} power supply rejection ratio of each circuit version at a 700 mV supply voltage operation. As can be noticed, the enhanced body input OTA version exhibits a better DC PSRR than simple bulk input OTA version, but they exhibit almost the same behavior at higher frequencies. The gate OTA version has a similar DC PSRR at this supply voltage operation point, yet it has a better performance at higher frequencies, due to transistor gate-drain transconctances being considerably higher than body transconductances.

Figure 4d shows a transient simulation depicting the start-up time and circuit stability with a 1 μs rise time 700 mV supply voltage pulse signal. All circuits use a compensation capacitor C_M to ensure stability, but only the OTA version needs a start-up circuit, as shown in Figure 2.

Figure 5 shows the enhanced body input current reference version I_{REF} and TC_{eff} spread from 1000 monte carlo runs, including process variation and mismatch. Fig. 5a shows the reference current spread with a $\sigma/\mu = 6.5\%$. While Fig. 5b presents a TC_{eff} spread with 99 % of samples below the 300 ppm/°C. In order to correct the process variability undesired effects, a calibration scheme, such as digitally trimmed reference resistors [18] could be used.

Table II presents a summary of our topologies and com-

	This Work**			[5]**	[6]*	[7]**	[17]*
	(a)	(b)	(c)				
Technology	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Temperature range (° C)	-55 to 100	-55 to 125	-55 to 125	-40 to 85	-70 to 100	-25 to 125	0 to 100
Minimum Power Supply (V)	0.7	0.6	0.6	1.4	1.0	0.65	1.0
I_{REF} (μA)	0.690	0.690	0.690	5.0	0.042	0.01	144
Total current (μA)	4.14	2.76	2.76	196	-	0.09	
Power (μW)	2.90	1.65	1.65	342	-	0.07	227
Power Supply Sensitivity (%/V)	0.02	3.00	0.75	2.5	0.2	0.01	
Temperature coefficient (ppm/° C)	80	65	65	15	3000	350	185
PSRR (dB)	45.8	36.8	48.5	-	-	-	-
Start-Up Time (μs)	2.0	2.0	3.0	-	-	5500	-
Area mm^2	-	-	0.008	0.010	0.010	0.025	-

TABLE II: Comparison of CMOS current references
* Measured results ** Simulated results

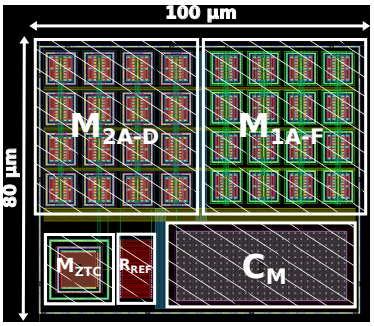


Fig. 6: Enhanced Bulk Driven OTA version self biased current reference layout

parison of published current references in similar process technologies. The main advantage of the presented solution is its low supply voltage requirement.

V. Conclusion

Forward body biasing lowers the MOSFET ZTC condition and this technique can be used to decrease the minimum supply voltage, as it has been demonstrated in the proposed self-biased current reference. A body input OTA has also been used to further reduce the minimum supply voltage and composite transistors were implemented to improve the OTA voltage gain. Transitor-level simulation results have shown TC_{eff} of 65 ppm/^{o}C from -55 to 125 ^{o}C and a fabrication sensitivity of σ/μ = 6.5 %, with 0.75 %/V of power supply sensitivity.

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