Investigation on the Switching Waveforms of GaN Power Devices to Gate Current Profiles

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***Abstract*—The extended use of Gallium Nitride (GaN) transistors in power applications, such as automotive, industrial and power distribution, leads practitioners and researchers to a review of the classical driving techniques, to meet the different characteristics of such devices compared to traditional ones, such as MOS and IGBT. In particular, the smaller intrinsic capacitances of GaN transistors allows faster switching transitions, thus decreasing the power dissipation during commutations. On the other hand, the higher slope of the switching waveforms drives high frequency resonant circuit that, using slower devices, would not be excited. This paper proposes a technique to obtain an optimal pair of non-oscillating switching waveforms, which exploits time-varying resistances in the power loop. A gate charge driving technique, based on the modulation of the gate current, is exploited for shaping the optimal waveforms by means of the power transistor itself. A simulation analysis was carried out considering two different driving waveforms and studying the sensitivity of ringing as a function of their significant parameters. Such analysis highlights that the optimal switching waveforms can be obtained by means of several driving shapes. Finally, a comparison with the RC snubbered circuit, in terms of efficiency and ringing, is reported to highlight the advantages of the proposed technique.**

***Index Terms*—GaN gate driver, EMI reduction, ringing suppression**

I. Introduction

In recent years, wide bandgap semiconductors have become more and more popular in power electronics applications because of their higher efficiency with respect to traditional silicon devices [1]. In particular, GaN transistors exhibit a lower intrinsic parasitic capacitances, resulting in a higher switching frequency. Voltage and current transitions, therefore, are characterized by high $\mathrm{dv/dt}$ and $\mathrm{di/dt}$, which may cause oscillations, worsen the electromagnetic (EM) performance and permanently damage the circuit components as a result of over-currents and/or over-voltages. Thus, switching waveforms should be tightly controlled to have the entire system operating in an optimal way.

The traditional approach when dealing with Si transistors is the use of RC snubbers and series gate resistance. Such solution allows one to remove the undesired oscillations, at the cost of lower efficiency and duration of transitions. Nevertheless, in the case of GaN transistors, the aforementioned drawbacks may not be acceptable.

Active Gate Driver (AGD) has become an established technique to address such issues. It consists of shaping the switching waveforms with the aim to reduce oscillations and overshoots, with negligible effect on efficiency. If the driver strength is modulated in a proper manner during transients, resonant circuits in the power loop are not excited and the slope of switching waveforms is barely affected, at the same time. In particular, gate resistance modulation [2], [3], staircase shaped gate voltage [4] or current [5], [6], have been successfully exploited. In principle, the power transistor should be slowed down during the Miller's plateau to not excite the resonant circuits, which results in a higher dissipation, since the transistor is kept in saturation.

On the other hand, little attention has been paid to AGD techniques for GaN devices. In this case, the gate driver should be able to modulate its strength with a sub-nanosecond time resolution. In particular, [8] and [9] propose a variable gate resistance, [10] and [11] an active $\mathrm{dv/dt}$ control and [12] a two-current level driver. However, a GaN driver with an optimal gate current waveform has not been presented yet. This work proposes a driving technique to lower the ringing phenomenon occurring on the switching node and current. A method to evaluate the optimal switching waveforms as a function of parasitic elements, and a technique to drive the power switch acting on gate charge are proposed. In particular, two different gate current waveforms are considered to highlight the pros and cons of each of them.

The paper is organized as follows: in Section II, a high side buck converter is analyzed to understand the effects of parasitic elements on the ringing. Section III proposes a criterion to prevent oscillations and a technique to obtain the optimal waveforms using the power GaN itself. Section IV reports a sensitivity analysis of the switching current as a function of significant parameters of the driving waveforms and a comparison between the proposed gate driver and the classical solution. Final remarks are withdrawn in the concluding section.

II. Switching transients in a buck converter

In this section, the switching behavior of a buck converter, shown in Fig. 1, is analyzed. Both high side and low side switches are GaN transistors, however, for the sake of simplicity, the low side one behaves like a free wheeling diode, meaning that its gate and source terminals are short circuited. The aim of the following analysis is to highlight which transitions cause voltage and current oscillations. In particular, it is assumed that the parasitic inductances $\mathrm{L_d}, \mathrm{L_s}, \mathrm{L_{p6}}, \mathrm{L_{p7}}$ (Fig. 1) are far smaller than the equivalent inductance of the DC link. Such hypothesis is meaningful, since GaN devices

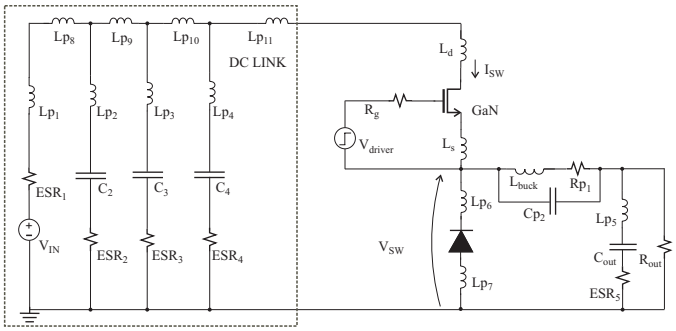

Fig. 1. Buck converter including its parasitic elements.

are typically available in lead-free packages. The analysis was performed assuming that the driver can source/sink all the needed current to turn-on/turn-off the switch, instantaneously.

A. High side switch turn-on

As long as the high side transistor is kept off, the load current flows through the freewheeling diode, which keeps the switching voltage $\mathrm{V_{sw}}$ to the constant value $-\mathrm{V}_\gamma$. When the driver voltage $\mathrm{V_{driver}}$ goes up to its on-value, the current flowing in the high side transistor, $\mathrm{I_{sw}}$ starts to increase, but the voltage $\mathrm{V_{sw}}$ remains at $-\mathrm{V}_\gamma$ until the diode turns off, i.e. when $\mathrm{I_{sw}}$ equals the load current $\mathrm{I_{out}}$. The rise time $\mathrm{t_r}$ of $\mathrm{I_{sw}}$ is only limited by the DC link parasitic inductance, $\mathrm{L_{p_{eq}}}$, (Fig. 3) accordingly to Eqn. 1.

$$t_r = L_{p_{eq}} \frac{I_{out}}{V_{in}}. \tag{1}$$

Such current transition can not cause any oscillations, because a constant voltage drops on all parasitic capacitances.

When the current $\mathrm{I_{sw}}$ reaches its nominal value, the diode turns-off and the voltage $\mathrm{V_{sw}}$ begins to rise. The power loop involved in this phase contains both the $\mathrm{L_{p_{eq}}}$ and the low side parasitic capacitance. This means that the transient of $\mathrm{V_{sw}}$ excites a resonant circuit, and uncontrolled oscillations of voltages and current take place. Fig. 2 shows the equivalent circuits modeling current and the voltage transitions, on the left and right side, respectively.

B. High side switch turn-off

When the driver turns-off the GaN transistor, the voltage drop across the high side switch starts to decrease. In this phase, the current $\mathrm{I_{sw}}$ is kept constant by the load, thus any current variation affects the inductance, and no resonance is excited (Fig. 2 on the right side).

Once the voltage $\mathrm{V_{sw}}$ has reached the value $-V\,\gamma$, the freewheeling diode turns-on and the current $\mathrm{I_{sw}}$ starts to decrease (Fig. 2 on the left side). Now the resonant circuit, consisting of the parasitic inductance $\mathrm{L_{p_{eq}}}$ and the high side parasitic capacitance, oscillates.

C. Equivalent Circuit

The previous analysis suggests that only one transition, the voltage one for the turn-on and the current one for the turn-off, is responsible for exciting the corresponding resonant circuit. Moreover, the analysis highlights that the frequency of oscillations could be different, since that the parasitic capacitance involved in the phenomena is not the same.

TABLE I
USED VALUES FOR COMPONENTS IN BUCK CONVERTER.

Name	Value	Name	Value	Name	Value
$\mathrm{ESR_1}$	$200\,\mathrm{m\Omega}$	$\mathrm{L_{p_1}}$	$18\,\mu\mathrm{H}$	$\mathrm{V_{in}}$	$52\,\mathrm{V}$
$\mathrm{ESR_{2,3,4}}$	$20\,\mathrm{m\Omega}$	$\mathrm{L_{p_{2,3,4}}}$	$50\,\mathrm{nH}$	$\mathrm{R_{p_1}}$	$2.4\,\mathrm{m\Omega}$
$\mathrm{ESR_5}$	$150\,\mathrm{m\Omega}$	$\mathrm{L_{p_5}}$	$30\,\mathrm{nH}$	$\mathrm{L_{buck}}$	$10\,\mu\mathrm{H}$
$\mathrm{C_{2,3,4}}$	$680\,\mu\mathrm{F}$	$\mathrm{L_{p_{6,7,9,10,11}}}$	$100\,\mathrm{pH}$	$\mathrm{C_{out}}$	$680\,\mu\mathrm{F}$
$\mathrm{C_1}$	$200\,\mathrm{pF}$	$\mathrm{L_{p_8}}$	$1\,\mathrm{nH}$	$\mathrm{V_{out}}$	$12\,\mathrm{V}$
$\mathrm{C_{p_2}}$	$10\,\mathrm{pF}$	$\mathrm{L_{s,d}}$	$500\,\mathrm{pH}$	$\mathrm{I_{out_{max}}}$	$20\,\mathrm{A}$

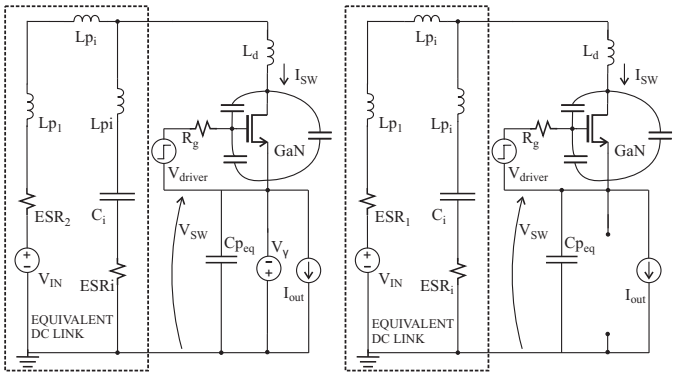

Fig. 2. Equivalent circuits for the current transition (left side) and for the voltage transition (right side) during turn-on and turn-off.

The values of $L_{p_{eq}}$ and of $C_{p_{eq}}$ can be extrapolated from the circuit in Fig. 1 using the procedure adopted in [13]. In order to validate the proposed equivalent circuit, a buck converter to step down an input voltage of $52\,\mathrm{V}$ to an output voltage of $12\,\mathrm{V}$ with the capability to provide the load with a current of $20\,\mathrm{A}$, was designed. The devices used in the converter are *EPC2001C* GaN transistors [7]. Table I shows the adopted values regarding the other components. All simulations were performed in *Cadence Virtuoso* environment. In particular, the switching current exhibits an oscillation at $\mathrm{f_{r1}} = 37\,\mathrm{MHz}$ after the turn-on, and one at $\mathrm{f_{r2}} = 56\,\mathrm{MHz}$ after the turn-off. From these values, it is possible to compute the parameters of the proposed equivalent model, resulting in $\mathrm{C_{p_{eq}}} = 1\,\mathrm{nF}$ and $L_{p_{eq}} = 18.5\,nH$. It should be noticed that the high side parasitic capacitance is already included in the model of the GaN transistor. The resonant frequencies of the complete circuit and of the proposed model are in good agreement both for the current $\mathrm{I_{sw}}$ and the voltage $\mathrm{V_{sw}}$, as shown in Fig. 4. On the other hand, the amplitudes of oscillations are different, since the ESR parasitic resistances are not included in the equivalent model.

III. OSCILLATION DAMPING

The equivalent circuit proposed in the previous section has been exploited to develop a method for damping oscillations. Such technique requires to properly dissipate the energy that,

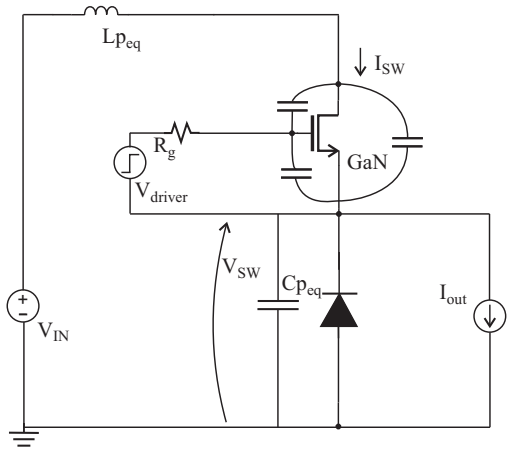

Fig. 3. Equivalent circuit modeling the ringing behavior of the buck converter.

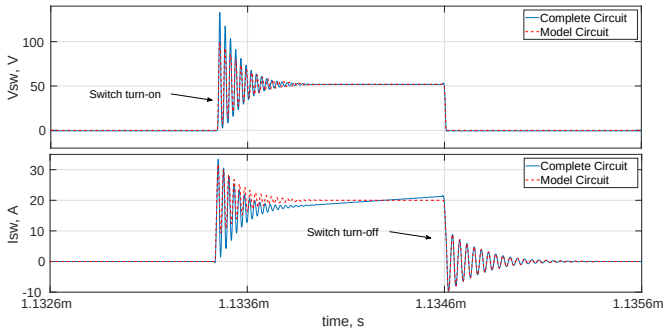

Fig. 4. Comparison between the switching waveforms of the buck circuit with parasitic elements (blue lines) and that of its equivalent circuit (red line). The voltage switching waveform is characterized only by the ringing at f_{r_1}, while, the switching current exhibits both ringing at f_{r_1} and f_{r_2}.

otherwise, would be exchanged by the aforementioned parasitics. For this purpose, a time-varying resistance in series to the high side switch and proportional to the derivative of V_{sw} (see Fig. 5 on the left side), and a time-varying conductance in parallel to it, proportional to the derivative of I_{sw} (see Fig. 2 on the right side), have been included in the circuit. Such power consuming elements are effective only during the transitions that can cause the oscillations, meaning that $R_t(t)$ works only during the voltage transition of the turn-on, while $G_t(t)$ is active only during the current transition of turn-off commutation. The values of $R_t(t)$ and $G_t(t)$ are chosen accordingly to Eqn. (2) where k_1 and k_2 are two constant coefficients.

$$R_t(t) = k_1 \frac{dV_{sw}}{dt} \qquad G_t(t) = -k_2 \frac{dI_{sw}}{dt} \tag{2}$$

A. Evaluation of coefficient k_1

In order to find the optimal value of k_1 coefficient, parametric simulations were carried out (Fig. 6). The aim of such simulations is to find out the best compromise between the amplitude of ringing and the transition speed. In accordance with the aforementioned analysis, only the slope of the switching voltage decreases because of $R(t)$. For the proposed goals, the optimal value of k_1 is approximately $400\,\mathrm{ps/A}$.

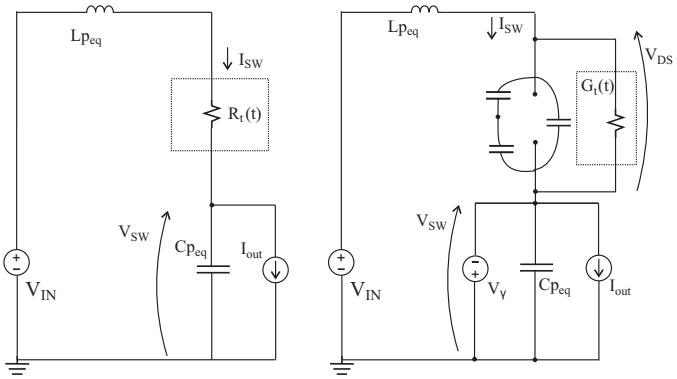

Fig. 5. Equivalent circuits of voltage transition during the turn-on with the $R_t(t)$ element (left side) and during the turn-off current transition with $G_t(t)$ element (right side).

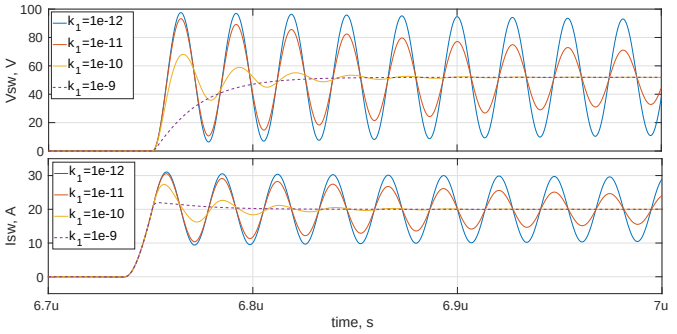

Fig. 6. Switching voltages and currents obtained performing a parametric simulation on k_1 coefficient during the voltage transition of the turn-on phase.

B. Evaluation of coefficient k_2

The same type of simulation was performed for evaluating the k_2 coefficient (Fig. 7). Also in this case, an inverse relationship between the amplitude of oscillations and the duration of the current transient exists. As in the previous case, a high value of such parameter implies a slower transition, whereas a lower value leads to oscillations. The optimal value of k_2 results to be $90\,\mathrm{ps/V}$, eventually.

C. Using GaN transistor to reproduce the optimal waveforms

$R_t(t)$ and $G_t(t)$ represent an intermediate step required to obtain the optimal switching waveforms, i.e. the faster and non oscillating ones. The behavior of such dissipative components should be reproduced exploiting the GaN transistor itself. In particular, during the turn-on, the voltage $V_{turn_{on}}$ (Fig. 8) should drop on the power transistor, whereas, during the turn-off, the current $I_{turn_{off}}$ (Fig. 8) should be entirely absorbed by the GaN switch. It is worth noticing that the diodes in the optimal driver circuit are only needed to clamp the driving voltage. For the sake of simplicity, only the turn-on optimal waveforms are considered in the following sections. In this paper, two different I_{driver} current waveforms, shown

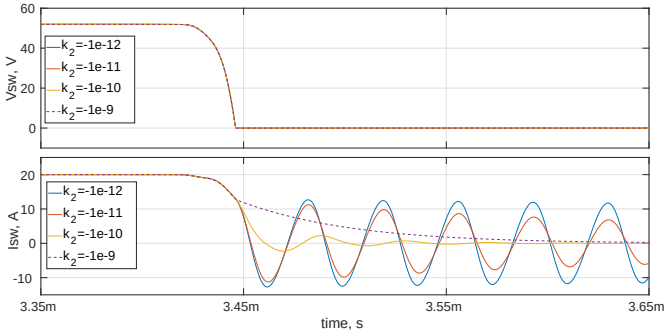

Fig. 7. Switching voltage and current obtained performing a parametric simulation on k_2 coefficient during the current transition of turn-off phase.

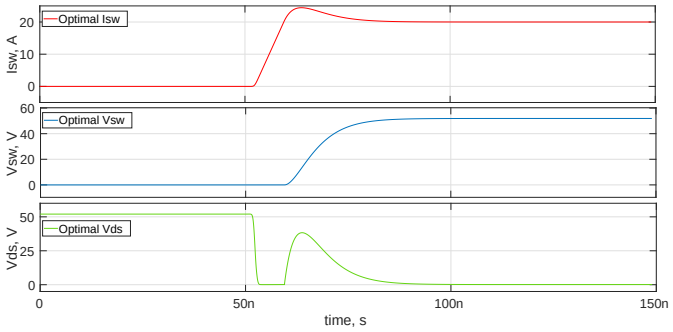

Fig. 9. Voltage and current waveforms that should be reproduced using the switch to obtain the optimal commutation during turn-on.

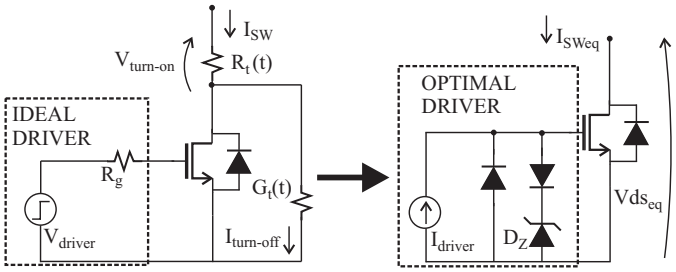

Fig. 8. Equivalent switch circuit with $R_t(t)$ and $G_t(t)$ (left side) and switch with optimal current driver (right side).

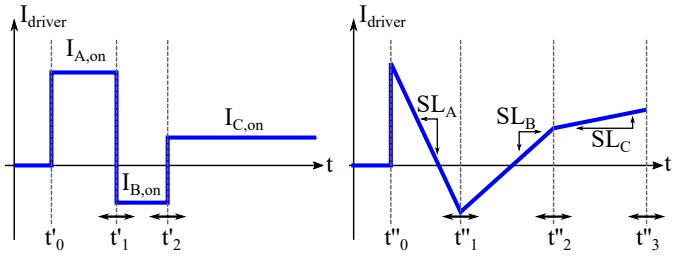

Fig. 10. Three-level current driver (on the left side) and three-slopes current driver (on the right side).

in Fig.10, are analyzed to highlight that the shape of the gate current is not crucial, but the key point is the matching of the optimal waveforms by means of the transistor itself. The first shape is a constant piecewise waveform where the second current level is negative, instead the second one is a variable slope saw-tooth waveform. Also in this case, there is a phase in which charge is extracted from the gate.

IV. Simulation Analysis

This section provides a validation of the proposed method by means of simulations. The parameters involved in the simulations are, for three-level constant waveforms, the first, the second and the third current levels, $\mathrm{I_{A,on}}, \mathrm{I_{B,on}}, \mathrm{I_{C,on}}$, respectively, and the time instants $\mathrm{t'_1}, \mathrm{t'_2}$ (Fig. 10 on the left side). Instead, for the variable slope saw-tooth driver, the considered parameters are the slopes $\mathrm{SL_A}, \mathrm{SL_B}, \mathrm{SL_C}$ and the time instances $\mathrm{t''_1}, \mathrm{t''_2}$ (see Fig. 10 on the right side). All involved parameters are swept of 5% around optimal value.

A. Three level constant piecewise driver

Firstly the finest parameters of the three-level constant piecewise were extrapolated to match the optimal waveforms. As shown in Fig. 11, they are in good agreement, meaning that the first proposed current driver, if properly tuned, allows the power transistor to emulate the $\mathrm{R(t)}$ behavior, thus removing the oscillations, completely. In order to assess such gate current waveform, sensitivity analysis were carried out, exploiting parametric simulations. In particular, Fig.12 depicts how the $\mathrm{I_{sw}}$ current is affected by a variation of $\mathrm{I_{A,on}}, \mathrm{I_{B,on}}, \mathrm{I_{C,on}}$. It can be noticed that the first level is the most critical, since the ringing amplitude increases, significantly. Similarly, Fig. 13 (top and middle plots) shows the higher sensitivity of parameters $\mathrm{t'_1}, \mathrm{t'_2}$ with respect to the previous ones. In the bottom plot of Fig. 13, finally, a variation of the slopes, i.e. the transitions from level 0 to $\mathrm{I_{A,on}}$, $\mathrm{I_{A,on}}$ to $\mathrm{I_{B,on}}$ and $\mathrm{I_{B,on}}$ to $\mathrm{I_{C,on}}$, is simulated, keeping the middle point constant in time. It should be noticed that no variation occurs on $\mathrm{I_{sw}}$, highlighting that the particular shape of the gate current is not crucial, if the injected/removed charge from the transistor is the same.

B. Variable slope saw-tooth driver

After the validation of the three-level current driver, a variable slope saw-tooth one was considered. A preliminary comparison with the optimal switching waveforms is reported, as shown in Fig. 14. Also in this case, the curves are in good agreement, as expected from the previously results of the slope variations, since only the net gate charge affects the results. As in the previous analysis, the sensitivity of significant parameters is simulated. Firstly, the different slopes were swept around the optimal value, resulting in a relevant sensitivity on slope $\mathrm{SL_A}$ with respect to the other two. Then, Fig. 16 reports the sensitivity analysis performed translating, at the same time, $\mathrm{t''_0}, \mathrm{t''_1}$ (top),$\mathrm{t''_1}, \mathrm{t''_2}$ (middle) and $\mathrm{t''_2}, \mathrm{t''_3}$ (bottom), and keeping the slopes constant at their optimal values. It can be noticed that the first two are the most significant for the ringing suppression.

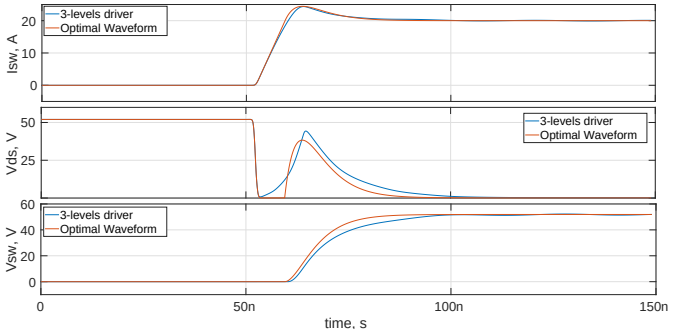

Fig. 11. Comparison between the optimal switching waveforms (red) and the that obtained exploiting the tuned three-level current driver (blue).

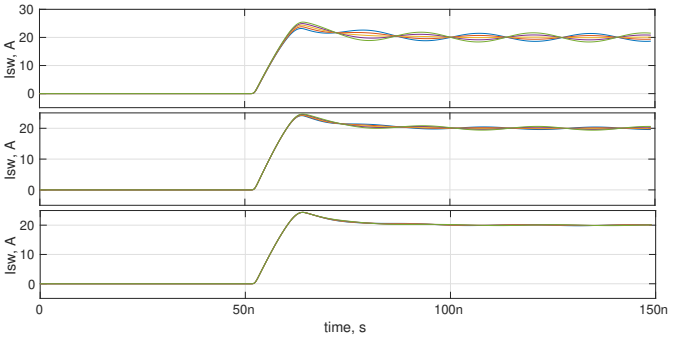

Fig. 12. Switching current waveforms obtained varying with a 5 % the level of $I_{A,on}$ (top), $I_{B,on}$, (middle) and $I_{C,on}$, (bottom).

TABLE II
COMPARISON BETWEEN THE MOST SIGNIFICANT PARAMETERS INTERESTING THE BUCK CONVERTER WORKING

	No Snubber	**Snubber RC with Rg**	**3-level**	**Slope sawtooth**
$\mathbf{P_{sw}}$	$1.62\,W$	$4.68\,W$	$3.66\,W$	$3.65\,W$
$\mathbf{P_{diode}}$	$221\,mW$	$198\,mW$	$200\,mW$	$199\,mW$
$\mathbf{P_{lsnb}}$	//	$1.43\,W$	//	//
$\mathbf{P_{hsnb}}$	//	$1.26\,W$	//	//
$\mathbf{P_{tot}}$	$1.84\,mW$	$7.57\,W$	$3.86\,W$	$3.85\,W$
$\mathbf{V_{sw_p}}$	$103\,V$	$58\,V$	$52\,V$	$52\,V$
$\mathbf{V_{ds_p}}$	$193\,V$	$65\,V$	$68\,V$	$68\,V$
$\mathbf{I_{sw_p}}$	$33\,A$	$30\,A$	$25\,A$	$25\,V$

C. Comparison with standard solution

The traditional solution consists of an high side and low side snubber with a fixed R_g. The design of the two snubbers was performed as reported in [13]. The comparison was carried out between no snubber, traditional approach and the two proposed gate waveforms. Table II lists the considered figures of merit which are: the power dissipated by the low side switch (P_{sw}), by the high side diode (P_{diode}), by the snubbers (P_{lsnb} and P_{hsnb}) and their sum (P_{tot}), and finally their peak values (V_{sw_p}, V_{ds_p}, I_{sw_p}). The data shows an increment of the efficiency of more than 50%, reducing the peak of the switching current and voltage. Finally, the three-level driver and the variable slope one are characterized by similar performance because they match the optimal waveform in the same way.

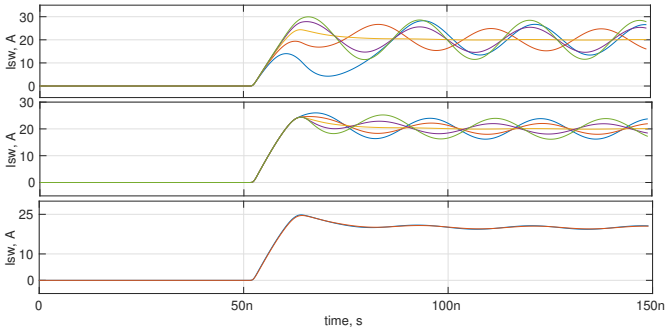

Fig. 13. Switching current waveforms obtained varying with a 5 % the value of t_1' (top), t_2' (middle) and the current slopes (bottom).

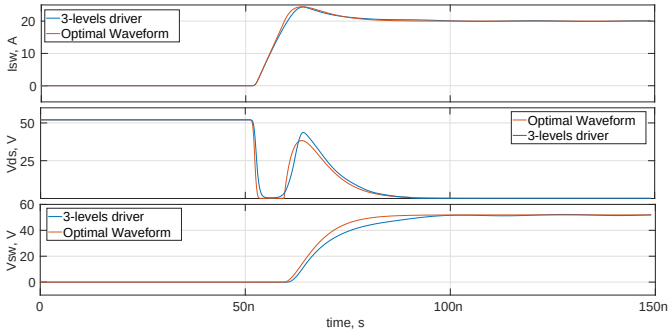

Fig. 14. Comparison between the optimal switching waveforms (red) and the that obtained exploiting the tuned slope variable saw-tooth current driver (blue).

V. CONCLUSION

In this paper, a method to extract the optimal switching waveforms for GaN transistors is presented. Firstly, the turn-on and turn-off commutations are analyzed referring to a high-side buck converter, then, the optimal switching waveforms are extracted by means of intermediate dissipative time-variant elements. The GaN transistor was driven to reproduce the obtained waveforms. In particular, a three-level constant current and a variable slope sawtooth current driver were considered, proving the effectiveness of the proposed method. Simulation results show that both current drivers are able to match the optimal waveforms. Finally, a comparison with standard solution, i.e. RC snubber and gate series resistance, shows that the proposed technique reduces the total dissipated power of about 50% respect to traditional approach, reducing the peaks of switching current and voltage significantly. The similar performance of the three-level gate driver and of the variable slopes one supports that the input waveform are equivalent, proving that the optimal matching can be obtained with several waveforms.

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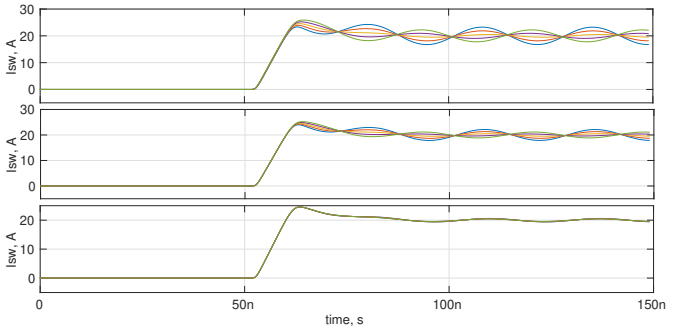

Fig. 15. Switching current curves with a $5\,\%$ variation on level $\mathrm{SL_A}, \mathrm{SL_B}, \mathrm{SL_C}$ (from the top to the bottom).

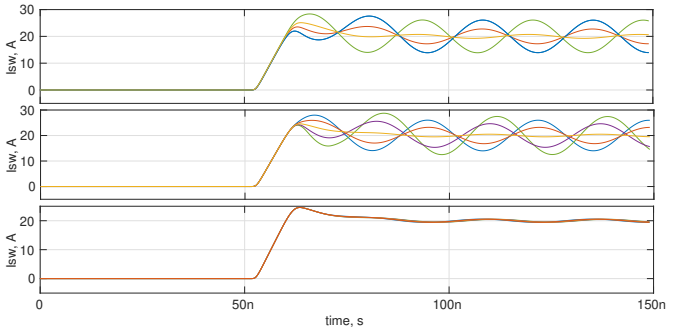

Fig. 16. Switching current curves with a $5\,\%$ variation of time offset (from the top to the bottom).

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