A High Voltage Dc-Dc Converter for HEVs with a Novel Floating Control Stage

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***Abstract*—High-side gate drivers to be used in EVs and HEVs should target high insulation voltage, as well as efficiency and monitoring capability. In traditional step-down converters, the entire control stage is referred to ground, thus either a pulse transformer or an isolated integrated gate driver is required. The paper proposes a buck converter having the entire control unit referred to the floating node. The design was carried out considering discrete components, which allows for low-cost and low-profile implementation. Simulations were conducted to validate the proposed converter, and to compare it with traditional high-side gate driver topologies. The overall efficiency results to be consistent with the other topologies, whereas the estimated occupied area and the cost, at PCB level, are both significantly lower.**

***Index Terms*—High-side driver, Gate driver, Floating control stage, dc-dc converter, HEVs**

I. Introduction

In Hybrid Electric Vehicles (HEVs), a dc-dc converter to step down the traction battery voltage, ranging from 200 V up to 400 V, to the auxiliary battery (14 V), is definitely required [1]. Power converters used in automotive applications should be designed to achieve reliability, high efficiency, wide operating temperature range, minimum weight and volume. To address such issues, SiC devices can replace traditional silicon-based power switches [2], since their power losses are lower and the required heat-sink can be smaller.

Traditional topologies of step-down converters, e.g. buck and buck-boost, include at least a high-side switch, which should be driven to behave, ideally, either as an open or a short. This implies that the driver of such transistor has to be referred to its source terminal. A gate driver requires a stable DC power supply and an on-off control signal which is responsible for the proper timing. Such signal is typically driven by the compensator (analog or digital), which in a standard architecture is referred to ground. In particular, such control stage should not be affected by noise or over-voltages coming from the power stage, as they can both cause undesired malfunctions. Level-shifter gate drivers, like those shown in [3]- [5], are an established solution, however, they do not provide electrical insulation between the control stage and the power stage.

When electrical insulation is required, as in the case of highly reliable application, pulse transformers are typically used, however, they are bulky, and can only be used to transfer an AC signal at the time. Opto-insulators and optical fibers can be even exploited, but their limited operating temperature range affects their application in harsh environments [6]. On the other hand, isolated gate drivers have been widely investigated in the last years, and successfully integrated [7]-[8]. The main drawbacks of such solution are the hardware complexity, since a transmitter and a receiver are necessarily required, and the reliability of the integrated isolation barrier.

Approaching from a different perspective, the entire control stage, i.e. the compensator, the gate driver and their corresponding power supply circuitries, may be referred to the floating node. The main advantage of such solution is that the control stage is not affected by noise coming from the power stage. Moreover, the input voltage is scalable to higher values with less efforts, since bulky isolators are no longer needed and the hardware complexity does not increase significantly. The aim of this paper is to propose a possible architecture and some preliminary simulations regarding such kind of converter. In particular, a 200 W hard switching buck is designed, along with the floating stage.

The paper is organized as follows. Section II reports some considerations on the most popular topologies of high side gate driver, then, in Section III, the proposed converter is described using a top-bottom approach and reporting some considerations regarding the design of each sub-part. Simulation results and a comparison of the required area and of the estimated cost are reported in Section IV, and, in the concluding section, some final comments are withdrawn.

II. High-side drivers

In order to turn on and turn off the high-side FET, the driving voltage should be referred to its source node SW, however, in a buck converter, such node swings from ground up to the input voltage V_{HV}. Level shifters, pulse transformers and isolated gate drivers are the most popular solutions to address this issue. Hereinafter, a brief description of each of them is reported, with the purpose of highlighting the pros and cons. In particular, it is assumed that an external low-voltage

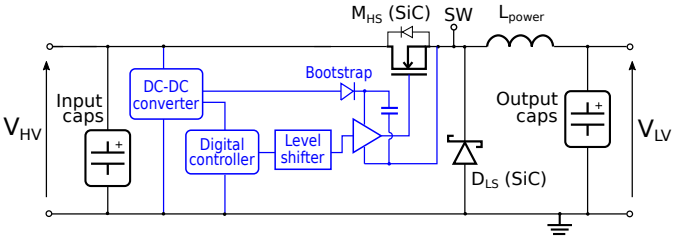

Fig. 1. Level shifter topology.

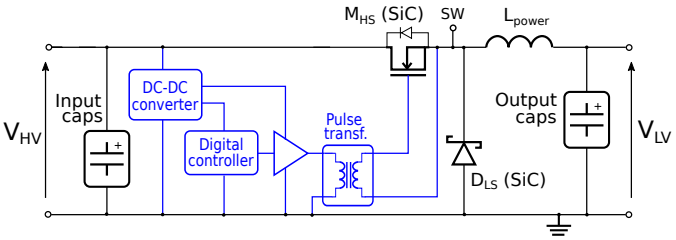

Fig. 2. Pulse transformer topology.

power supply is not available, thus the supply voltage for the gate driver and the controller should be derived from the input voltage itself.

A. Level shifter

When no galvanic insulation between the control and the power stage is strictly required, an integrated level shifter can be used, as depicted in Fig.1. The control stage is referred to ground, the integrated level shifter translates the on-off command to the switch source, and the bootstrap circuit is needed to provide the driver with a stable DC power supply. As far as integrated solutions are concerned, the isolation well can block up to $600\,\mathrm{V}$ using a standard CMOS process [9], conversely, the exploitation of SOI-CMOS technology allows for isolation voltage up to $1200\,\mathrm{V}$. This aspect limits the scalability of such topology to higher input voltage, since a safety margin between $\mathrm{V_{HV}}$ and the isolation voltage should be guaranteed in any condition.

B. Pulse transformer

Pulse transformers represent the traditional approach to achieve electrical insulation for voltages in the $1-5\,\mathrm{kV}$ range. The actual driver is upstream of the transformer, whose secondary port is connected to the gate terminal, as shown in Fig. 2. In particular, the low coupling capacitance between the primary the and secondary side of the transformer protect the control stage from the switching noise generated by the power stage [11]. When high voltage insulation is concerned, both clearance and creepage distances should be taken into account: the former refers to instantaneous voltages across the terminals of insulator, while the latter to long term failures, which are related to the RMS value of the working voltage [12]. In order to comply with safety standards, e.g. IPC-2221 [13], the physical dimensions of such transformer cannot be neglected, especially when targeting a low-profile design.

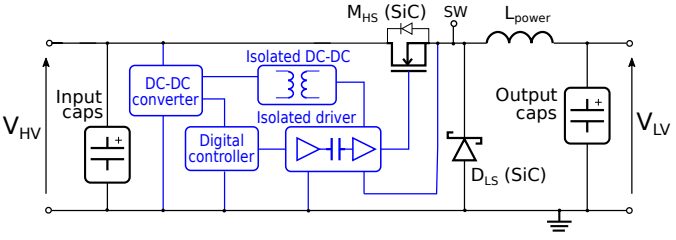

Fig. 3. Integrated isolated gate driver.

C. Integrated isolated gate driver

Isolated drivers have been recently integrated exploiting either on-chip transformer [15] or electro-magnetic resonant couplers [7]. The key idea underlying such technique is that the PWM signal is On-Off Keying (OOK) modulated and transmitted from the primary side to the secondary side, where it is demodulated and drives the actual gate driver, eventually. In particular, the use of a high frequency carrier, i.e. above $1\,\mathrm{GHz}$, leads to a reduction of both on-chip transformer and couplers. As far as the power supply of the gate driver is concerned, it should be referred to the switching node, meaning that either an insulated power supply, as shown in Fig. 3, or a bootstrap circuit is required. If the diode of the bootstrap circuit exhibits a breakdown voltage sufficiently high for the target application, the second solution may be preferred since magnetic components are avoided.

In such topology, the insulator material is typically $\mathrm{SiO_2}$ oxide, which is characterized by a dielectric strength of $500\,\mathrm{Vrms}/\mu\mathrm{m}$, approximately. Nevertheless, it suffers from the Time Dependent Dielectric Breakdown (TDDB) phenomenon [16]. Both intrinsic breakdown, which is caused by the generation of defects in the dielectric, and extrinsic breakdown, related to the pollution of dielectric by Cu atoms, affect the lifetime of the insulation barrier [17]. This last aspect should be carefully considered when targeting high reliability.

III. Proposed Converter

The architecture of the proposed system is shown in Fig. 4. It consists of a traditional buck converter with a free-wheeling diode, equipped with a floating control stage. A bootstrap circuit is required to provide the driver and the control stage with a constant DC power supply referred to the floating node. Input and output voltages are sensed and reported to the floating node, thus enabling monitoring and controlling functionalities. It should be noticed that only small signal diodes are placed at the interface of the floating stage; and since discrete components are used, such diodes can have the same breakdown voltage class of diodes in the power stage, thus the proposed topology does not suffer from scalability issues. The buck design was carried out to meet the specifications mentioned in Table I. In particular, the proposed converter was entirely simulated in Cadence Virtuoso environment, and off-the-shelf devices were preferred in anticipation to a prototype with discrete components.

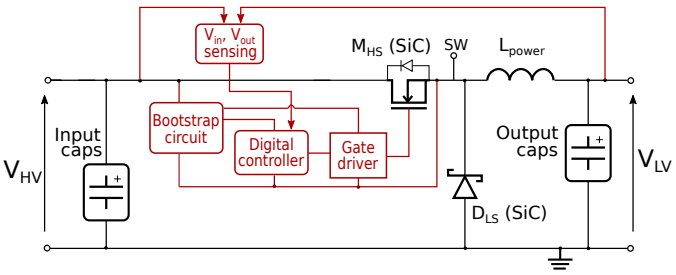

Fig. 4. Block level view of the proposed converter.

TABLE I
DESIGN REQUIREMENT.

Input voltage (V_{HV})	[200, 400] V
Output voltage (V_{LV})	14 V
Maximum output power (P_{out})	200 W
Topology	Buck with free-wheeling diode
Output voltage ripple	$\leq 200\,mV$

A. Power stage

Firstly, the switching frequency f_{sw}, which was kept constant to ease the design, should be fixed. The power dissipated by the high side SiC FET, M_{HS}, and by the low side SiC diode D_{LS}, is the sum of two terms: conduction and switching losses. Referring to the latter, it is proportional to the switching frequency. A low switching frequency, however, implies an higher current ripple on the power inductor, thus an heavier component, and the DCM (Discontinuous Current Mode) condition to occur at higher output current. Choosing an inductor with nominal value equals to $47\,\mu H$, then the lowest switching frequency to stay in CCM with an output current greater than the 25% of the nominal value, corresponds to 50 kHz. Table II shows the most significant parameters of the converter.

B. Bootstrap

The adopted topology is shown in Fig. 5, and it consists of a coarse-regulation stage plus two series LDOs to finely adjust the output voltages, which are the DC supply voltage of the driver, $V_{PS,drv}$, and of the control logic, $V_{PS,logic}$. The use of linear converters avoid high-frequency noise to be injected in the driver. When the high-side switch is on, the SW node is approximately at V_{HV}, thus the bootstrap capacitor C_{boot} should deliver all the charge needed with a negligible voltage drop on itself. The diode D_2 avoids the discharge of C_{boot} on the power stage and the reverse conduction of transistor M_z. On the other hand, when the high side switch is off, the bootstrap circuit is in parallel to the input capacitors, thus the voltage V_{unreg} can reach its maximum value. The value of the bootstrap capacitor should be chosen considering the maximum amount of charge (Q_{tot}) that it should be able to deliver to the load.

Then, settling an upper bound on the voltage drop $\Delta V_{boot,max}$ on C_{boot} during the on-time of the high side switch, it is possible to derive the following design expression

$$C_{boot} \geq \frac{\Delta V_{boot,max}}{Q_{tot}}. \tag{1}$$

TABLE II
PARAMETERS OF THE POWER STAGE, EVALUATED FOR $V_{HV} = 300\,V$

Parameter	Expression
Nominal output current	$I_{out} = \frac{P_{out}}{V_{LV}} = 14.3\,A$
Inductor current ripple	$\Delta I_L = \frac{V_{HV}-V_{LV}}{f_{sw}L}\frac{V_{LV}}{V_{HV}} = 5.7\,A$
Input cap current ripple	$\Delta I_{C_{in},rms} = I_{out}\sqrt{d(1-d)} = 3\,A$
Output cap current ripple	$\Delta I_{C_{out},rms} = \frac{\Delta I_L}{\sqrt{12}} = 1.6\,A$
High side switch current	$I_{HS,peak} = 17.16\,A$ $\overline{I_{HS}} = 0.66\,A$
Low side switch current	$I_{LS,peak} = 17.16\,A$ $\overline{I_{LS}} = 13.6\,A$

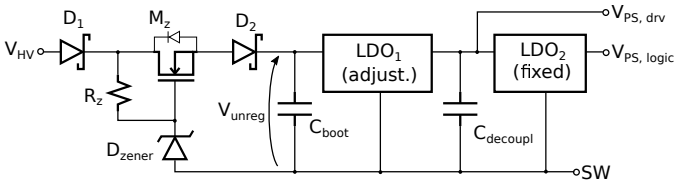

Fig. 5. Bootstrap circuit.

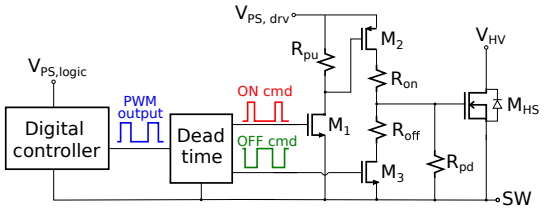

Fig. 6. Gate driver circuit.

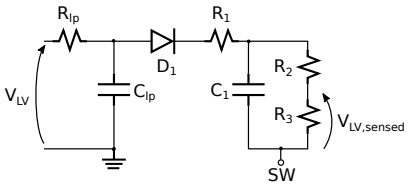

Fig. 7. Input and output voltage sensing circuitry.

C. Gate driver

The adopted topology is shown in Fig. 6, where M, M_2, M_3 MOSFET are used as open or close switch, $R_{on} = R_{off} = 1.8\,\Omega$ limit the gate current i_{gate} during turn on and turn off transients, respectively, and finally a bistable circuit with a delayer introduces some dead time to avoid cross conduction through the driver itself. The value of resistor R_{pu} and of dead time t_{dead} should be chosen to minimize both the power dissipation during the on-time, i.e. when M_1, M_2 on and M_3 off, and the turn off time of M_2. Thus, parametric simulations were carried out to determine which values maximize the overall efficiency in nominal condition, resulting in $R_{pu} = 250\,\Omega$ and $t_{dead} = 800\,ns$.

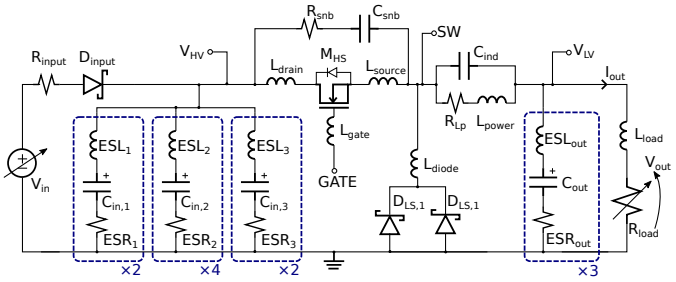

Fig. 8. Power stage with parasitics.

TABLE III
USED VALUES FOR COMPONENTS IN BUCK CONVERTER.

Name	*Value*	*Name*	*Value*	*Name*	*Value*
Power stage					
ESL_1	40 nH	$C_{in,1}$	680 μH	ESR_1	400 mΩ
ESL_2	15 nH	$C_{in,2}$	68 μH	ESR_2	150 mΩ
ESL_3	1 nH	$C_{in,3}$	1 μH	ESR_3	100 mΩ
ESL_{out}	20 nH	C_{out}	68 μH	ESR_{out}	80 mΩ
$L_{drain,src}$	1 nH	L_{gate}	100 pH	L_{diode}	1 nH
C_{ind}	10 pF	L_{power}	47 μH	R_{Lp}	2.4 mΩ
R_{in}	50 mΩ	L_{load}	10 nH	$R_{load,nom}$	980 mΩ
R_{snb}	3.2 Ω	C_{snb}	1.4 nF	$V_{LV,nom}$	14 V
Pulse transformer and isolated driver					
R_{open}	$1, M\Omega$	$R_{close,1}$	$2.5, \Omega$	$R_{close,2}$	$0.3, \Omega$
R_f	2Ω	C_{ac}	1 μH	L_{prim}	1.4 mH
L_{leak}	300 nH	C_{coupl}	1 pF	R_{pd}	10 kΩ
$C_{PS,drv}$	10 μF	R_{ser}	1 Ω	$V_{PS,drv}$	18 V
$V_{PS,logic}$	5 V	L_{wind}	38 μH	k	7.7

D. Input and output voltage sensing

The output and input voltage should be sampled by the controller to regulate the duty cycle of the PWM signal. In the proposed topology, however, the reference of the compensator is the floating node SW, thus some circuit is required in between. The output voltage V_{LV} of the buck converter can be sensed by the floating control stage exploiting the circuit shown in Fig. 7. In particular, R_{lp} and C_{lp} implement a first order low pass filer; D_1 and C_1 are a peak detector, and R_2, R_3 are needed to adapt the sensed voltage to the input voltage range of the analog-to-digital converter of the control stage.

IV. Simulation result

Simulations were carried out to compare the proposed topology with standard high-side driver solutions, i.e. pulse transformer, shown in Fig. 9, and isolated gate driver, depicted in Fig. 10. In the following analysis, the same power stage, which is shown in Fig. 8 and whose values are reported in Table III, was considered for all topologies. Diodes and FET were simulated using the netlist provided by the manufacturer, which already include the parasitic inductance of the package. The parasitic elements of passive components were considered, as well. Moreover, a snubber circuit was required to damp oscillations occurring at the turn-off of the high-side switch.

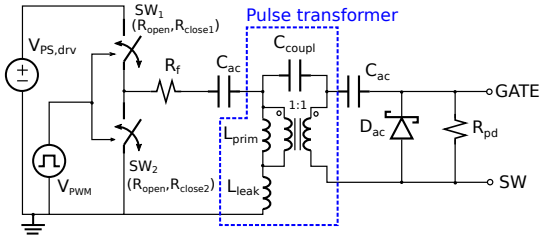

Fig. 9. Simulated pulse transformer topology.

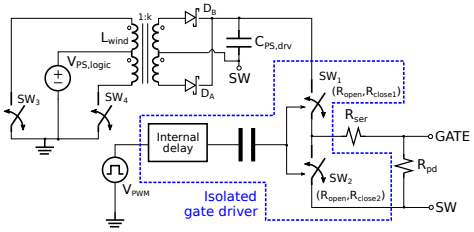

Fig. 10. Simulated isolated integrated gate driver topology with isolated power supply.

A. Parasitic estimation

In the analysis of the proposed converter, parasitic elements should be estimated to do not neglect their effects on performance, in particular on efficiency. The parasitic capacitance C_p of the power inductor L_{pow} was evaluated from the corresponding resonant frequency of the chosen power inductor. Regarding the modelling of input and output capacitors, it was assumed that ceramic capacitors were used for values $\leq 1\,\mu$F since they are available in SMD technology, and electrolytic ones for larger values. For ceramic devices, it was assumed $ESL = 1\,nH$ and $ESR = 0.1\,\Omega$, instead, for electrolytic caps, the corresponding ESR was evaluated from $tan(\delta)$ parameter, and the ESL assuming, as a rule of thumb, 1 nH per millimeter of height.

B. Efficiency

The efficiency evaluation of the power converter was performed considering the overall input power with respect to the one delivered to the load. For the sake of simplicity, in the case of pulse transformer and isolated gate driver, it was assumed that an extra dc-dc converter, which is not reported in the aforementioned schematics, is able to step the input voltage V_{HV} down to $V_{PS,drv}$, with an efficiency of 0.9. Parametric simulations were carried out considering a load current in the range $[4, 20]$ A and input voltages $V_{HV} = 200, 300, 400$ V, then the resulting curves are reported in Fig. 11, 12 and 13, respectively. It is worth noticing that the efficiency of the pulse transformer topology is approximately equal to that of the integrated isolated gate driver. On the other hand, the efficiency of the proposed driver worsens when the input voltage increases, because the bootstrap circuit is basically a dissipative converter.

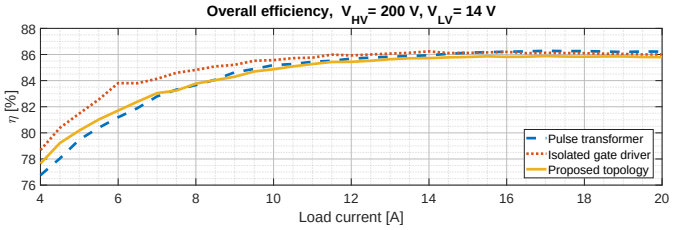

Fig. 11. Efficiency corresponding to an input voltage V_{HV} equals to 200 V.

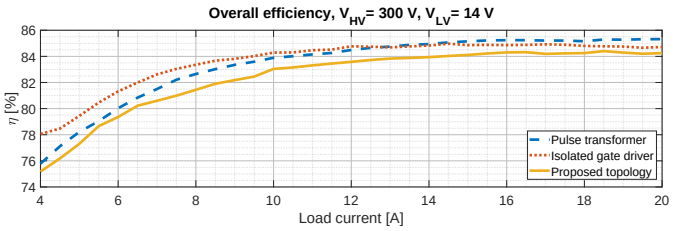

Fig. 12. Efficiency corresponding to an input voltage V_{HV} equals to 300 V.

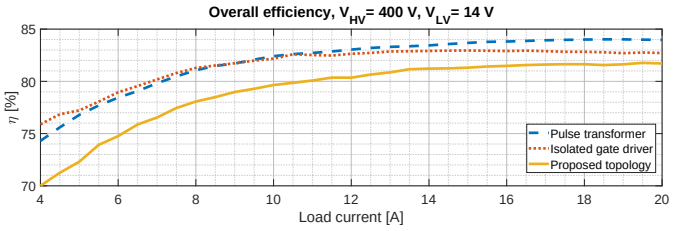

Fig. 13. Efficiency corresponding to an input voltage V_{HV} equals to 400 V.

In particular, for the proposed converter working under nominal conditions, the contribution to the dissipated power for each component is reported in Fig. 14. It can be noticed that the major contribution is related to the low side diodes, as expected. As far as the bootstrap and the gate driver are considered, the power dissipation is distributed among their components accordingly to Fig. 15.

C. Area and cost estimation

Besides electrical parameters, the occupied area at PCB level and the cost become of particular importance when dealing with automotive applications. Thus, for the analysed topologies, the overall dimensions and costs of each sub-circuit were estimated and compared. Gate driver, input and output voltage sensing circuits as well as bootstrap or high voltage to low voltage converter are considered in the following analysis, whereas power stage and controller are neglected since it was assumed that they remain unchanged. In the case of pulse transformer and isolated gate driver, an extra dc-dc converter is required to step the input voltage down to $V_{PS,drv}$, $V_{PS,logic}$. Figure 16 gathers the data related to the estimated occupied area. It results that the proposed topology is characterized by a 15% and 50% area reduction with respect to pulse transformer and isolated gate driver, respectively. In particular, the floor-planning for each analysed topology was depicted, as shown in Fig. 18, 20 and 19. The Bill Of Materials (BOM) of such

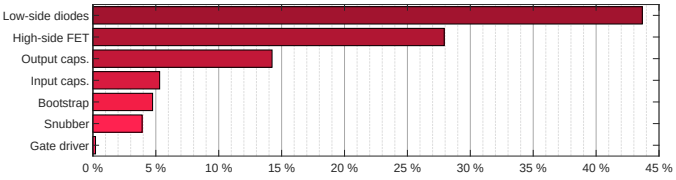

Fig. 14. Partial contributions of the power by the entire converter.

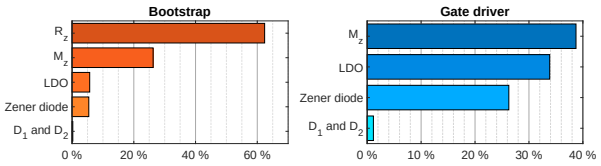

Fig. 15. On the left, partial contributions of the power dissipated by the proposed bootstrap, on the right, by the proposed gated driver.

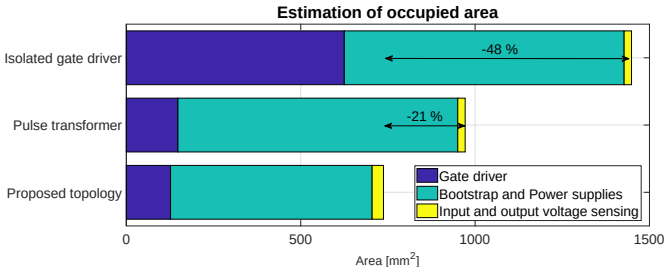

Fig. 16. Comparison between the required area for the different solutions.

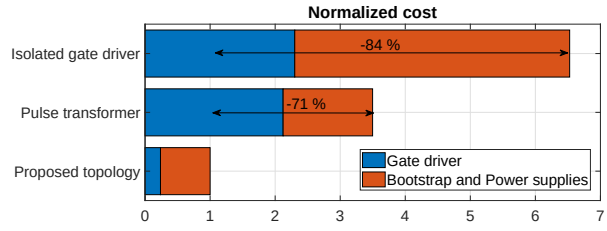

Fig. 17. Comparison between the costs for the different solutions, normalized to the proposed topology.

layouts were subsequently exploited to estimate the overall cost of each solution. It is worth noticing that the proposed topology leads to a significant cost reduction, as shown in Fig. 17, since it allows one to save 71 % and 84 % on the cost, compared to pulse transformer and isolated gate driver.

V. Conclusion

In this paper, a hard-switch buck converter with a novel high side driver, targeting HEVs application, is reported. With respect to standard solutions, the entire control stage is referred to the switching node, thus avoiding pulse transformer and integrated isolated gate driver. In particular, such topology is immune to noise coming from the power stage. Using discrete diodes at the interface of the floating stage, the proposed topology can scale better than integrated level shifters. The bootstrap stage, the driver itself and a circuit for the input and output voltage sensing are described in details. Simulations

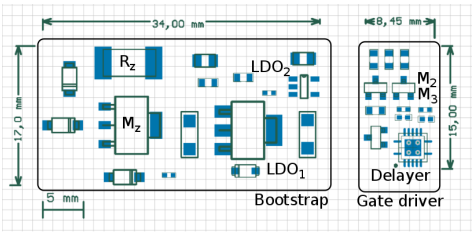

Fig. 18. Floor-planning, at PCB level, of the proposed solution using off-the-shelve components. Top layer is shown in blue, top overlay in dark green.

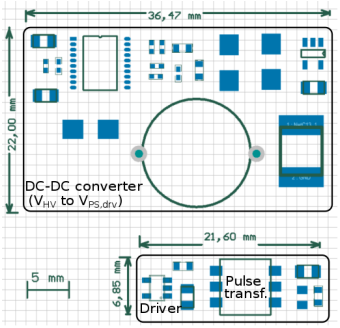

Fig. 19. Floor-planning, at PCB level, of the pulse transformer topology using off-the-shelve components. Top layer is shown in blue, top overlay in dark green.

were carried out to validate the proposed topology, in particular the efficiency is in agreement with standard high side driver solution, and the estimated occupied area to implement the proposed topology using discrete components is up to 50% lower. Finally, the estimated cost is significantly lower with respect to standard solutions, allowing one to save 84 % of the cost.

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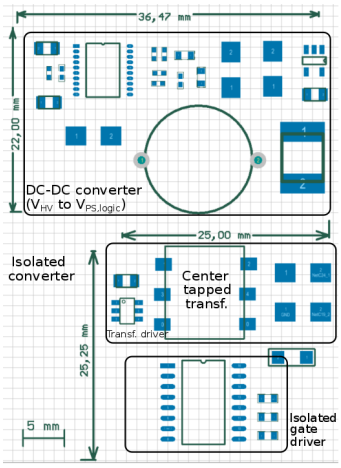

Fig. 20. Floor-planning, at PCB level, of the integrated isolated gate driver using off-the-shelve components. Top layer is shown in blue, top overlay in dark green.

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