

A Criterion for an Optimal Switching of Power Transistors

Original

A Criterion for an Optimal Switching of Power Transistors / Quitadamo, MATTEO VINCENZO; Raviola, Erica; Fiori, Franco. - STAMPA. - (2019). (Intervento presentato al convegno 2019 IEEE 12th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo) tenutosi a Haining, Hangzhou (China) nel 21-23 October 2019) [10.1109/EMCCompo.2019.8919738].

Availability:

This version is available at: 11583/2756493 since: 2019-09-30T13:01:03Z

Publisher:

IEEE

Published

DOI:10.1109/EMCCompo.2019.8919738

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright

IEEE postprint/Author's Accepted Manuscript

©2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

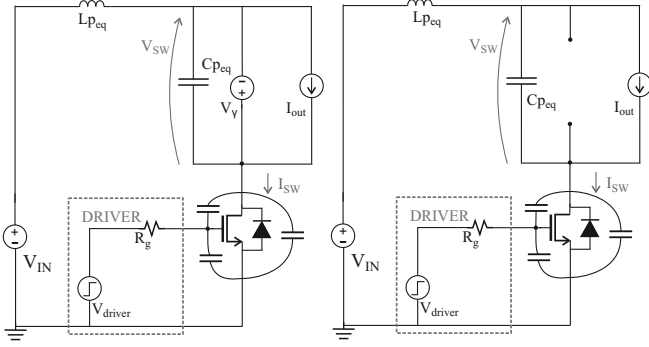


Fig. 2. Equivalent circuits for the current transition (left side) and for the voltage transition (right side) during turn-on and turn-off.

until its command is not under the threshold. During this phase, the current is constant and $L_{p_{eq}}$ is not subjected to any current variation, so no resonance is excited (Fig. 2 on the right side). When the voltage V_{sw} has reached the value $-V_{\gamma}$, the freewheeling diode turns-on and the current I_{sw} starts to decrease (Fig. 2 on the left side), exciting the resonant circuit. As a result, to damp such resonance, the turn-off current transient has to be controlled.

III. PREVENTING THE OSCILLATION

As described in the previous section, only the voltage V_{sw} transition excites the resonant circuit during the turn-on, resulting in the undesired oscillations. On the other hand, the I_{sw} current transition, is responsible for ringing during the low side switch turn-off. The key point is that, to prevent oscillations from taking place, it is required to dissipate energy only during the aforementioned transitions. Thus, a resistance and a conductance were inserted in series and in parallel to the low side power switch, respectively. Such elements, $R_t(t)$ and $G_t(t)$, dissipate energy only during the resonance exciting transitions, with a time-variant values that depend on the derivative of V_{sw} (Fig. 3 on the left side) and of I_{sw} (Fig. 2 on the right side), respectively. In such way only the needed amount of energy is dissipated, without affecting the efficiency. The values of $R_t(t)$ and $G_t(t)$ are chosen to follow (1).

$$R_t(t) = k_1 \frac{dV_{sw}}{dt} \quad G_t(t) = k_2 \frac{dI_{sw}}{dt} \quad (1)$$

The values of coefficients k_1 and k_2 were evaluated performing parametric simulations on their values.

$R_t(t)$ and $G_t(t)$ were introduced in the power loop only to obtain the optimal switching waveforms. During the voltage transition of the turn-on phase, the switch should be driven so that the voltage $V_{turn-on}$ (Fig. 3) drops on power transistor. Instead, for the turn off phase, the switch should be driven to limit the current flowing in the parasitic inductance, thus absorbing the excess of current $I_{turn-off}$. The diodes included in the optimal driver circuit are required to clamp the driving voltage to the maximum and minimum desired values.

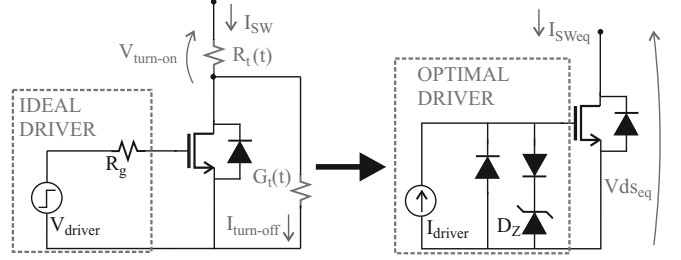


Fig. 3. Equivalent switch circuit with $R_t(t)$ and $G_t(t)$ (left side) and switch with optimal current driver (right side).

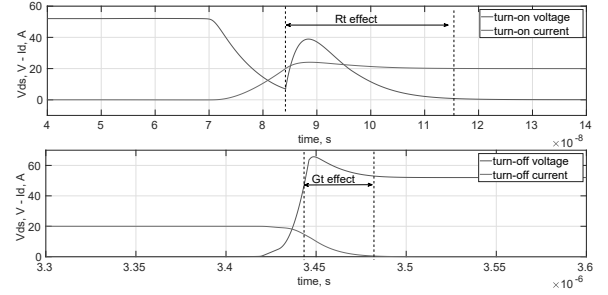


Fig. 4. Voltage and current waveforms that should be reproduced using the switch to obtain the optimal commutation during turn-on and during turn-off.

The optimal transistor waveforms, shown in Fig. 4, can be closely reproduced exploiting a three-level current driver.

1) *Turn-on*: The three phases for the turn-on (Fig. 5), can be explained as follows:

- The first level consists of the switch turn-on with all the driver available current $I_{A,on}$. During this phase the switching current I_{sw} reaches the nominal value and the drop voltage on it starts to decrease from the V_{in} value.
- The level $I_{B,on}$ should be negative and its goal is to increase the voltage drop on the switch, to reproduce the behavior shown in Fig. 4.
- The level $I_{C,on}$ leads slowly the switch voltage approximately to $0V$ while the switching voltage V_{sw} reaches V_{in} .

2) *Turn-off*: The turn-off behavior is the dual of the turn-on and consists of the following three steps:

- The first level $I_{A,off}$ is the maximum current that the driver can absorb, and allows the switch voltage to reach rapidly its nominal value.
- Level $I_{B,off}$ turns-on the switch to reduce the I_{sw} slope.
- The third level $I_{C,off}$ is negative and leads the switch off.

IV. SIMULATION RESULTS

In this section the three-level gate driver technique is validated performing parametric simulations, and a comparison in terms of speed and dissipated power with the classical solution, i.e. fixed R_g and two RC snubber, is reported.

A. Three level current driver validation

Once defined t_0 and I_A for both the commutations, parametric simulations were performed to tune t_1 , t_2 , I_B and I_C . Fig.

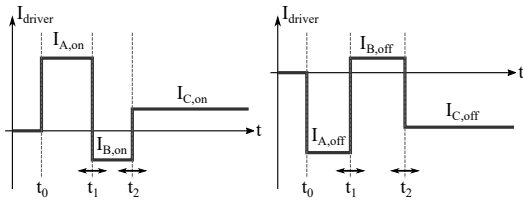


Fig. 5. Current driver for the turn-on phase (on the left side) and for the turn-off phase (on the right side).

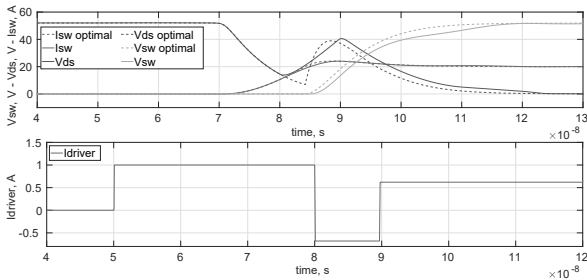


Fig. 6. Comparison between the optimal switching waveform and the ones obtained with the three level gate driver during the turn on.

6 shows, in the top graph, a comparison between the optimal turn-on waveforms and the ones obtained driving the power transistor with the proposed driver. All the curves are in good agreement and both the switching voltage and current are not affected by oscillations.

B. Comparison with standard solution

The traditional solution consists of an high side snubber in parallel to the freewheeling diode and a low side snubber in parallel to the power switch, with a fixed R_g . A diode is insert in parallel to R_g to create a low impedance path for the turn-off. The comparison was conducted considering three different topologies, i.e, no snubber, traditional approach and proposed technique. Table I lists the considered figures of merit. The data shows that the proposed technique removes completely the switching voltage overshoot, reduces the current peak but the maximum value reached by the V_{ds} voltage is slightly greater. In both cases, the commutation times of the proposed solution are between the other two topologies. Finally the most significant improvement is the power saving which is greater than 50% compared to the classical solution. Finally, Fig. 7 shows a comparison between the amplitudes of the frequency spectra of the switching current for the analyzed circuits. The spectrum of the no snubbed circuit presents two peaks at 27 MHz and 37 MHz as expected, while the other two are smoothed, and are characterized by a less rich frequency content.

V. CONCLUSION

This paper proposed a novel criterion for controlling the switching waveforms of power transistor avoiding oscillations and reducing the stress of components. In the first part, the commutations of a lowside buck are analyzed to determine

TABLE I
COMPARISON BETWEEN THE MOST SIGNIFICANT PARAMETERS INTERESTING THE BUCK CONVERTER WORKING

	No Snubber	Proposed technique	Snubber RC with Rg
P_{sw}	1.42 W	3.78 W	4.95 W
P_{diode}	231 mW	199mW	200 mW
P_{lsnb}	//	//	1, 17 W
P_{hsnb}	//	//	1, 95 W
P_{tot}	1.65 W	4 W	8.27 W
$t_{I_{sw,on}}$	8.22 ns	8.22 ns	24.5 ns
$t_{V_{sw,on}}$	6 ns	38 ns	70 ns
$t_{I_{sw,off}}$	18 ns	60 ns	60 ns
$t_{V_{sw,off}}$	9 ns	9 ns	18 ns
$V_{sw,p}$	104 V	52 V	52 V
$V_{d,s,p}$	81 V	67 V	62 V
$I_{sw,p}$	32 A	24.5 A	33.8 A

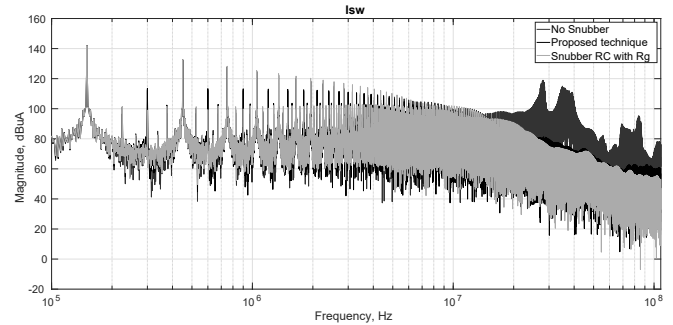


Fig. 7. Comparison between the EM spectrum of the analyzed topologies.

which phases are truly responsible for the starting of oscillations. A three levels current gate driver is proposed, and its parameters are extracted by means of parametric simulations in order to match the optimal waveforms. With respect to previous works, in the second phase of the turn-on/turn-off, charge is extracted/injected from/to gate, with the effect of avoiding ringing shorting the commutations less respect to the classical RC snubber solution. From efficiency point of view, preliminary results have shown a 50% power saving with respect to the traditional approach. The complete version of the paper will contain further simulation results, focusing on the extrapolation of the optimal switching waveforms.

REFERENCES

- [1] L. Middelstaedt, J. Wang, B. Stark, and A. Lindemann, "Direct Approach of Simultaneously Eliminating EMI-Critical Oscillations and Decreasing Switching Losses for Wide Bandgap Power Semiconductors", IEEE Transactions on Power Electronics, vol XX, pages YY, April 2019.
- [2] H. Dymond, J. Wang, et al. "A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI", IEEE Transactions on Power Electronics, vol. 33, issue 1, pp. 581-594, Jan. 2018.
- [3] M. Rose, J.Krupar, and H. Hauswald, "Adaptive dv/dt and di/dt control for isolated gate power devices", 2010 IEEE Energy Conversion Congress and Exposition, Sept. 2010.
- [4] M. Blank, T. Glück, A. Kugi and H.-P. Kreuter, "Slew rate control strategies for smart power ics based on iterative learning control", in Proceedings of Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX,USA, Mar. 2014, pp. 2860-2866
- [5] N. Idir, R. Bausiere and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," in IEEE Transactions on Power Electronics, vol. 21, no. 4, pp. 849-855, July 2006.