A Timing Pixel Front-End Design for HEP Experiments in 28 nm CMOS Technology

A Timing Pixel Front-End Design for HEP Experiments in $28\,\mathrm{nm}$ CMOS Technology

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***Abstract*—This work describes the design of a low-power low-jitter, analog front-end for timing-pixel radiations sensors. The circuit will provide the input stage for the front-end ASIC proposed for the TimeSpOT project that will be manufactured in a commercial $28\,\mathrm{nm}$ CMOS process. This front-end is designed to be part of 4D tracking detectors for future high data rate high energy physics experiments. This research aims at realizing $55\,\mu\mathrm{m} \times 55\,\mu\mathrm{m}$ pixels with sub $100\,\mathrm{ps}$ resolution within less then $10\,\mu\mathrm{W}$ power consumption.**

***Index Terms*—CMOS, ASIC, Front-End, Pixel Sensor, Timing, 4D Tracking**

I. Introduction

The goal of High Energy Physics (HEP) experiments is to measure rare events with high statistics.

Future trackers need to be designed to sustain the high data rate that will be produced by the primary events which is expected to be of $3\,\mathrm{GHz\,cm^{-2}}$[1]. Current tracking techniques has proved to be inadequate, producing an excessive number of miss-tracks and ghost-tracks. Common 3D Tracking consists in inferring the particle trajectory on the base of a set of point positions in 3D space, captured with layers of 2D pixel detectors.

4D Tracking can solve the identification problem with the addition of the time information to the position one, enabling tracking algorithms to rely on momentum and time correlation criteria. In order to make this technique feasible research efforts are needed both in terms of sensor and front-end electronics design. Moreover the new tracker will face new challenges posed by the large data bandwidth produced by the front-end, and by the high radiation hardness that will be required near the interaction point.

The time TimeSpOT (Time & Space real-time Operating Tracker)[2] project by INFN aims to develop a demonstrator of a 4D Tracker suitable for the next generation of experiments to be done at the Large Hadron Collider (LHC) in CERN, Geneva [3][4][5]. It will consists in a scaled-down version of a full 4D Tracking chain comprising the fast sensors matrix[6][7], the pixel front-end ASIC and a full speed track reconstruction system implemented in FPGA. 3D sensors [8] were selected, rather then the common planar ones, on the base of their fast signal, natural radiation hardness and contained signal variation.

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This work consisted in designing the prototype analog front-end for TimeSpOT . It was developed in a commercial $28\,\mathrm{nm}$ CMOS technology, which has been selected to provide both faster amplification stages and higher integration density. The ASIC design was submitted in October 2018 for manufacturing.

The target specifications in terms of spatial and timing resolution for the pixel channel are respectively of $55\,\mu\mathrm{m} \times 55\,\mu\mathrm{m}$ and less then $100\,\mathrm{ps}$. The target time resolution is required for the single measure, therefore any random contribution to the measure (e.g. jitter) must be below $30\,\mathrm{ps}$. Considering the chosen pixel area, the expected signal rate per channel will be Poissonian distributed with an average of $75\,\mathrm{kHz}$, this will pose an upper limit on the total dead-time per measure of $1.8\,\mu\mathrm{s}$ for the whole system (with a confidence level of $99\,\%$).

Moreover, in order to be compliant with a power dissipation around $300\,\mathrm{mW\,cm^{-2}}$, power consumption per channel must be kept below $10\,\mu\mathrm{W}$. At least half of the available power must be left to the TDC and the control logic. The analog front-end was designed for at most $5\,\mu\mathrm{W}$ of static power consumption. Bearing in mind that the technology supply voltage V_{dd} is $900\,\mathrm{mV}$, the available bias current must be below $10\,\mu\mathrm{A}$.

The system was optimized and designed around the target radiation sensor using its simulated signal and electrical characteristics[9]. Attention was paid in order to build a robust design in terms of PVT variation since the design must be suitable to be replicated in thousands of channels over a large area.

II. Analog Front-end Design

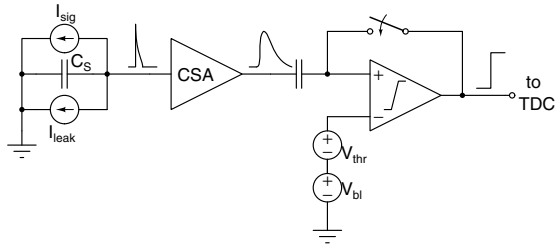


Fig. 1: Schematic block of the proposed Front-end and sensor equivalent circuit.

A schematic representation of the proposed pixel architecture is presented in Fig. 1. The first component of the chain is Charge Sensitive Amplifier (CSA), a transimpedance stage which produce a voltage signal with fixed rising time and amplitude proportional to the charge associated to the input current signal. This signal is compared with a voltage threshold using a Leading Edge Discriminator (LED) with offset compensation. The rising edge of the digital pulse generated in this way is then used as the start signal for a Time to Digital Converter (TDC) which digitize the time difference between the start signal and the stop one, which in this case is the next rising edge of a reference clock. In principle there will be one TDC per pixel.

Therefore, the selected architecture is a binary one with added timing information. Information on particle charge can, in any case, be extracted from the signal Time Over Threshold (TOT), since it is linearly correlated to the charge.

Finally a charge injection circuit, which mimics the sensor signal and electrical characteristics, has been inserted for both testing purpose of the prototype and as a calibration utility of the target pixel architecture.

The offset compensation circuit enables an absolute setting of the voltage threshold V_{thr} above the signal baseline V_{bl}; and equalize channel variability due to process and mismatch variations. Usually this is performed using continuous time techniques [10] resulting in costly calibrations in terms of area, power and complexity. This works adopts the solution of a discrete time circuit [11][12] to efficiently calibrate a timing system. The layout of the circuit is presented in Fig. 2, it occupies a $50\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$ area excluding power rails.

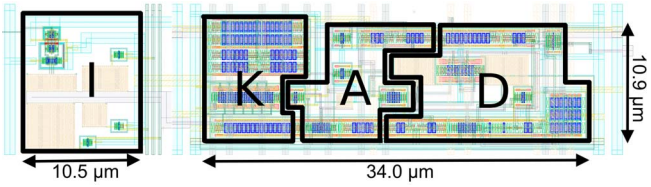
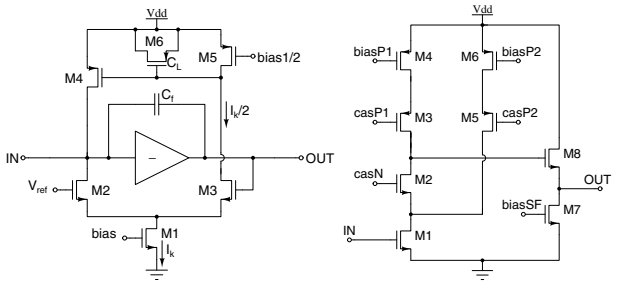


Fig. 2: Layout of a single channel of the proposed front-end. (I) Charge injection, (K) Krummenacher filter, (A) Core Amplifier, (D) Discriminator.

A. Preamplifier

The selected preamplifier is a CSA with DC current compensation. The capacitive feedback is realized with a $4\,\mathrm{fF}$ MOM capacitor, while the resistive one is implemented with a Krummenacher filter[13] which provides also the leakage current compensation. A schematic of this feedback element is presented in Fig. 3a. For high frequency signals this element behaves as a resistive feedback path by sensing the output at the gate of M_3 and acting on the input node through M_4. At lower frequency the differential cell formed by the branch of M_2-M_4 and M_3-M_5 reacts to the imbalance of its currents caused by the current sunk by the sensor on the output node, compensating it. Capacitor C_L is used to separate the two frequency operating regions.



(a) (b)

Fig. 3: Transistor level schematics of the CSA feedback circuit (a) ans its core amplifier (b).

While the maximum expected value for the sensor leakage current is $15\,\mathrm{nA}$ and the total Krummenacher's current I_k must be slightly grater than it, I_k value was selected to be $50\,\mathrm{nA}$ due to stability reasons. Therefore the feedback element gives a negligible fraction of the total power budget. On the other hand it uses a relatively large portion of the design area in order to obtain good pairs matching and to implement the MOS capacitor C_L.

The core amplification stage of the CSA is a telescopic cascode amplifier with split bias branches. The schematic of this element is presented in Fig.3b. This architecture was chosen in order to increase the load while maintaining a stable biasing with the small available voltage headroom. The sizing of this element is critical in terms of timing performance since this stage introduces most of the jitter of the entire chain.

A key aspect in the design a low jitter amplifier in this power constraint condition is to reach a compromise between bandwidth and noise. The first approach was to oversize every transistor in order to reduce to a few percent the flicker noise. Then every thermal contribution, except for the one of the input transistor, was minimized. As result the input transistor contributes to more than $60\,\%$ to the CSA total noise. The usage of any local triple-N-well was avoided in order to eliminate any unnecessary capacitance to small signal ground.

Finally a source follower is used as buffer in order to protect the cascode output high impedance node. The biasing current for this stage is $0.5\,\mu\mathrm{A}$ current, while the one of the first stage is $2\,\mu\mathrm{A}$ at nominal power level.

B. Discriminator

The proposed discriminator is formed by a first differential amplification stage followed by a single ended stage buffered with an inverter. The schematic is presented in Fig. 4. The first stage is designed to be a fast low-gain stage with small capacitive input in order to minimise the load presented to the previous stage. The second stage is a cascode common source amplifier which increases the total gain generating a fast transient signal which is then buffered by the last inverter. The first and second stages draw $2\,\mu\mathrm{A}$ and $500\,\mathrm{nA}$ respectively. The chosen offset compensation scheme has favorable consequence from a design point of view: having the liberty to not account for mismatch variations on the compensated device by over

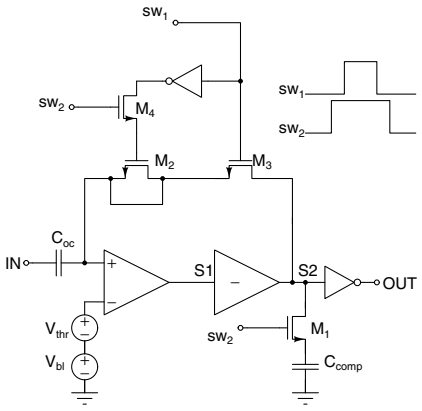


Fig. 4: Schematic block of the proposed LED with offset compensation.

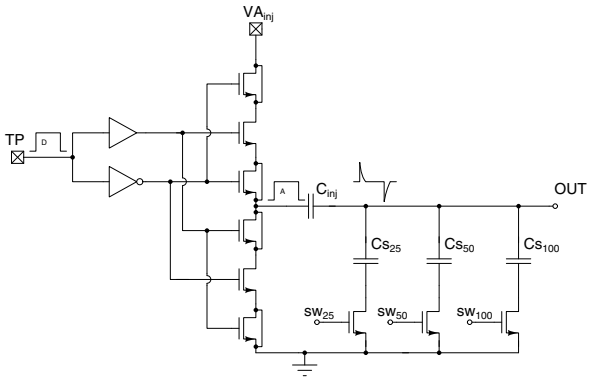


Fig. 5: Transistor level schematic of the charge injection circuit.

sizing transistors opens the possibility to use short length device and thus obtain larger bandwidth.

The offset compensation operates by recording the voltage offset between the discriminator input terminals on the capacitor C_{OC}. In particular the transistor M_3 is used as switch to close the negative unitary feedback path between the non inverting input and the second stage output (which is inverted) forcing the voltage on the OC node to equalize the one on the inverting input minus the offset. During the compensation process the voltage at the inverting input is set to the desired V_{bl}, then, during the measure, threshold V_{th} is added in the same terminal.

The NMOS switch M_1 and the capacitor C_{comp} are used to stabilize the circuit during the compensation procedure. In order to avoid instability during M_3 switching, M_1 needs to be previously opened and closed after. M_2 is a dummy switch used to compensate the charge injection of M_3 on C_{oc}.

The compensation time represents a dead time for the point of view of the system. In order to keep it contained the recorded voltage must be stable for an adequate amount of time. This was achieved limiting unwanted C_{oc} charges and discharges. It must be noted that increasing C_{oc} capacitance value was not an option due to the excessive increase in area occupation. The adopted solution was to limit every parasitic current on C_{oc} terminals. The switch-off current of M_3 was reduced with proper transistor sizing. Another big contribution was given by transistor gate leakage current. The discriminator first stage input transistors leakage was limited by adopting thick oxide devices. The same method can't be used for M_2: using thick oxide device for it and therefore M_3 will increase the switch-off current to an unacceptable level. NMOS switch M_4 was then used to drive M_2 gate at high impedance during the measure phase (removing the large voltage applied across M_4 oxide layer). M_3 doesn't represents a problem because of its small gate source voltage during operation.

C. Charge Injection Circuit

This block simulates the behavior of the sensor by both producing the current signal and emulating its capacitance C_S. A schematic of this circuit is presented in Fig. 5. Signals of both polarities can be generated charging and discharging the capacitor C_{inj} between ground and an analog level V_A, utilizing two charge-injection compensated NMOS switch driven by two complementary digital signals. Capacitor C_{inj} was sized in order to produced the desired characteristic time, the injected charge can be selected varying V_A. C_S value can be selected between 25 fF and 175 fF with a 25 fF step, in order to explore the circuit performance in relation to this parameter.

III. Simulations

TABLE I: Simulated Front-End Parameters

Input Signal	**Delta-like**		**Simulated Sensor**	
Power [µW]	***4.1***	***7.2***	***4.1***	***7.2***
G [mV fC^{-1}]	190	168	150	124
σ_n [mV]	2.8	2.0	2.8	2.0
ENC [e]	94	77	120	103
t_{pk} [ns]	16.4	7.7	18.2	10.2
t_A [ns]	2.1	2.1	4.2	3.5
TOT [ns]	100	98	79	78
SR [mV ns^{-1}]	53	98	39	68
σ_j [ps]	54	21	74	30
σ_p [ps]	66	65	67	66
σ_{mm} [ps]	33	26	40	29

Description in the text.

A first evaluation on the performance of the system is presented in Tab. I. For these simulations the setup was: V_{thr}=20 mV, C_S=150 fF and Q_{in}=2 fC (which is the estimated deposit of a minimum ionizing particle). The selected circuit was first evaluated with nominal power consumption level (with core amplifier total current I_{amp} =2.5 µA) and at the maximum power consumption testable on the prototype chip (I_{amp} =6.25 µA). A delta response of the circuit is presented to illustrate its ideal operation, then, the same parameters were evaluated using signals taken from sensor physics simulation (which presents a $\sim 200ps$ signal duration). Fig. 6 presents the two output signals (extracted from transient noise simulation) in this condition, rms jitter variation as function of input charge due to slope variation is also presented

in the inset. Firstly CSA signal characteristics were evaluated by the mean of the its charge to amplitude gain G, the output rms noise σ_n, the related ENC and signal peaking time t_{pk}.

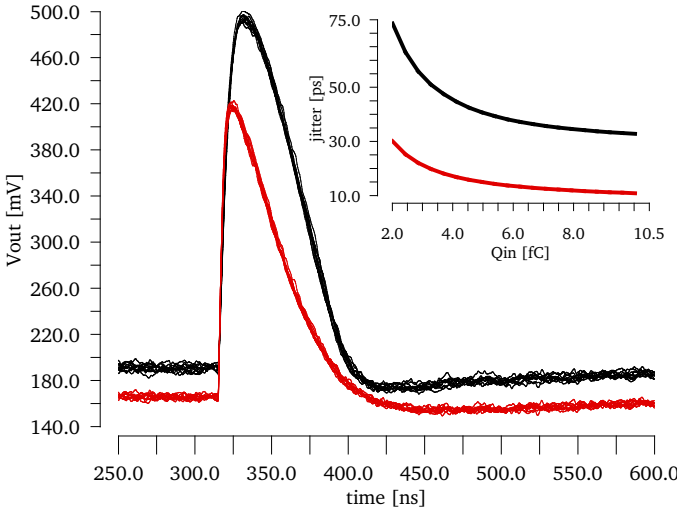


Fig. 6: CSA output signals for 2 fC input charge, at nominal (black) and high (red) power consumption. Insert: rms jitter as function of input charge.

As can be seen G suffer from a reduction compared to ideal one of $206\,\mathrm{mV\,fC^{-1}}$(computed using C_f and input transistor gate-drain capacitance). Observing the delta response, a first cause of this effect can be attributed to finite open loop gain of the core amplifier coupled with the relatively large sensor capacitance C_S. Using sensor signals, a further reduction can be observed due to charge development time. As expected increasing the power consumption will increase the input transistor transconductance, reducing σ_n.

Moreover the increase on core amplifier bias can be seen on t_{pk}, the larger transconductance of the max power case enables a faster charge of C_f, C_S and all transistors and parasitics capacitances. The effect of non ideal signal moves systematically t_{pk} of $\sim$2 ns.

In terms of timing performance both time of arrival t_A and TOT of the signal were taken in consideration. t_A was defined by the time difference between the input signal initial development and the discriminator $V_{dd}/2$ crossing. For the timing measure small variation on t_A are essential, in this work different contribution were investigated: jitter, process and mismatch variations. These contribution are presented by the mean of their rms values: σ_j, σ_p and σ_{mm} respectively. σ_p and σ_{mm} were extracted from Monte Carlo simulations. The slew rate SR is also reported since it represents a key factor in the conversion of voltage fluctuations into time ones. This parameter is evaluated around the threshold crossing point.

Jitter results show that, in the worst case scenario of a power consumption below 5 µW per channel and realistic signal shape, the proposed front-end will not be capable to deliver the desired performance. However, simulations shows promising results within a 75% increase on power consumption in respect to the nominal one.

Mismatch variations show that the current design can satisfy the requested performance by adopting minor per-channel digital corrections by taking advantage of the charge injection circuit. This result is achieved thank to offset compensation circuit, for reference the uncompensated values for σ_p and σ_{mm} in the best case were 650 ps and 160 ps respectively.

In terms of event rate performance, the simulations shows a recovery time for the baseline after a 10 fC signal of 1.4 µs, the probability to have two events inside this time frame is 0.5%. The time in which the baseline drift on the discriminator input terminal determines a t_A error of 20 ps is 600 µs, after the end of offset correction procedure. Considering 150 ns for the duration of compensation process, the channel will be inactive for 0.25‰of the time causing an average signals loss of 0.24‰. The total t_A difference due to time walk of the full signal range is evaluated to be of 250 ps, requiring a more advanced discrimination scheme or a digital correction technique which will be investigated in a future prototype.

IV. Summary

The proposed front-end occupy a fifth of the total pixel target area, proving to be a sufficiently compact solution. It exhibits, thanks to the offset compensation technique, small mismatch variation are achieved. It shows promising results in terms of timing performances of 74 ps and 30 ps rms jitter, within 4.1 µW and 7.2 µW power consumption respectively. Both the signal and compensation related dead-times are sufficiently short to sustain the expected signal rate. The first 28 nm design was submitted to the foundry at the end of 2018. The prototypes will be testes in the first half of 2019. Future development will investigate the possibility of more efficient solutions for both the preamplifier core stage and its feedback element.

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