4-Channel Front-End Integrated Circuit For Readout of Large Area of SiPM under Liquid Argon

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Alejandro D. Martinez R.
DET, Politecnico di Torino & Istituto Nazionale di Fisica Nucleare, Sez. Torino
alejandro.martinez@polito.it
Turin, Italy

***Abstract*—This paper presents the structure and transistor-level design of CMOS front-end amplifier for the readout of large area SiPM at LAr temperature (87 K). The front-end circuit, a trans-impedance amplifier and a summing amplifier, has been designed using a standard 110 nm CMOS technology, and the simulation results with the foundry PDK are included in this work. Each stage is implemented in a Folded Cascode Operational Trans-impedance Amplifier (OTA) architecture with a power rail of +1.25 V and -1.25 V, a power consumption of 95 mW and an open-loop gain over 100 dB. The target sensor is a SiPM tile of 24 cm^2 produced in the Darkside collaboration project, with 6 MΩ of quenching resistance and 6 nF/cm^2 capacitance. For a single photoelectron (250 fC), the front-end can achieve a signal-noise ratio above 12 and a jitter better than 45 ns.**

I. INTRODUCTION

Liquid argon (LAr) time projection chamber (TPC) technology will be used on future experiments for neutrino and direct dark matter detection experiments such as DarkSide20K [1] or ProtoDUNE [2]. The high photodetection efficiency, PDE $>$ 40 %, robustness and the low cost of silicon photomultipliers (SiPMs) has created a huge interest on using these sensors for the instrumentation of such frontier detectors. Extensive R&D on the cryogenic performance of silicon sensors allows the development of near ultra-violet SiPM technology to be optimised for operation at LAr temperature [3], [4]. This work describes the design of a front-end amplifier architecture to readout a large areas of SiPMs at Liquid Argon (LAr) temperature (87 K) using a standard CMOS 110 nm technology. The target sensor is a 24 cm^2 SiPM tile developed by the Darkside collaboration (Fig. 1). The circuit has been designed to be compliant with the readout topology described in [5]. A 2-series 3-parallel grouping configuration is used to decrease the total sensor capacitance, estimated 6 nF/cm^2, and thereby the tile is divided into 4 quadrants of 6 cm^2. Each quadrant is connected to a low-noise Trans-impedance amplifier (TIA), which reads out the SiPM tile with a total capacitance of 9 nF.

The Trans-impedance Amplifier has been designed with a Folded Cascode OTA proposed by the work in [6], adding a modification explained in chapter II. The FC architecture provides a large DC gain (108 dB) with a good bandwidth (350 KHz) in this work. These features are essential for a Front-End circuit with a large input capacitance provided by the detector.

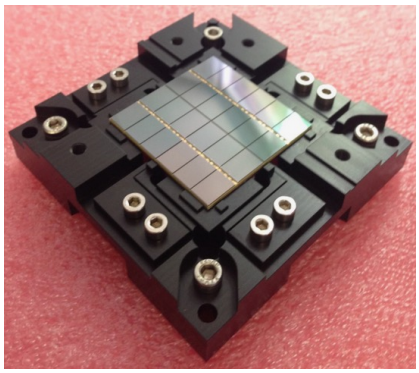

Fig. 1: A 24 cm^2 SiPM tile developed by the Darkside Collaboration.

The Folded Cascode architecture has been designed to reduce the probability of hot carrier effect in the 110 nm standard CMOS technology. Thus, some hot carrier reduction techniques were applied to increase the lifetime of transistor, such as the reduction of drain-source voltage in order to reduce the stress on transistors, and a longer channel length to reduce the internal electric field. Additionally, the NMOS transistors present a larger channel length than PMOS transistor, due to the fact that these are more susceptible under low temperature conditions [7].

The TIA has been simulated using a cryogenic SiPM electrical model (Fig. 4). A Spice model was developed, based on extracted characterisation parameters, for simulations at 300 K and 77 K [8]. This model generates a current signal proportional to the overvoltage value applied within the SiPM pins (i.e 5 VoV) over the quenching resistor at both 300 K and 77 K.

II. DESIGN AND IMPLEMENTATION

This paper describes the transistor-level design and simulations for the TIA input stage and the voltage summing amplifier with unity gain. Each stage has been implemented in a Folded Cascode architecture (Fig. 2). This OTA uses a PMOS input transistor with an NMOS cascode. This configuration provides a low Flicker noise [9], [10]. The input transistors (M1 and M2) operate in weak inversion. Thus, the aspect ratio

is computed following Eq. (1). The bias current is computed basing on Eq. (2).

$$\left(\frac{W}{L}\right)_{1,2} \geq \left.\frac{(C_o * GBW)}{2\beta_p \Phi_t e^{\frac{Vgs-V_{th}}{n\Phi_t}}}\right\} \quad (1)$$

$$I_{M1,2} = 2n\beta_p \left(\frac{W}{L}\right)_{1,2} \Phi_t^2 e^{\frac{Vgs-V_{th}}{n\Phi_t}} \Bigg\} \quad (2)$$

With:

- $I_{dM1,M2}$ = 500 uA;
- GBW, Gain Bandwidth product;
- $\beta_p = \frac{\mu_p C_{ox}}{2}$, μ_p carrier mobility of PMOS and C_{ox}, Silicon oxide capacitance;
- Φ_t, Thermal voltage 26 mV, 6.7 mV at 300 K, 77 K;
- C_o, Capacitance on the output node;
- n, Slope factor $\frac{C_{ox}-C_{dep}}{C_{ox}}$, C_{dep}, Depletion capacitance;

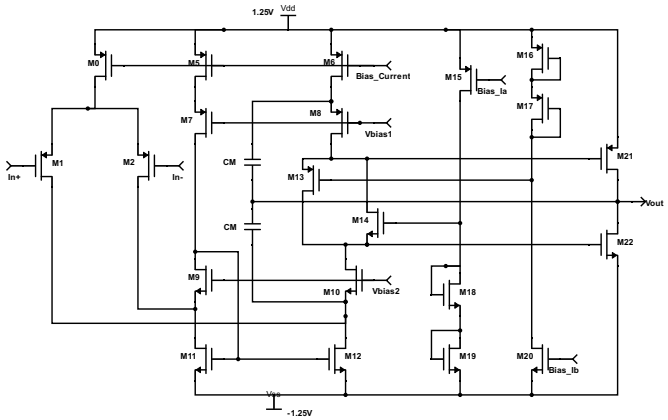

Fig. 2: Transistor-level design of Folded Cascode.

The Folded Cascode circuit uses a class AB amplifier on the output to enhance the total DC gain up to 108 dB. Furthermore, the circuit employs a frequency Miller compensation to regulate the phase and gain margin in order to avoid an instability condition related to the second pole. The Miller compensation is performed by the capacitor C_M together with the transconductance of output transistors (M_{21} and M_{22}) shown in Fig. 2. Consequently, the slew rate of the Folded Cascode is limited by the compensation capacitance (C_M), as described Eq. (3). Furthermore, the front-end circuit provides a dynamic range described by Eq. (4). The transfer function, considering the detector capacitance and feedback components is described by Eq. (5). The bandwidth (W_o) strongly depends on the detector capacitance, which, in this case, affects considerably the frequency response, as shown Eq. (6).

$$SR = \frac{I_{ss}}{C_M} \quad (3)$$

$$DR = V_{DD} - V_{CC} - 2V_{od} \quad (4)$$

With:

- V_{dd}, V_{cc} = +1.25, -1,25 V Voltage supply;
- I_{ss}= 500 uA;
- V_{od}, Overdrive voltage of transistors M_{21} and M_{22};

The output swing is much higher than a conventional Folded Cascode since this output node can swing from +0.9 V to -0.9 V keeping (M_{21}) and (M_{22}) in the saturated region. Hence, an output swing of 1.8 V from a 2.5 V supply is obtained.

$$H(s) = \frac{-R_f}{s^2 + s\frac{W_o}{Q} + W_o^2} \quad (5)$$

$$W_o = \sqrt{\frac{GBW}{R_f C_d}} \quad (6)$$

With:

- C_d, Detector capacitance, Q, Quality factor;
- R_f, feedback resistor of TIA;

The second stage consists of a summing voltage stage, using a folded cascode amplifier with a higher driving capability and a larger Miller compensation to guarantee stability during a load variation or open circuit on the output node. The simplified schematics of the full front-end is shown in Fig. 3

The Front-End electronic was designed to reach a signal-to-noise ratio (SNR), defined as the peak value of a single photo-electron (PE) signal divided by total r.m.s. output noise voltage, higher than 8.

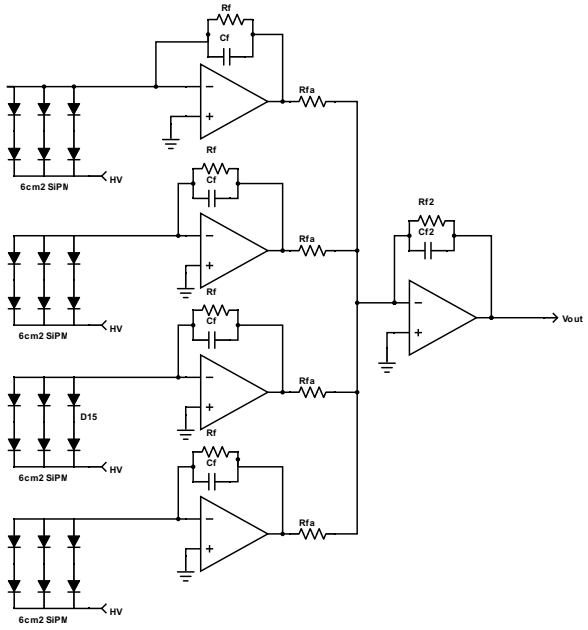

Fig. 3: Simplified schematics for the readout of 4 quadrants

III. SIMULATION RESULTS

The designs were simulated using standard Spice models of 110 nm CMOS technology provided by the foundry PDK (Process Design Kit). The mathematical extrapolation of the

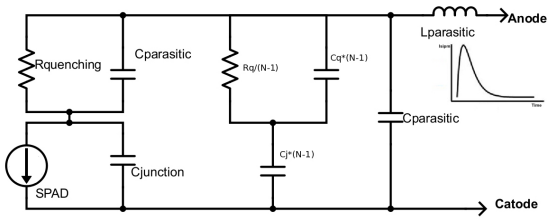

Fig. 4: SiPM electrical model with the parasitic inductance due to interconnections

BSIM models provide an approximate response of the MOSFET to be obtained at cryogenic temperature of 77K, since semiconductor foundries do not provide characterisation qualified models for temperature corners below $-40°$ C. However, we assumed the reliability of the drain current and transconductance of transistors within simulation at 77K justified by previous works [11]. To perform the simulations of a single PE, a 1 cm^2 cryogenic SiPM electrical model (160000 SPADs) with a detector capacitance around 6 nF, a charge of 250 fC and a quenching resistance of 6 MΩ at 77 K is used [12], as shown in (Fig. 4). The expected recovery time at 77K is in the order of 300 ns.

The equivalent noise charge is strongly dependent on the sensor capacitance. The flicker (ENC_f) and series white noise (ENC_w) contributions to the total noise are given by Eq. (7). The dynamic range of the amplifier is limited by the maximum output voltage at the output stage, and is in the order of 40 charge-equivalent photo-electrons.

$$ENC_f = \frac{C_d}{e}\sqrt{A_f ln(B)} \qquad ENC_w = \frac{1}{e}\sqrt{k_B C_d T} \quad (7)$$

With:

- e, electron charge, k_B, Boltzmann constant;
- A_f, Flicker noise factor $\frac{K_f}{W_1 L_1 C_{ox}}$;
- B, capacitor ratio, T, temperature;

Fig. 5 shows the layout design submitted to the foundry. Here, The full front-end chain (4 TIAs and a summing amplifier) is implemented in 1 mm^2 of silicon area.

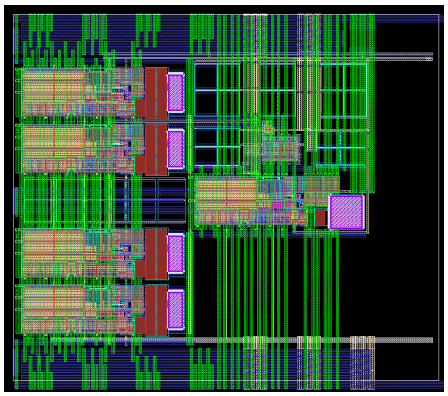

Fig. 5: Layout design submitted to the foundry.

The transient noise simulation is performed with 10 runs of the output signal shown in Fig. 6, and illustrates the effect of the noise superimposed to a single photo-electron signal. Fig. 7 shows the Bode plot with the DC gain and bandwidth of the first stage. The DC gain is 108 $dB_{V/I}$ with a bandwidth of 350 KHz at 77 K.

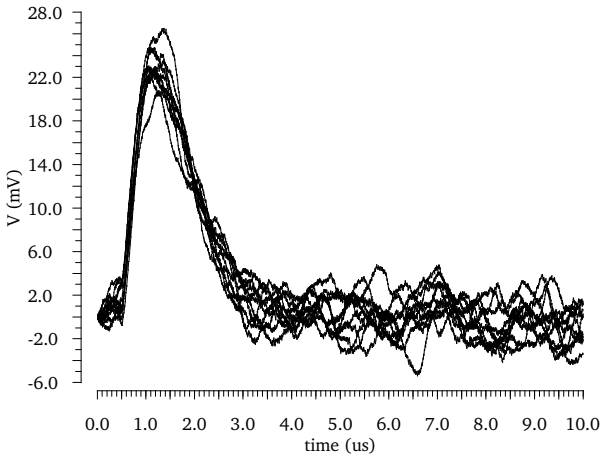

Fig. 6: Transient Noise Signal of the output voltage at 5VoV.

A summary of the electrical parameters from the post-layout netlist for the cryogenic front-end circuit is shown in Table. I. The front-end presents a phase margin of 75° in first stage and 40° in the summing voltage 2 with 1 MΩ of load.

Table. II compares the expected performance of the OTA herein described with similar designs described in recent publications.

A Montecarlo simulation was performed to estimate the stability of the circuit under a statistical variations of the active and passive device process parameters. Fig. 8 and Fig. 9 show the timing jitter and SNR at 77 K for the circuit. The TIA circuit provides a mean SNR = 12.02 with std. dev. = 0.3 and a mean timing Jitter = 42.5 ns with std. dev. = 2.5 ns.

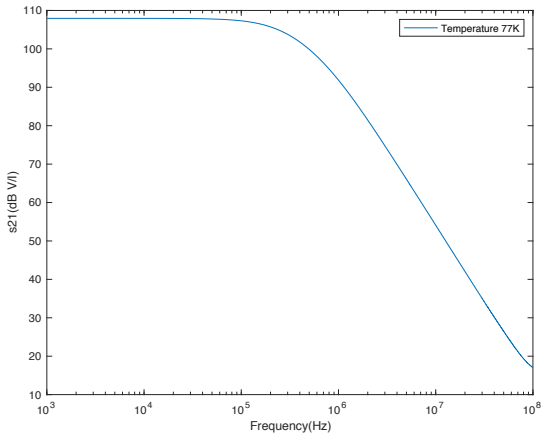

Fig. 7: AC response of the Folded Cascode single-ended.

TABLE I: Parameters and simulation results of 24 cm^2 amplifier

Parameters	Simulation Results
Gm1,m2(mS)	24
Gm21,m22(mS)	18, 25.8
Cm(stage1) (fF)	30
Cm(stage2) (fF)	100
Vout(mV)	23.1
Vnoise(mV)	1.94
Dynamic Range (PEs)	> 40
PM(stage1)	75
PM(stage2)	40

TABLE II: Performance comparison of different Operational Amplifiers

Parameters	[13]	[14]	[15]	[16]	This work
Technology (nm)	130	180	180	180	110
Supply Voltage (V)	1.5	1.8	1.8	1.8	-1.25/1.25
DC Gain (dB)	94.5	65	85.6	90	108
GBW(GHz)	4.75	0.436	0.987	1.44	1.2
BW(MHz)	–	0.25	–	–	0.5
Power (mW)	–			7.34	15

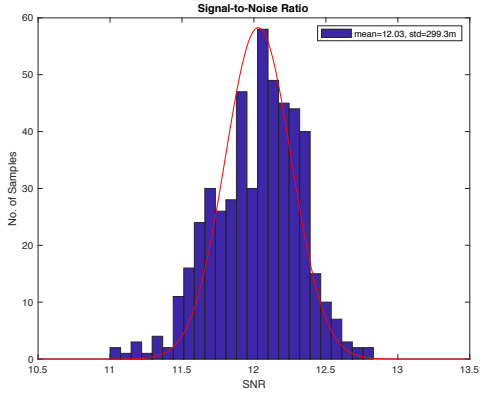

Fig. 8: Montecarlo simulation of Folded Cascode, signal-to-noise ratio.

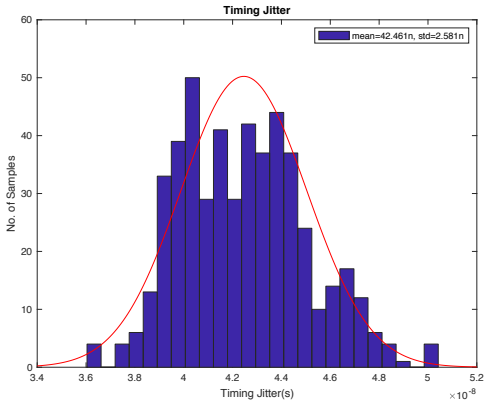

Fig. 9: Montecarlo simulation of Folded Cascode, timing Jitter.

IV. CONCLUSION

This work presents the transistor-level design and post-layout simulation results of a CMOS amplifier for large area SiPM readout at cryogenic temperature. The circuit was designed using the standard CMOS 110 nm technology. This first prototype was sent to fabrication and will be tested with external charge injectors and a 24 cm^2 SiPM tile into a liquid nitrogen bath. Post-layout simulation results show that the circuit should achieve a SNR above 12 and a timing Jitter better than 45 ns for the signal produced by a single photo-electron.

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