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***Abstract*—A mixed-signal ASIC developed to readout silicon photomultipliers (SiPM) at low temperature is presented. The chip is designed in a 110 nm CMOS technology. Both single photon counting and Time-over-Threshold (ToT) operating modes are supported. The ToT modality is useful when many photons pile-up to yield a continuous signal. In single photon counting mode an event rate of up to 5 MHz per channel can be accommodated. The time resolution is 50 ps and the target power consumption is less tha 5 mW per channel. The architecture of a first 32-channel prototype is described. Dedicated test structures to qualify critical building blocks at cryogenic temperature have also been deployed and experimental results will be shown at the conference.**

***Index Terms*—Silicon radiation detectors, Mixed analog digital integrated circuits, Timing, Cryogenic electronics**

I. ASIC ARCHITECTURE

There is a growing interest in the use of Silicon photomultipliers (SiPMs) operating at cryogenic temperatures [1]–[4]. The largely suppressed dark count rate observed at liquid Xenon and liquid Argon temperatures makes such sensors ideally suited to equip large area detectors like those needed in dark matter and neutrino experiments [5]–[8]. Research programs to explore the possibility of building total body PET scanners based on noble liquids readout by SiPM are also ongoing [9] [10]. Highly integrated front-end electronics embedded in the cold volume close to the sensor allows for a significant reduction of the interconnections and feed-through as data can be easily multiplexed and serialised in the digital domain. Depending on the application, the SiPM pixel size may range from a few mm^2 to a few cm^2.

ALCOR (A Low-power Circuit for Optical Readout) is a mixed-signal ASIC optimised for the readout of SiPMs with a wide range of sensor capacitance (pF to nF) at low temperature. The basic unit of the chip is a compact mixed-signal channel (see Fig. 1) that occupies an area of 440×440 μm^2. In each channel, a regulated common-gate input stage acts as the interface between the sensor and the rest of the chain. The biasing of the input stage can be regulated in order to provide an optimal power to performance ratio for a given sensor capacitance. Input capacitance as high as 1 nF can be accommodated. After the input stage, the signal is conditioned by two amplifiers with programmable gain and shaping time. Two leading edge discriminators with configurable threshold generate the trigger CMOS signals (Trg_1 and Trg_2) that are fed to the channel digital control block. A coarse time stamp, derived from a binary 15-bit counter on-channel, is generated at the rising/falling edge of Trg_1/Trg_2, depending on the operation mode. Four low-power time-to-digital converters (TDCs), based on analogue interpolation, generate the fine counter information of 9-bit. The system master clock frequency can be up to 320 MHz. In this condition, the TDCs have a binning of 50 ps and a dead-time of 150 ns. The channel can be configured to operate either in single photon counting or in Time-over-Threshold (ToT) mode. In the first mode, the arrival time of the individual photons is recorded. The TDCs act as four independent derandomizing buffers, allowing to manage an event rate of up to 5 MHz/channel. The minimum time interval between two consecutive pulses is equal to two clock cycles. In the ToT mode the TDC are paired and a two-level buffering is provided. One TDC captures the leading edge of the pulse and the companion TDC measures the trailing edge of the same pulse. The leading edge is always provided by the discriminator connected to the high-gain branch. The trailing edge can be taken either from the same discriminator or from the one connected to the low-gain branch. A time-out mechanism is foreseen in case the trailing edge of the pulse is not detected. The ToT mode is useful when many photons pile-up in the individual SiPM pixel and are treated by the electronics as a single continuous signal. Such a situation is common, for instance, in PET applications. Whenever all four TDCs are in busy state, any new trigger will be discarded and the number of lost events is counted in a dedicated register. The channel generates a 32-bit data payload that includes the time-stamp, the channel, and the specific TDC address. The Data Control block inside the channel handles the payload generation and storage, as well as the data transmission to the chip periphery. Generated payloads are queued and stored in a FIFO register (depth=4), waiting for a write enable from the periphery. In case of FIFO saturation, lost payloads are counted in a second lost-event register. The channel contains also digital to analogue converters that are used to set the discrimination thresholds and the bias currents of the TDCs. The configuration state of each channel is stored into a local 32-bit control registers. The chip periphery contains two static RAMs. The first RAM stores the data received from predefined group of channels. The data belonging to the same time windows identified by the MSB of the coarse counter are

grouped together and a CRC 32-bit code is added. The data are then transferred into the second RAM where they are queued for serialisation and off-chip transmission through LVDS links.

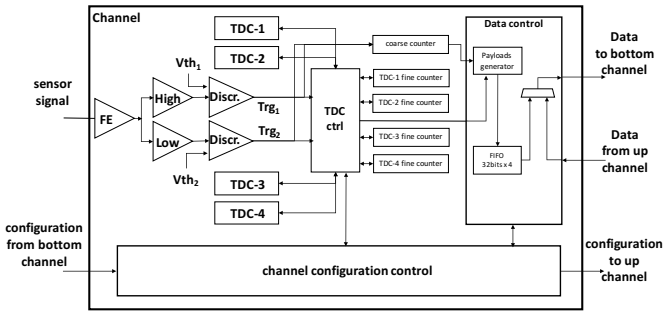

Fig. 1. Channel architecture block diagram.

The channels, being squared, can be naturally organised in a matrix. If the total channel count is low, the interconnection between the chip and the outside world can be realised with standard wire bonding pads located at the chip periphery. For small size chips, a careful layout allows to minimise the parasitic resistance and inductance of the input connection. For larger arrays bump bonding pads should be used. The ASIC in this case is flip-chip mounted on the support PCB. One can also envisage a direct connection between the channel and a corresponding "mini-SiPM" on the sensor. The logic in the channel and in the periphery have been designed in a modular structures. Therefore, starting from the same building blocks one can easily generate ASICs with up to 1024 channels per chip. To test the key design concept in silicon a first 32-channels version with wire bonding pads as shown in Fig. 2 will be submitted to the foundry in fall 2019.

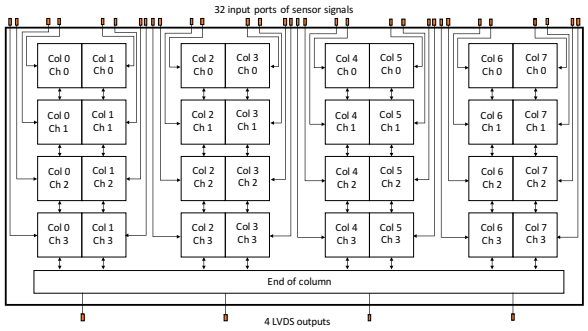

Fig. 2. ALCOR 32-channels architecture block diagram.

II. Test structures

The design of chips working at cryogenic conditions entails several issues. The increased carriers mobility at low temperature may induce an accelerated device ageing. This can be partially mitigated by avoiding minimum length transistors and/or reducing the power supply voltage. Furthermore transistor and digital standard cells are usually not modelled below -40 °C. To gain useful insights in view of the design of the ALCOR chip, dedicated test structures were fabricated. These include a copy of the front-end amplifier, a bandgap reference voltage and LVDS transmitters. To asses the performance of basic digital gates a clock buffer and a synchronisation circuit were also implemented. Fig. 3 shows a picture of the test structure delivered by foundry. The characterisation work is being started. The ALCOR design will be then finalised and optimised using inputs provided by the results obtained on the test structures. At the conference the ALCOR chip architecture will be discussed and experimental results at cryogenic temperature of the building blocks implemented on the test structure will be presented.

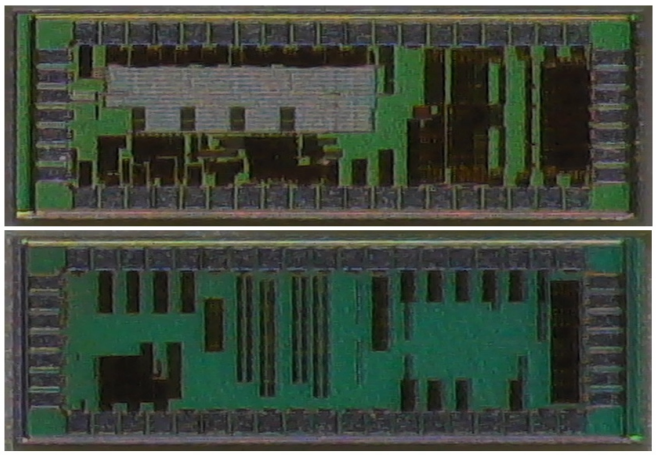

Fig. 3. Two test chips to study critical blocks at cryogenic temperature are fabricated.

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