FPGA Qualification and Failure Rate Estimation Methodology for LHC Environments Using Benchmarks Test Circuits

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A 0.3-1.2V Schottky-Based CMOS ZTC Voltage Reference

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***Abstract*—A voltage reference based on MOSFETs operated under Zero Temperature Coefficient (ZTC) bias is proposed. The circuit operates in a power supply voltage range from 0.3V up to 1.2V and outputs three different reference voltages using Standard-V_T (SVT), Low-V_T (LVT), and Zero-V_T (ZVT) MOS transistors biased near their ZTC point by a single PTAT current reference. Measurements on 15 circuit samples fabricated in a standard 0.13-μm CMOS process show a worst-case normalized standard deviation (σ/μ) of 3% (SVT), 5.1% (LVT) and 10.8% (ZVT) respectively with a 75% of confidence level. At the nominal supply voltage of 0.45 V, the measured effective temperature coefficients (TC_{eff}) range from 140 to 200 ppm/^{o}C over the full commercial temperature range. At room temperature (25^{o}C), line sensitivity in the ZVT VR is just 1.3%/100mV, over the whole supply range. The proposed reference draws around 5 μW and occupies 0.014 mm^2 of silicon area.**

***Index Terms*—low voltage, voltage reference, Schottky diode, zero temperature coefficient (ZTC) condition.**

I. Introduction

In recent years, MOSFET-only voltage references at sub-1V supply have been extensively studied [1] to address the limits of nanoscale technologies and the requirements of low power applications. Most MOSFET-only voltage references have been obtained taking advantage of the thermal drift of the difference in the threshold voltages (V_T) either of two NMOS devices [2–4] or of an NMOS and of a PMOS device [5], or exploiting the V_T dependence on the transistors geometry [6], [7], or even biasing the MOSFET at its Zero Temperature Coefficient (ZTC) operating point [8–11].

Aiming to reconfigurability, which is highly demanded in present-day energy constrained applications [12], ZTC-based references are particularly attractive since, unlike in other solutions, where thermal compensation is achieved at a single, fixed, process-dependent voltage V_{REF}, they can be more easily re-configured to operate at different output voltages without extra circuitry and power overhead. Moreover, ZTC-based references are appealing since a ZTC bias point can be found in UTBB SOI, FinFET devices and advanced MOSFETs technologies as well [13], indicating itself as good strategy for future reference designs.

In this paper, an ZTC-based integrated reference exploiting the approach outlined in [14] is demonstrated on silicon for the first time. Based on the ZTC theoretical modeling aspects reviewed herein, the reconfigurability of the final desired voltage reference by changing the PTAT current generator under the same device is also demonstrated. The measured power consumption of the proposed circuit (5μW) is in the average of other ZTC-based solutions such as [15], [16], and it could be pushed down to the hundred nanowatt range by the approach proposed in [17] at the cost of increased area (using very low aspect ratio (W/L), i.e., very large transistor length).

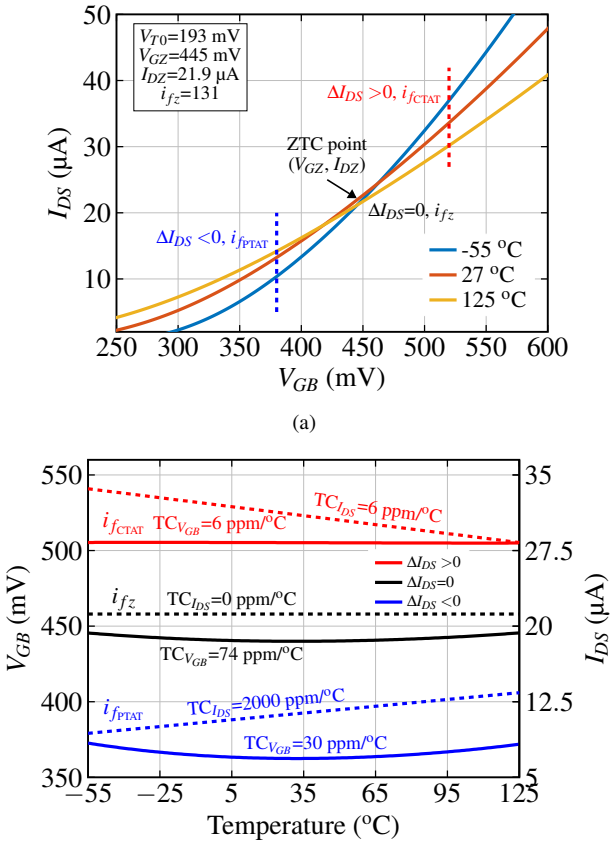

Fig. 1. (a) ZTC condition for a standard NMOS transistor in a 0.13-μm CMOS process. (b) In solid line, $V_{GB}(T, \Delta I_{DS} = I_{DS} - I_{DZ})$ with the right amount of thermal drift $TC_{I_{DS}}$ applied into the MOS transistor. In dashed line, the bias currents with the needed thermal drift $TC_{I_{DS}}$.

II. MOSFET ZTC Condition Review

In a MOSFET, the ZTC condition for the drain current follows from the mutual cancellation of the mobility and threshold voltage dependencies on temperature, which occurs at a particular MOSFET gate-to-bulk voltage bias. The best-known simplified model for this gate-to-bulk voltage at ZTC condition, which was initially proposed by [18] and then deeply explored in [16] and [10], is given by

$$V_{GZ} = V_{T0}(T_0) + nV_{SB} - \alpha_{V_{T0}} T_0 \tag{1}$$

$$J_{DZ} = \frac{I_{DZ}}{(W/L)} = \frac{\mu_n(T_0) T_0^2 C'_{ox}}{2n} \alpha_{V_{T0}}^2 \tag{2}$$

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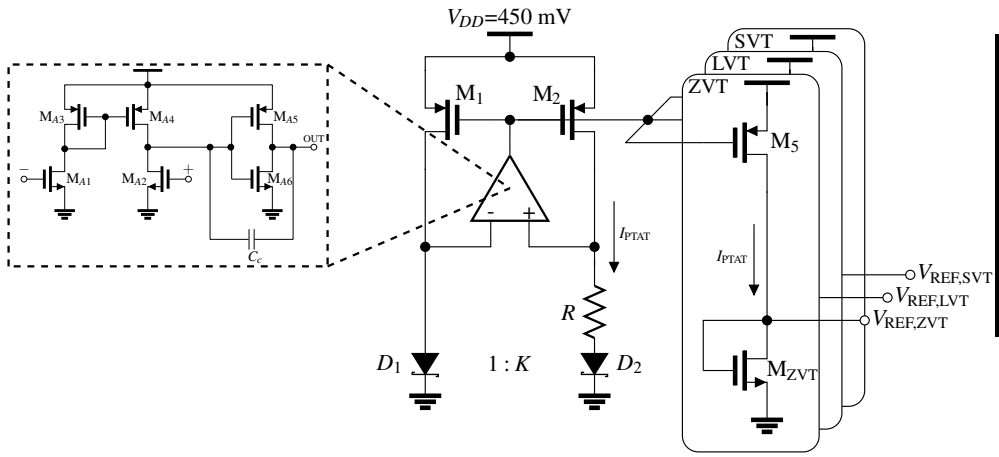

Device	W (μm)	L (μm)
D_1	5	5
D_2 (K=8)	5	5
$M_{1,2,3,4,5}$ (N=8)	16	2
M_{SVT}	3.2	2
M_{LVT}	2.65	2
M_{ZVT}	21.35	2
C_o (N=3)	15	15
$M_{A1,2}$	1	2
$M_{A3,4}$	4	1
M_{A5}	16	2
M_{A6}	4	1
C_c	10	10

N is multiplier number

Fig. 2. Proposed 0.45-V CMOS voltage reference schematic circuit.

where T_0 is the room temperature, $V_{T0}(T_0)$ is the threshold voltage at room temperature, n is the slope factor, V_{SB} is the source-bulk voltage, $\alpha_{V_{T0}}$ is the thermal coefficient of the threshold voltage (stressing that V_T decreases with T), $\mu_n(T_0)$ is the low field mobility at room temperature, C'_{ox} is the oxide capacitance per unit of area and $\frac{W}{L}$ is the transistor aspect ratio. The J_{DZ} can be defined as ZTC normalized drain-current and one can readily conclude that V_{GZ} and J_{DZ} are only dependent on device fabrication processes.

Fig. 1 (a) shows the drain current of a long-channel NMOS transistor in saturation as a function of the gate-bulk voltage (V_{GB}), simulated over temperatures ranging from -55 to 155 °C in standard 0.13-μm CMOS. The ZTC operation point can be seen to be around $V_{GB} \approx 445$ mV for a transistor with V_T = 193 mV and L = 1 μm. From the same Fig. 1 (a), looking at the vertical dotted lines, it can be observed that if the bias point is not exactly at ZTC, the V_{GB} or I_D has a nearly linear PTAT or CTAT behavior depending on its value, which can be expressed by series expansion around V_{GZ} as:

$$V_{GB}(T) = V_{GZ} - \left(\frac{\beta_z \Delta I_D}{I_{SQ}\frac{W}{L}}\right) T \tag{3}$$

where $\Delta I_D = I_D - I_{DZ}$ indicates how far from ZTC operating point the transistor is biased and β_z is defined as the ZTC slope [10], [18].

To eliminate the first order temperature drift close to the ZTC, a drain current I_D with a suitable temperature coefficient TC_{PTAT} should be applied, i.e., it is needed to find out the forward inversion level (i_{f0}) in which, once TC_{PTAT} is applied, the V_{GB} associated to this i_{f0} becomes less sensitive to temperature variations. As detailed in [10], this is equivalent, indeed, to change the reference voltage V_{REF} achieving ZTC condition, as highlighted in (4) and (5), or in other words, to re-configure the same circuit so that to obtain a different, first-order temperature independent, reference voltage V_{REF}.

$$V_{REF} = V_{T0} + n\phi_{t0}\left[\sqrt{1+i_{f0}} - 2 + \log\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{4}$$

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \left[\frac{TC_{PTAT}T_0}{2} - \left(\frac{\alpha_\mu + 2}{2}\right)\right]\left(\frac{i_{f0}}{\sqrt{1+i_{f0}}+1}\right) + \left[\sqrt{1+i_{f0}} - 2 + \log\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{5}$$

where ϕ_{t0} is the thermal voltage at room temperature, k is the Boltzmann constant, q is the elementary electric charge, and i_{f0} is defined as the ZTC forward inversion level for an associated TC_{PTAT}. Note that i_{f0} is related to i_{fPTAT} and i_{fCTAT} in Fig. 1(b) and V_{REF} can be set up based on both parameters, V_{T0} and TC_{PTAT} .

III. Voltage Reference Analysis and Design

The design of a 0.3-1.2V voltage reference based on the approach revised in the previous Section and featuring a Schottky-diode based PTAT current reference for low voltage operation is proposed in the following subsections.

A. Schottky-diode based PTAT Current Reference

To achieve low-voltage operation, a low power PTAT current is generated using the forward voltage difference of two Schottky diodes operated under different current densities by a current mirror. Fig. 2 shows the schematic diagram of the PTAT current reference where a two-stage operational amplifier topology was chosen to increase the loop gain so that to enhance power supply rejection (PSR). The PTAT current analysis is given in [19], and leads to the following well known expression of the thermal drift:

$$I_{PTAT} = I_0(1 + TC_{PTAT}(T - T_0)) \tag{6}$$

where

$$I_0 = \frac{n\phi_{t0}\log(K)}{R_0} \therefore TC_{PTAT} = \frac{1}{T_0\left[1+\alpha_1(T-T_0)\right]^2} \tag{7}$$

R_0 is poly resistance at room temperature, α_1 is its first order temperature dependence and K is ratio area between D_2 and D_1.

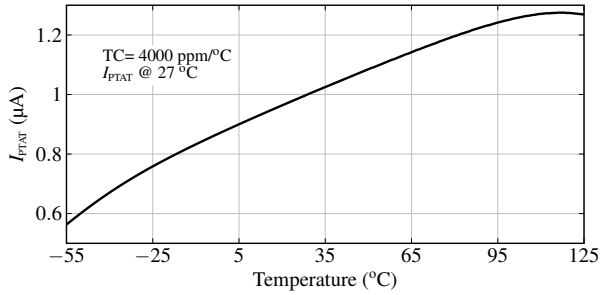

Fig. 3. Simulated PTAT current source temperature dependence.

TABLE I
SIMULATED PERFORMANCE OF THE VOLTAGE REFERENCE

Process	0.13-µm⋆		
Temp. Rage (°C)	-55 ↔ 125		
V_{DD} (V)	0.45 ↔ 1.2		
Transistor Type	SVT	LVT	ZVT
$\overline{V_{REF}}$ † (mV)	312	237	51
V_{REF} µ/σ (%)	5.7	9.7	22.5
LS (V/100mV)	3.55	3.9	1.5
TC_{eff} † (ppm/°C)	214	372	953
PSR @ DC † (dB)	-28	-27.5	-36.8
Power⊕ (µW)	5.9		

⊕@(27 °c, $V_{DD,MIN}$); ⋆ Simulation results; † Process and Mismatch (1000 runs)

B. Circuit Analysis and Design

The complete schematic of the proposed voltage reference is also shown in Fig. 2, and includes a low supply PTAT current reference biasing three diode-connected NMOS transistors operated close to their ZTC bias points. Using this topology it is possible to generate the needed amount of current temperature dependence TC_{PTAT} in order to compensate the first order temperature drift as described by (3) and discussed at Section II. The PTAT current reference by counterbalancing the CTAT behavior of the ZTC vicinity results a first order temperature compensation and provides a voltage reference given by (4) and (5).

The reference voltages are obtained directly from the gate-bulk voltages (V_{GS}=V_{REF}) of M_{SVT}, M_{LVT} and M_{ZVT}. Based on (4)-(6), i.e., after generated the bias current with a defined TC_{PTAT} and found out the i_{f0}, each diode-connected transistor in Fig. 2 can be properly designed and their aspect ratio can be obtained by the procedure reported in [14]. In particular, transistor aspect ratio $\left(\frac{W}{L}\right)$ can be expressed as a function of its inversion level i_f [20] in (8) as:

$$\left(\frac{W}{L}\right) = I_D(T_0)\left(\mu_n(T_0)C'_{ox}n\frac{\phi_{t0}^2}{2}i_{f0}\right)^{-1} \tag{8}$$

which can be simplified as

$$\left(\frac{W}{L}\right) = \frac{2nI_0}{C_{ox}}\left(\frac{TC_{PTAT}}{2|\alpha_{V_{T0}}|} - \frac{\alpha_\mu}{T_0}\right)^2 \tag{9}$$

in strong inversion.

C. Simulation Results

Using a 0.45 V supply voltage, the voltage reference is simulated under the temperature range from -55 to 125 °C in order to predict the following performance parameters: PTAT current (I_{PTAT}) and reference voltages (V_{REF}), effective temperature coefficients (10),

$$TC_{eff} = \frac{V_{REF_{max}} - V_{REF_{min}}}{(T_{max} - T_{min})V_{REF(T_0)}} \tag{10}$$

line sensitivity (11),

$$LS = \frac{V_{REF(V_{DD}=1.8V)} - V_{REF(V_{DD}=0.45V)}}{(1.8V - 0.45V)V_{REF(V_{DD}=0.45V)}} \tag{11}$$

power supply rejection (PSR) and power consumption. The same expressions are used in section IV. Fig. 3 shows the PTAT current reference temperature dependence, which was designed for an 1 μA nominal value at 27 °C and a temperature coefficient TC of 4000 ppm/°C. As can be noted, the PTAT current temperature dependence is not linearly constant for entire temperature range, and decreases at high temperatures, specially above 90 °C. The proposed circuits simulated results are summarized in Table I which will be compared against its measured performances. Each performance metric presented in Table I represents the median value of 1000 Monte Carlo runs.

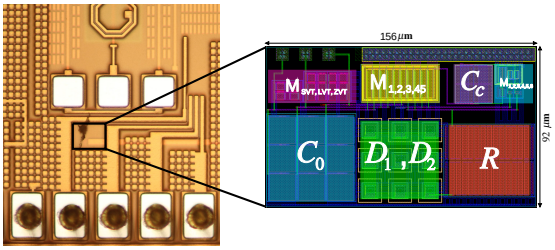

Fig. 4. Micrograph of the proposed 0.45 V voltage reference.

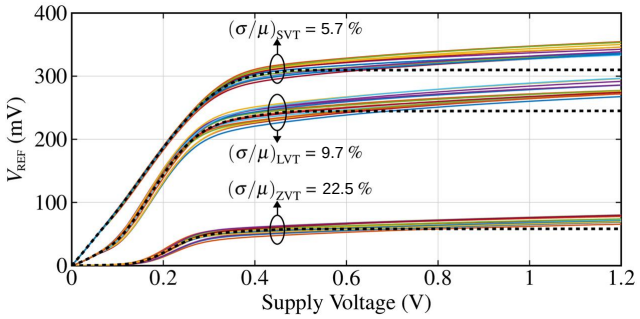

Fig. 5. Supply voltage dependence of 15 measured samples (solid), and typical voltage reference (dashed).

IV. MEASUREMENTS RESULTS

The proposed circuit was designed and fabricated in a standard 0.13-μm CMOS process. Fig. 4 shows the chip photo and its layout, which occupies a total silicon area of 0.014 mm^2. Measurements were performed using a Keysight 4156C Semiconductor Parameter Analyzer for DC sweep, and a Tenney Jr. thermal chamber for temperature control. A total of 15 chips were packaged and measured. Their supply voltage dependence at room temperature is shown in Fig. 5 and proves to be compatible with simulated normalized standard deviation

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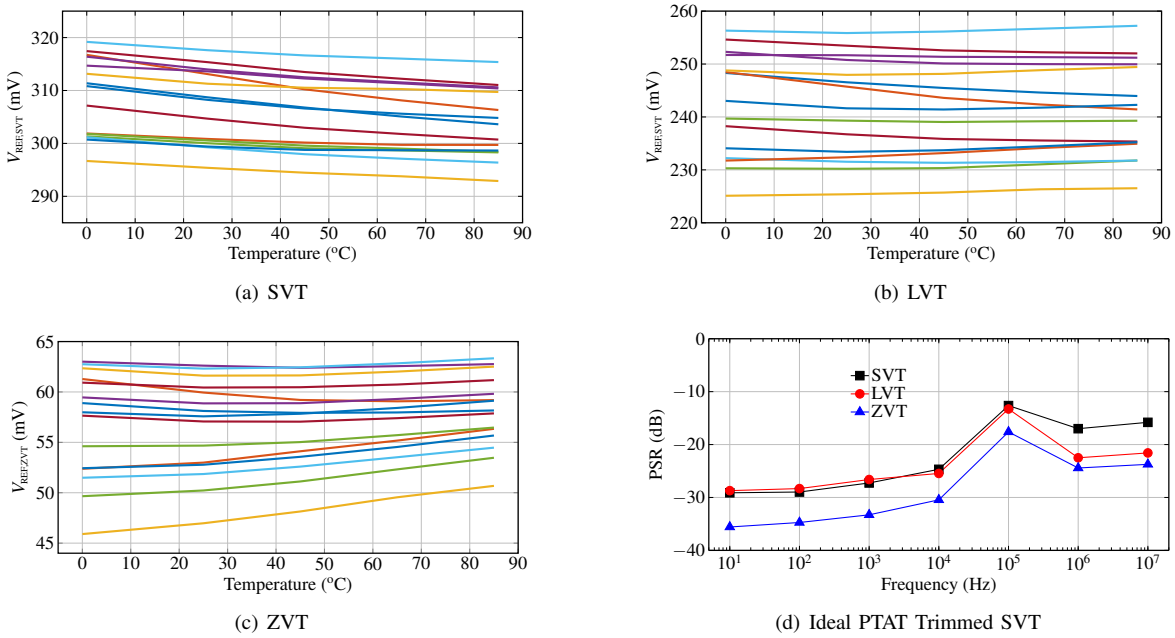
TABLE II
PERFORMANCE COMPARISON BETWEEN THE PROPOSED CIRCUIT AND MICROPOWER SUB-1 V STATE-OF-THE-ART VOLTAGE REFERENCES

Parameter	This Work			[21]st	[22]st	[23]	[24]	[25]	[26]	[27]	[28]
	SVT	**LVT**	**ZVT**								
Process (μm)	**0.13**			0.09	0.5	0.032	0.6	0.5	0.18	0.4	SIMOX
Temp. Rage (°C)	**0 - 85**			5 - 100	5 - 70	0 - 125	0 - 100	-40 - 125	-40 - 140	27 - 125	20 - 80
V_{DD} (V)	**0.3-1.2**			0.5	1.2	0.9	0.98	0.95	0.85	0.84	0.6
V_{REF} (mV)	**306.8**	**241.8**	**56.9**	251	400	545	603	628	500	518	530
LS (%/V)	**13**	**18**	**31.1**	3	1.4	-	3.6	-	4.4	0.1	-
TC (ppm/°C)	**81.5**	**24.2**	**114**	263	107	962	15	17	33	116	37.7
PSR @ 100 Hz (dB)	**-29**	**-28.3**	**-34.7**	-	-	-	-44	-	-	-	-
Power (μW)	**4.12**			450	59.4	12.6	17.6	10	9	4.6	100
Area (mm^2)	**0.014**			0.02	N/A	0.016	0.24	1.09	-	0.1	0.06
FoM (°C^3/W$\times$mm^2)	**3.87**	**6.34**	**3.88**	0.0038	-	0.080	0.158	0.147	-	0.18	0.016

st Schottky-diode-based $^{\oplus}$@(27 °C $V_{DD} = 0.45V$),‡@(27 °C, $V_{DD} = 0.45V$ to $1.2V$) †@($V_{DD} = 0.45V$)



(a) SVT (b) LVT (c) ZVT (d) Ideal PTAT Trimmed SVT

Fig. 6. Measured temperature dependence proposed voltage references @ V_{DD} = 0.45 V of untrimmed (a) SVT, (b) LVT and (c) ZVT. (d) Measured PSR @ V_{DD} = 1.2 V.

(σ/μ) of the reference voltage estimated from 1000 Monte Carlo simulations.

Fig. 6 shows the measured temperature dependence of the three outputs of the proposed voltage reference. To delivery a reasonable estimation of the circuit yield, the statistical benchmarking proposed in [29] is adopted here. Roughly speaking, [29] suggests to include confidence level and interval errors whenever experimental characterization over a limited number of samples is performed. Since only 15 measured samples are considered here, a 75% confidence level is considered in post-measurement statistical analysis. Based on this approach, an output reference voltage (SVT, LVT, ZVT), with a mean value in the interval of μ_{SVT} = (304.6, 309.0) mV and a standard deviation for different samples in the same batch in the interval σ_{SVT} = [5.827,9.101] mV, μ_{LVT} = [238.91, 244.75] mV and σ_{LVT} = [7.845, 12.25] mV, μ_{LVT} = [238.9, 244.7] mV and σ_{LVT} = [7.845, 12.25] mV, μ_{ZVT} = [55.51, 58.37] mV and σ_{ZVT} = [3.83, 5.991] mV, respectively, have been reported.

The power supply voltage rejection (PSR) is shown in Fig 6 (d). Even though presenting a relatively high LS, around 11.9$\sim$33.6 %/V, it could be significantly reduced by regulating its V_{DD} using a sub-0.5 V supply voltage reference.

In Tab.II, the performance of the proposed circuit are compared with other *pn*− and Schottky-diode-based sub-1 V voltage references in the literature. It is worth being observed that the mean and standard deviation of the other references in the table have been calculated in the conventional way. The LS and TC values in Tab.II are the central value of mean interval; similar procedure done for V_{REF}. While the minimum supply voltage for the LVT version is comparable to [21], the ZVT output presented here starts to operate above 0.3V supply. The proposed topology was designed to optimize power consumption, consuming more than 10$\times$ less power than previous Schottky-diode-based implementations (At 0.45V V_{DD}, measured chips consume in average between 3.8 μW at 0^{o}C and 7 μW at 85^{o}C). The *LVT* output shows

a smaller TC. In addition, our reference circuit occupies the lower silicon area. The overall performance of our voltage reference can be evaluated using a Figure of Merit (FoM) [30]:

$$\text{FoM} = \frac{(T_{\text{MAX}} - T_{\text{MIN}})^2}{\text{TC} \times \text{Power} \times \text{Area}} \times \frac{1}{10^{15}} \tag{12}$$

and the proposed circuit presents one of the best FoM performance among others Schottky-diode based, low voltage references considered for comparison.

V. Conclusion

A voltage reference circuit operated under the MOSFET ZTC condition at 0.45 V has been proposed in this paper. The circuit generates three voltage references by biasing three MOS transistors with different threshold (standard-V_T, low-V_T and zero-V_T) under the ZTC condition, sharing the same current reference core. The proposed circuit has been designed in a standard 0.13-μm CMOS process. Based on measurement results on 15 samples, three voltage references ranging from 47.66 up to 317 mV nominal voltages have been obtained, achieving a best measured TC of 73 ppm/°C over the whole 0 to 85 °C temperature range with a power consumption more than 10× less than previous Schottky-based implementations.

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