Low temperature sensitivity CMOS transconductor based on GZTC MOSFET condition

Low Temperature Sensitivity CMOS Transconductor Based on GZTC MOSFET Condition

Pedro Toledo[1], Hamilton Klimach[1,2], David Cordova[1], Sergio Bampi[2], and Eric Fabris[1]

[1]NSCAD Microeletrônica - UFRGS - Porto Alegre, RS, Brazil
[2]PGMicro - UFRGS - Porto Alegre, RS, Brazil
e-mail: eng.pedro.toledo@gmail.com, hamilton.klimach@ufrgs.br, david@nscad.org.br and {bampi,fabris}@inf.ufrgs.br

ABSTRACT

Complementary Metal Oxide Semiconductor (CMOS) Transconductors, or Gm cells, are key building blocks to implement a large variety of analog circuits such as adjustable filters, multipliers, controlled oscillators and amplifiers. Usually temperature stability is a must in such applications, and herein we define all required conditions to design low thermal sensitivity Gm cells by biasing MOSFETs at Transconductance Zero Temperature Condition (GZTC). This special bias condition is analyzed using a MOSFET model which is continuous from weak to strong inversion, and it is proved that this condition always occurs from moderate to strong inversion operation in any CMOS fabrication process. Additionally, a few example circuits are designed using this technique: a single-ended resistor emulator, an impedance inverter, a first order and a second order filter. These circuits have been simulated in a 130 nm CMOS commercial process, resulting in improved thermal stability in the main performance parameters, in the range from 27 to 53 ppm/°C.

Index Terms: CMOS, analog integrated circuits, Low Temperature Sensitivity Transconductors, ZTC Condition.

I. INTRODUCTION

CMOS Transconductors are essential building blocks for analog, mixed-signal and RF designs. They have been used in a large variety of analog/Radio Frequency (RF) circuits, such as filters, multipliers, oscillators, and amplifiers. In the middle of '80s, the use of transconductors in continuous-time monolithic filters has become very attractive for high frequency applications, in contrast to RC filters which are comprised by Operational Amplifiers (OpAmp) instead of Operational Transconductance Amplifiers (OTA) [1]. Also, they have been playing a fundamental role in oscillators, sensing amplifiers and current-mode latch circuits (CML), where they were used in cross-coupled configuration to generate a negative resistance [2]–[4].

Recently, power-management systems for microprocessors and portable devices have increased the demand for CapacitorLess Low Drop-Out (CL-LDO) voltage regulators. CL-LDOs are voltage regulators without off-chip compensation capacitor, which had the advantage of low number of external components and small PCB area, thereby reducing the total system cost. This sort of implementation is usually comprised by 3 or more OTA cells, which are straight-linked to the regulator performances (Phase Margin, Load and Line Transients, Load and Line Regulation and, Power Supply Rejection) [5].

Speaking of RF design, a relevant research effort has been applied in wideband receivers in order to replace multinarrowband front-end solutions, which are usually found in the literature. Among one of the alternatives, it is the use of Low-Noise Transconductance Amplifiers (LNTA), instead of Low-Noise Amplifiers (LNA), which can deliver a satisfactory linearity performance presenting low noise and high bandwidth [6]. Still in the same area but focusing in low power, current reuse receiver architecture has been shown an interesting circuit technique for low power wireless circuit implementation. The LNTA still being the first stage in this approach [7].

In Analog and RF CMOS literature, there have been several proposed topologies for transconductors where the main concerns have been to improve the noise [6], linearity [8], [9] and speed [10]. However, few works attempt to reduce the impact of temperature variation on their performances. Usually, the temperature sensitivity is not considered in these designs and often is not even measured (in some works the tem-

perature sensitivity is implicitly analyzed in the corner PVT simulation). Among those few CMOS RF thermal-care designs, it is the work published in [11], at which the high temperature effects on the LNA gain and on the Partially Depleted Silicon-on-Insulator (PD-SOI) transistors were observed and investigated in order to analyze the LNA behavior versus temperature. This work uses the GZTC condition as bias point but there is no any kind of modeling explaining how the sizing has been made.

Another similar approach was one presented in [12]. This paper has proposed a new technique consisting of a compensation circuit that adapts and generates an appropriate bias voltage for LNAs and mixers so that the variability with temperature and process corners of their main performance metrics (S-parameters, gain, noise figure, etc.) is minimized. In more details, the proposed technique uses conventional gm constant voltage references which can be sized to generate a desired voltage versus temperature and process characteristic that, when applied to the biased circuit, counteracts the effects of process and temperature variations [12].

In CMOS mixed-signal domain, an temperature compensated OTA [13], using the same approach as in [12], has been proposed with a view to generate few low thermal sensitivity applications such as a CMOS readout circuit for wide-temperature range capacitive MEMS sensors [14], a CMOS capacitance to frequency converter for high-temperature MEMS sensors [15], an extreme wide temperature range 8-bit digital to analog converter [16] and a CMOS sigma-delta modulator for wide-temperature applications [17]. However, none of these works have pointed out clearly what was the operation bias point used into their transconductors.

The paper main idea is to present a complete analysis of the MOSFET transconductance zero-temperature condition (GZTC) as well as its application into the transconductor design flow. This special bias condition is analyzed using a MOSFET model which is continuous from weak to strong inversion [18], resulting some general design conditions that can be used with any CMOS process. Powered by all this analysis, this work in a general way concludes with the importance of a dependent temperature bias in order to make transconductor less temperature dependent.

The paper is organized as follows: Section II presents the analysis of the ZTC condition for the MOSFET transconductance, based on a continuous MOSFET model that can predict its behavior from weak to strong inversion. In Section III, the GZTC condition is used in the design of four Gm circuits and their temperature sensitivities are evaluated. Simulation results are shown in Section IV and Section V presents the conclusions.

II. MOSFET ZERO TEMPERATURE COEFFICIENT ANALYSIS

A. MOSFET Bias ZTC Condition

The MOSFET ZTC condition derives from the mutual cancellation of mobility and threshold voltage dependencies on temperature, that happens at a particular transistor gate-to-bulk voltage bias. Which defines a resulting drain current that barely depends on the temperature, as can be seen in Fig. 1(a). The bias ZTC operating point was first defined for design purpose in [19] and later in other publications [20], always based on the quadratic MOSFET model, which is restricted to the strong inversion region. From [20], ZTC operating point is given by Eqs. (1) and (2)

$$V_{GZ}=V_{T0}(T_0)+nV_{SB}-\alpha_{V_{T0}}T_0 \tag{1}$$

$$\frac{I_{DZ}}{\left(\frac{W}{L}\right)}=J_{DZ}=\frac{\mu(T_0)T_0^2C'_{ox}}{2n}\alpha_{V_{T0}}^2 \tag{2}$$

where T_0 is the room temperature, $V_{T0}(_{T0})$ is the threshold voltage at room temperature, n is the slope factor, V_{SB} is the source-bulk voltage, $\alpha_{V_{T0}}$ is the thermal coefficient of the threshold voltage (stressing that V_T decreases with T), $\mu(T_0)$ is the low field mobility at room temperature, C'_{ox} is the oxide capacitance per unit of area and $\left(\frac{W}{L}\right)$ is the transistor aspect ratio. J_{DZ} can be defined as ZTC normalized drain-current and one can readily conclude that V_{GZ} and J_{DZ} are only dependent on device fabrication processes. In addition, there is no body effect in presented ZTC modeling [19].

Fig. 1 (a) shows the drain current (in a log scale) for a saturated long-channel NMOSFET as a function of gate-to-bulk voltage (V_{GB}), simulated under temperatures ranging from -55 to $+125\ ^oC$, for a regular transistor in a commercial 130nm CMOS process. The ZTC operation point can be seen around $V_{GB}\approx 490mV$ for a transistor with $V_T = 160\ mV$, resulting that the ZTC point occurs for an overdrive voltage around 330mV, meaning the transistor operates in strong inversion.

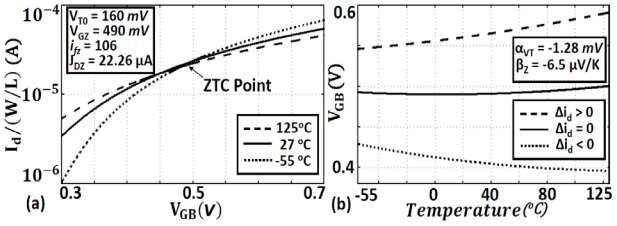

Figure 1. (a) ZTC condition for an NMOS transistor in a 130 nm process, and (b) $V_{GB}(T)$ for $\Delta I_d > 0$, $\Delta I_d = 0$ and $\Delta I_d < 0$.

In a more general analysis we can suppose that the ZTC condition does not only happen in strong inversion [21] [22] and a more complete MOSFET model must be used, such as the one presented in [18], that describes continuously the transistor behavior at any inversion level. From this model, the long channel NMOSFET I-V behavior is modeled by Eqs. (3), (4), (5) and (6).

$$I_D = I_F - I_R = I_S\left(i_f - i_r\right) \tag{3}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SQ}\left(\frac{W}{L}\right) \tag{4}$$

$$V_P - V_{S(D)B} = \phi_t\left[f\left(i_{f(r)}\right)\right] \therefore$$
$$f\left(i_{f(r)}\right) = \sqrt{1 + i_{f(r)}} - 2 + ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{5}$$

$$V_P = \frac{V_{GB} - V_{T0}}{n} \therefore V_{T0} = V_{FB} + 2\phi_F + \Upsilon\sqrt{2\phi_F} \tag{6}$$

where $I_{F(R)}$ is the forward (reverse) current, $i_{f(r)}$ is the forward (reverse) inversion coefficient, I_S is the normalization current, ϕ_t is the thermal voltage, V_P is called the pinchoff voltage, Υ is the body effect coefficient, V_{FB} is the flat band voltage, and ϕ_F is the Fermi potential at the bulk of the semiconductor under the transistor channel. Eqs. (5) and (6) relate the source and drain inversion coefficients (forward and reverse), $i_{f(r)}$, with the external applied voltages, V_{GB}, V_{SB} and V_{DB}, using the bulk terminal as the reference.

The V_{T0} and μ temperature dependence can be approximated by Eqs. (7) and (8), respectively [18].

$$V_{T0}(T) = V_{T0}(T_0) - \left|\alpha_{V_{T0}}\right|(T - T_0) \tag{7}$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{8}$$

$$\left|\frac{\delta V_{T0}}{\delta T}\right|_{T=T_0} = \left|\alpha_{V_{T0}}\right| = \frac{1}{T_0}\left(1 + \frac{\Upsilon}{\sqrt{2\phi_F}}\right)\left(\frac{E_G}{2q} - \phi_F\right) \tag{9}$$

where q is electron charge and E_G is silicon bandgap energy. As shown Eq. (9) and (8), $\alpha_{V_{T0}}$ is the temperature dependence of the threshold voltage, presenting dependencies on the doping concentration (N_a) and on the oxide thickness (t_{ox}), and α_μ is the temperature dependence power coefficient for the mobility. Since the carriers in the inversion layer of transistors undergo several scattering mechanisms, α_μ is negative, and its value depends on the prevalent scattering mechanisms (as Coulombic, phonon, or interface scatterings - all of them interfering on the carrier transport). Related to electron mobility and under room temperature this parameter varies in a range from -1.5 for high doping concentrations to -2.4 for light doping concentrations [23].

If one derives the drain current expression for temperature in the saturation region ($i_r << i_f$), the condition for which its temperature dependence is negligible can be found, i.e., $\partial I_D / \partial T\big|_{T=Tl} = 0$ [22]. Using the Eqs. (3) to (8) and after some analytical work, we can derive that

$$\frac{|\alpha_{VT0}|T}{n\phi_t} = \frac{|\alpha_{VT0}|q}{nk} = \left(\frac{\alpha_\mu + 2}{2}\right)\left(\frac{-i_{fz}}{\sqrt{1+i_{fz}}+1}\right) + \left[\sqrt{1 + i_{fz}} - 2 + \ln\left(\sqrt{1 + i_{fz}} - 1\right)\right] \tag{10}$$

where k is the Boltzmann constant, q is the elementary electric charge, and i_{fz} is defined as the ZTC forward inversion level. Eq. (10) means that when a saturated transistor is biased in this inversion level at the source i_{fz}, the drain current results insensitive to temperature. Now using the assumption $\alpha_\mu \approx -2$ [19] along with Eq. (10) and (5), a simple expression for the ZTC gate-bulk voltage (V_{GZ} - related to i_{fz}) is found

$$V_{GZ} = V_{T0}(T_0) + nV_{SB} - \alpha_{V_{T0}} T_0 \tag{11}$$

Eq. (11) presents the same result already derived from the strong inversion quadratic model in Eq. (1). The ZTC draincurrent, related to i_{fz}, can be found using Eq. (3) under the saturation condition ($i_f >> i_r$),

$$\frac{I_{DZ}}{\left(\frac{W}{L}\right)} = J_{DZ} = I_{SQ}(T_0) i_{fz} \tag{12}$$

Finally, the ZTC vicinity condition can be analyzed using Eqs. (5) and (6), resulting

$$V_{GB}\left(i_f\right) = n\phi_t f\left(i_f\right) + V_{T0}(T) + nV_{SB} \tag{13}$$

Eq. (13) can be expanded in Taylor's series around the ZTC forward inversion level (i_{fz}). Therefore, the first order approximation is given by

$$V_{GB}\left(i_f\right) \approx V_{GZ} + \left.\frac{\delta V_{GB}}{\delta i_f}\right|_{i_f = i_{fz}} \left(i_f - i_{fz}\right) \tag{14}$$

where

$$\frac{\delta V_{GB}}{\delta i_f} = n\phi_t \frac{\delta f\left(i_f\right)}{\delta i_f} = \frac{n\phi_t}{2(\sqrt{1 + i_f} - 1)} \tag{15}$$

Using the approximation $\alpha_\mu \approx -2$ [19], combined with Eq. (14) and (15), and the term $n\phi_t$ extracted from Eq. (10), results

$$V_{GB}(T) \approx V_{GZ} - \frac{\alpha_{VT0}\Delta i_f}{2f(i_{fz})\left(\sqrt{1+i_{fz}}-1\right)}T = V_{GZ} - \beta_z T \quad (16)$$

where $\Delta i_f = i_f - i_{fz}$ indicates how far the transistor is biased from the ZTC operating point and β_z is defined as the ZTC slope. Since $i_f = I_D/I_S$ from the Eq. (3), the $V_{GB}(T)$ dependency on temperature can be be found

$$V_{GB}(T) \approx V_{GZ} - \frac{\beta_z \Delta I_D}{I_{SQ}(T_0)\frac{W}{L}}T \quad (17)$$

Eq. (17) shows that V_{GB} presents a linear temperature dependence in the vicinity of V_{GZ}, and that this dependence can be positive or negative, depending on the ΔI_D chosen, as shown in Fig. 1 (b).

In this ZTC vicinity analysis so far, it was supposed that applied bias current, or $I_D = I_{DZ} + \Delta I_D$, is temperature independent. However, a current with a temperature coefficient (TC_I) can be inserted in transistor drain in order to compensate the Proportional To Absolute Temperature (PTAT) ($\Delta I_D > 0$) or Complementary To Absolute Temperature (CTAT) ($\Delta I_D < 0$) $V_{GB}(T)$ behavior, given by Eq. (17).

Making similar procedure, which has been done for Eq. (10), but now applying a current with temperature dependence given by Eq. (18) in Eq. (3) for saturation regime and differentiating latter with respect to temperature, Eq. (19) is achieved.

$$I_D(T) = (I_{DZ} + \Delta I_D)(1 + TC_I(T - T_0)) = I_{D0}(1 + TC_I(T - T_0)) \quad (18)$$

$$\frac{\delta}{\delta T}(I_S i_f)\Big|_{T=T_0} = I_S \frac{\delta i_f}{\delta T}\Big|_{T=T_0} + i_f \frac{\delta I_S}{\delta T}\Big|_{T=T_0} = I_{D0} TC_I \quad (19)$$

Where $\frac{\delta I_S}{\delta T}$ is given by Eq. (20) and $\frac{\delta I_S}{\delta T}$ is given by Eq. (21) [22].

$$\frac{\delta i_f}{\delta T} = 2\left(\sqrt{1+i_f}+1\right)\left(\frac{|\alpha_{VT0}|}{n\phi_t} - \frac{1}{T}\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right)\right) \quad (20)$$

And

$$\frac{\delta I_S}{\delta T} = I_S\left(\frac{\alpha_\mu + 2}{T}\right) \quad (21)$$

Now, using Eqs. (21) and (20) in (19) and after some algebra effort, we get

$$\frac{|\alpha_{VT0}|q}{nk} = \left(\frac{TC_I T_0}{2} - \frac{\alpha_\mu + 2}{2}\right)\left(\frac{i_{f0}}{\sqrt{1+i_{f0}}+1}\right) + \left[\sqrt{1+i_{f0}} - 2 + \ln\left(\sqrt{1+i_{f0}}-1\right)\right] \quad (22)$$

where i_{f0} is the inversion level related to I_{D0} under room temperature. Eq. (22) opens up scope for an interesting interpretation. For instance, $TC_I = 0$ leads to Eq. (22) to be the same as Eq. (10) such that i_{f0} becomes i_{fz}. Therefore, it is reasonable to claim that applying a drain current with $TC_I \neq 0$ is equivalent to moving the ZTC forward inversion level to another value, i.e., i_{fz} to i_{f0}.

Fig 2 (a) shows simulations data for a diode-connected NMOS transistor with (W/L = 2.5μm/1μm) in a commercial 180 nm CMOS technology. It is visible that five different bias current are applied: 5, 20, 26.25, 35, 50 μA, yielding distinct V_{GB} temperature dependence. These applied currents are temperature independent, i.e., $TC_I = 0$. In this picture, for $I_{D0} =$ 26.25μA is equivalent to say that NMOS is working on bias ZTC point. For I_{D0} with 5μA, 20μA and with 35μA, 50μA, the NMOS transistor is working on ZTC vicinity at CTAT and PTAT regime, respectively. This is in close agreement with Eq. (17).

On the other hand, if a current with a $TC_I \neq 0$ is applied, there is a specific inversion level value, or i_{f0}, where it is maintained constant regarding the temperature variations, more specifically around T_0 . Fig 2 (b), which shows V_{GB} versus temperature enforcing right TC_I that cancels PTAT or CTAT behavior, summarizes previous explained reasoning. In more details, Fig. 2 (c)(d) and Fig. 3 (a)(b) show V_{GB} temperature dependence being canceled for each applied I_{D0} with their suitable TC_I values. By contrast in Fig. 3 (c), this case does not needs a TC_I, or $TC_I = 0$, since it is on ZTC bias point.

Fig. 3 (d) shows the calculated Effective Temperature Coefficient (TC_{eff}) related to V_{GB} for each case, at which necessary TC_I to cancel temperature dependence has been already applied. TC_{eff} is given by Eq. (23) for X = V_{GB}. According to Fig. 3 (d), even if a suitable value for TC_I is chosen, the V_{GB} thermal stability will be worse than if it was biased exactly over ZTC point. In addition to other secondary effects, this deterioration in thermal stability is easily explained by noting that Eq. (22) has a non-zero second derivative with respect to temperature. It does not occur in the case where the MOS transistor is biased exactly over the ZTC point, as demonstrated in Eq. (10).

$$TC_{eff|X} = \frac{X_{MAX} - X_{MIN}}{X(T_0)(T_{MAX} - T_{MIN})} \quad (23)$$

where X is the desired parameter to be evaluated.

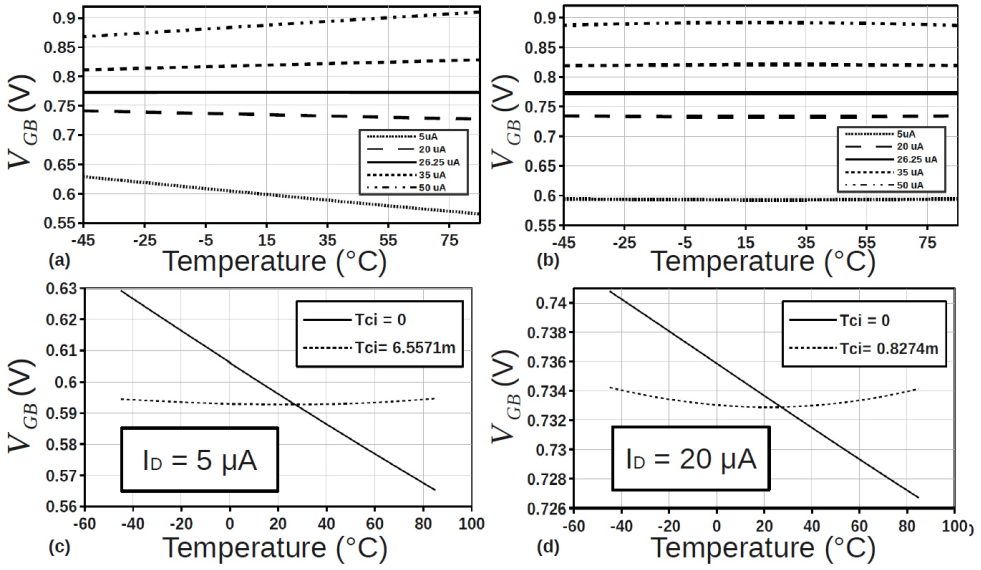

Figure 2. (a) simulations data for a diode-connected NMOS transistor (W/L = 2.5µm/1µm) in 180 nm CMOS technology with five different bias current (5, 20, 26.25, 35, 50 µA), yielding distinct V_{GB} temperature dependence. (b) V_{GB} versus temperature enforcing right TC_I that cancels PTAT or CTAT behavior. (c) Zoom for I_D = 5µA. (d) Zoom for I_D = 20µA.

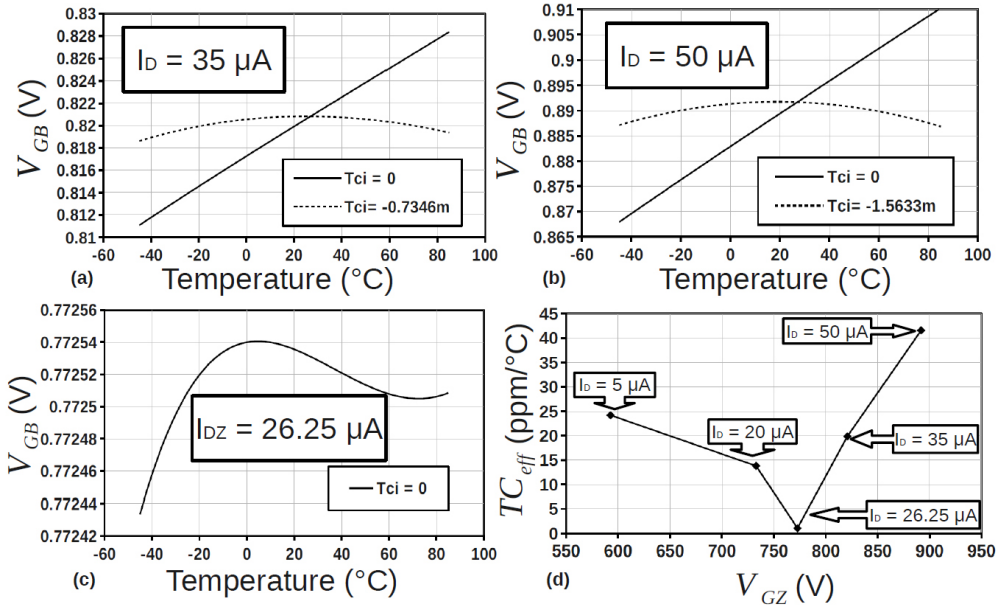

Figure 3. (a) Zoom for I_D = 35µA. (b) Zoom for I_D = 50µA. (c) Zoom for I_D = 26.25µA. (d) TC_{eff} for each vicinity condition.

B. MOSFET Transconductance ZTC Condition

As done in the last section for the bias operation point, a similar analysis can be developed for the MOSFET gate transconductance (g_{mg}) to define a bias condition where g_{mg} does not change with temperature variations, or presents a low dependence. Here, this condition is called Transconductance Zero Temperature Coefficient, or GZTC, and its definition is important since in any analog signal processing block the gain is fundamentally determined by the transistors transconductance, resulting that the gain is sensitive to temperature variations in most designs. If the design is developed with GZTC point in mind, the gain results less sensitive to temperature.

Similarly to the last section, an inversion level (i_{fgz}) where the transconductance presents low temperature dependence can be found. From [18], the small signal transconductance is related to the forward inversion level as follows

$$g_{mg} = \frac{g_{ms}}{n} = \frac{2I_S}{n\phi_t}\left(\sqrt{1+i_f}-1\right) \tag{24}$$

where g_{mg} and g_{ms} are gate-bulk and source-bulk transconductances, respectively.

Applying the condition $\partial g_{mg}/\partial T\big|_{T=Tl} = 0$ in Eq. (24),

$$\frac{\partial g_{mg}}{\partial \mathrm{T}} = \left(\frac{2}{n}\right)\frac{\partial}{\partial \mathrm{T}}\left(\frac{I_S}{\phi_t}\sqrt{1+i_f}-1\right) = 0 \tag{25}$$

Replacing I_S, or Eq. (4), in Eq (25)

$$\frac{\partial g_{mg}}{\partial \mathrm{T}} = C'_{OX}\left(\frac{W}{L}\right)\frac{\partial}{\partial \mathrm{T}}\left(\mu(T)\phi_t(T)\left(\sqrt{1+i_f}-1\right)\right) \tag{26}$$

Or,

$$\frac{\partial g_{mg}}{\partial \mathrm{T}} = C'_{OX}\left(\frac{W}{L}\right)\left[\frac{\partial}{\partial \mathrm{T}}\left(\mu(T)\phi_t(T)\right)\left(\sqrt{1+i_f}-1\right) + \mu(T)\phi_t(T)\frac{\partial}{\partial \mathrm{T}}\left(\sqrt{1+i_f}-1\right)\right] \tag{27}$$

The term $\frac{\partial}{\partial \mathrm{T}}(\mu(T)\phi_t(T))$ can be found using $\frac{\partial \mu}{\partial \mathrm{T}} = \frac{\mu\alpha_\mu}{\mathrm{T}}$ and $\frac{\partial \varphi_t}{\partial \mathrm{T}} = \frac{\varphi_t}{\mathrm{T}}$ from [22],

$$\frac{\partial}{\partial \mathrm{T}}\left(\sqrt{1+i_f}-1\right) \tag{28}$$

On the other hand, the term $\frac{\partial}{\partial \mathrm{T}}\left(\sqrt{1+i_f}-1\right)$ is given by

$$\frac{\partial}{\partial \mathrm{T}}\left(\sqrt{1+i_f}-1\right) = \left(\frac{1}{2\sqrt{1+i_f}}\right)\frac{\partial i_f}{\partial \mathrm{T}} \tag{29}$$

Substituting Eqs. (20) and (28) in (27) and after some algebra, we get

$$0 = \alpha_\mu\left(\sqrt{1+i_{fgz}}-1\right) - 2 + \frac{\sqrt{1+i_{fgz}}+1}{\sqrt{1+i_{fgz}}}\left(\frac{|\alpha_{VT0}|q}{nk} + 2 - \ln\left(\sqrt{1+i_{fgz}}-1\right)\right) \tag{30}$$

which defines the GZTC condition. The i_{fgz} is defined as GZTC forward inversion level.

One can note that, as in the case of the bias current I_D, the condition GZTC derives from the mutual cancellation of the mobility and threshold voltage dependencies on temperature, which happens for a particular bias condition, $V_{GB}(i_{fgz}) = V_{GGZ}$.

Fig. 4 (a) shows the ZTC forward inversion level surface (ZTCS) and the GZTC forward inversion level surface (GZTCS), i.e., all possible solutions of Eq. (10) and Eq. (30) as a function of α_μ and α_{VT0}. This solution shows that the minimum ZTC and GZTC forward inversion levels are different, resulting around 15.6 and 9.1 for the values $\alpha_\mu = -2.5$ and $\alpha_{VT0} = -0.5$ $mV/°C$. Since the inversion level $i_f = 3$ defines the condition where $V_{GB} = V_{T0}$ from Eqs. (5) and (6), one can readily conclude that both ZTC conditions always occur for gate-bulk voltages larger than the threshold voltage, in moderate or strong inversion.

To see how far each ZTC bias point is from the threshold voltage (the overdrive voltage for ZTC and GZTC bias point), for $V_S = 0$, i_{fz} and i_{fgz} can be directly applied in Eq. (5) and (6),

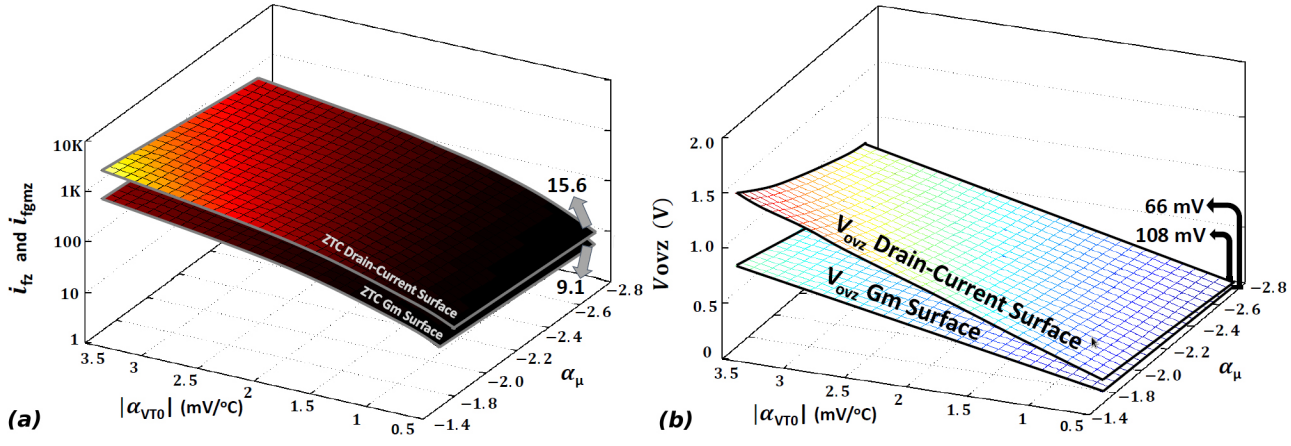

Figure 4. (a) ZTC forward inversion level surface (ZTCS) and GZTC forward inversion level surface (GZTCS) (b) overdrive voltage for the ZTC (V_{OVZ}) and GZTC bias point (VOVGZ) as a function of the values for α_μ and α_{VT0}.

$$V_{GZ(GZ)} - V_{T0} = V_{OVZ(GZ)} = n\phi_t f\left(i_{fz(gz)}\right) \quad (31)$$

where

$$f(i_f) = \sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right) \quad (32)$$

V_{OVZ} and V_{OVGZ} are defined as the ZTC and GZTC overdrive voltages, respectively. Fig. 4 (b) shows all possible overdrive voltages for any α_μ and α_{VT0} combination in the same range that was used in Fig. 4 (a). Taking as reference the threshold voltage at room temperature, the minimum V_{OVZ} and V_{OVGZ} found are around 108mV and 66mV respectively meaning that both ZTC bias points are always in the moderate or strong inversion regime. Another conclusion is that ZTC will be always above the GZTC bias point, i.e., GZTC is working in ZTC vicinity with a CTAT behavior (Fig. 1 (b)), as can be also seen in Fig. 5 for a PMOS transistor in the same 130 nm technology.

Finally, it is evaluated necessary TC_I to equalize $i_{f0} = i_{fgz}$, i.e., to maintain i_{fgz} stable over temperature variations in such manner that the transconductance (g_{mg}) becomes temperature independent. It is worth to note that this whole analysis is valid only when the transconductor biasing is done by current. In contrast, if the bias is realized directly on the gate-to-bulk voltage with a voltage reference, the GZTC condition can be already considered thermally stabilized.

Therefore, finding i_{fgz} from Eq. (30) for each $|\alpha_{VT0}|$ and α_μ and then putting in Eq. (22), the needed temperature coefficient, or TC_{IGZ}, to make the transconductance unvarying with temperature can be found, as shown Fig. 6. Unlike of previous results, α_μ has more impact than $|\alpha_{VT0}|$ in TC_{IGZ}. Values between 3000 and 9500 ppm/°C have been calculated, which comply with CMOS PTAT current reference found in literature, where TCI between 1000 and 10000 ppm/°C are readily achieved [24].

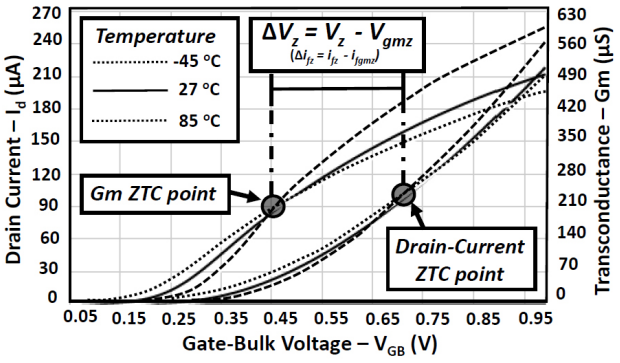

Figure 5. ZTC and GZTC condition for a PMOS transistor in a 130 nm process with V_{T0} = 250 mV.

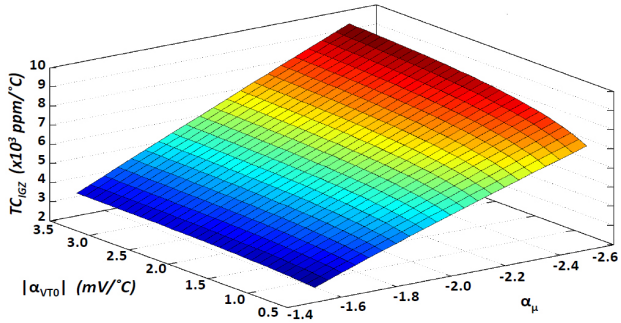

Figure 6. Fig. 6. Necessary TC_I, or TC_{IGZ}, to keep the MOSFET transconductance temperature independent in function of $|\alpha_{VT0}|$ and α_μ.

III. GM TOPOLOGIES BIASED IN GZTC CONDITION

In this section, some of basic Gm topologies [1] are designed to operate in GZTC condition and their main performances are analyzed.

A. Gm Topologies

Fig. 7 shows a single-ended resistor emulator, an impedance converter (gyrator), a first order filter and a second order filter. The main parameters of these four topologies are strongly dependent on transistors transconductance. Eqs. (33) and (34) give the input

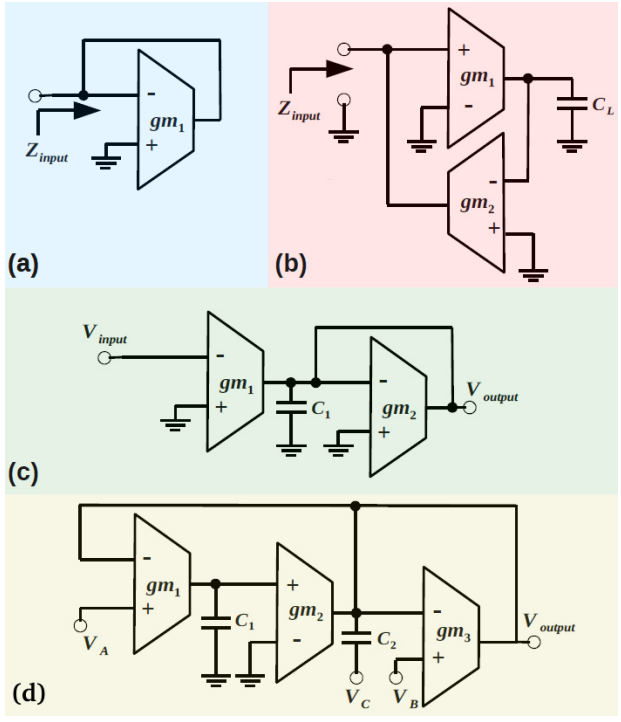

Figure 7. (a) single-ended resistor emulator (b) impedance inverter (c) first order filter (d) second order filter.

impedance of single-ended resistor emulator and impedance converter, respectively.

$$Z_{in} = \frac{1}{gm_1} \tag{33}$$

$$Z_{in}(s) = \frac{sC_L}{gm_1 gm_2} \tag{34}$$

Also the low frequency gain and dominant pole frequency of first order filter are defined by transconductance parameters as indicated in Eq. (35).

$$\frac{V_{output}(s)}{V_{input}(s)} = \frac{gm_1}{gm_2 + sC_1} \tag{35}$$

Finally the low pass (V_A), band pass (V_B) and high pass terms (V_C) of second order filter comply with Eq. (36) to (38), where the transconductance of three blocks directly affect their performance.

$$\frac{V_{output}(s)}{V_{input}(s)} = \frac{(C_1C_2)s^2V_C + (gm_3C_1)sV_B + gm_2gm_1V_A}{(C_1C_2)s^2 + (gm_3C_1)s + gm_2gm_1} \tag{36}$$

$$w_0 = \sqrt{\frac{gm_1gm_2}{C_1C_2}} \tag{37}$$

$$Q = \frac{1}{gm_3}\sqrt{\frac{gm_1gm_2C_2}{C_1}} \tag{38}$$

B. Circuit Analysis and Design

Fig. 8 shows the transconductor schematic that was used within each Gm cell. It was chosen a PMOS differential pair with active load for this proof-of-concept, as a demonstration that it is possible to design a temperature aware transconductor. Even more, the principles here described can be adopted in other transconductor circuits. This classical topology is composed by a biasing current mirror $M_{3A(B)}$, a transconductance differential stage $M_{1A(B)}$ and, an active mirror load $M_{2A(B)}$ [25].

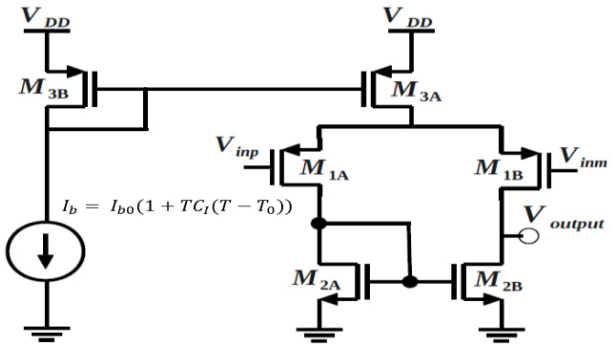

Figure 8. PMOS differential pair with active load.

Considering a fixed bias current (I_{DGZ}), the $M_{1A(B)}$ aspect ratio (W/L) must be defined so that its inversion level is i_{fgz} and then it is necessary to ensure that the GZTC bias condition remains stable over temperature. Using Eq. (3), the $M_{1A(B)}$ aspect ratio (W/L) is given by

$$\left(\frac{W}{L}\right) = \frac{I_{DGZ}}{i_{fgz}\mu C'_{OX} n \frac{\varphi_t}{2}} \tag{39}$$

where i_{fgz} is found by

$$0 = \alpha_\mu\left(\sqrt{1 + i_{fgz}} - 1\right) - 2 + \frac{\sqrt{1+i_{fgz}}+1}{\sqrt{1 + i_{fgz}}}\left(\frac{|\alpha_{VT0}|q}{nk} + 2 - \ln\left(\sqrt{1+i_{fgz}} - 1\right)\right) \tag{40}$$

As this condition is always located in ZTC bias vicinity (below the bias ZTC point), it is necessary to cancel its CTAT bias behavior by applying a small amount of PTAT bias current, as shown in Fig. 5 and described by Eq. (41).

$$I_B(T) = (I_{DGZ})(1 + TC_I(T - T_0)) \tag{41}$$

The requested Current Bias Temperature Coefficient (TC_I) can be found simply using Eq. (22), repeated below as a matter of convenience, with i_{fgz} that was already found in Eq. (40).

$$\frac{|\alpha_{VT0}|q}{nk} = \left(\frac{TC_IT_0}{2} - \frac{\alpha_\mu + 2}{2}\right)\left(\frac{i_{fgz}}{\sqrt{1+i_{fgz}}+1}\right) + \left[\sqrt{1+i_{fgz}} - 2 + \ln\left(\sqrt{1+i_{fgz}} - 1\right)\right] \tag{42}$$

Combination of Eq. (39) with Eq. (42) means that if $M_{1A(B)}$ are biased in GZTC condition along with right amount of PTAT current defined by TC_I coefficient, the transconductance of differential pair will present very low temperature sensitivity.

Some technologies present the GZTC condition operating in strong inversion regime. For these cases, a more simple expression, Eq. (43), can be used for a bias current temperature dependence estimation. Eq. (43) is derived from Eq. (42) by neglecting the logarithm term.

$$TC_I = 2|\alpha_{VT0}|\sqrt{\frac{W}{L}\frac{C'_{OX}}{2nI_{DGZ1}}} + \frac{\alpha_\mu}{T_0} \tag{43}$$

I. GM TOPOLOGIES BIASED IN GZTC CONDITION

The application circuits presented here have been designed and simulated in a 130 nm CMOS commercial process in schematic level only, since parasitic would mainly degrade frequency response.

The calculated bias current is 4 μA for each transcondutor, with a TC_I around 3000 ppm/ºC. The capacitors $C_L = C_1 = 10$ pF were used in the impedance converter and in the first order filter. The capacitors $C_1 = C_2 = 15$ pF were used in the second order filter.

Fig. 9 (a) presents the input impedance frequency response of the single-ended resistor emulator. When the curves are zoomed one can note that the equivalent resistance presents low temperature sensitivity. Fig. 9 (b) shows equivalent resistance ($1/g_m$) versus temperature, confirming a low sensitivity to temperature variations (continuous line), i.e., the equivalent resistance temperature coefficient is $TC_{eff} = 34$ ppm/°C under a supply voltage $V_{DD} = 1.2$ V. The resulting coefficient is comparable to TCs obtained in some CMOS voltage and current reference circuits found in the literature [26] [20].

On the other hand, if it is not applied the right amount of PTAT current the equivalent resistance will be more susceptible to temperature variations, as also shown (dashed line) in Fig. 9 (b) resulting a $TC'_{eff} = 1568$ ppm/ºC. The apostrophe on TC_{eff} means that this estimation was not done putting required TC_I in the transconductor in order to make it temperature independent.

The impedance converter also presented a good thermal immunity, resulting a $TC_{eff} = 52.5$ ppm/°C ($TC'_{eff} = 3300$ ppm/°C), as can be seen in Fig. 10 (a). Regarding the filters, a TC_{eff} of 44.5 ppm/°C ($TC'_{eff} = 1495$ ppm/°C) for the dominant pole (Fig. 10 (b)) and a TC_{eff} of 27 ppm/°C ($TC'_{eff} = 970$ ppm/°C) for the quality factor (Fig. 10 (c)) were obtained from the simulations of first order and second order filters, respectively.

To predict vulnerability to manufacturing process variations (average process variations + mismatch), 1000 simulations samples under a temperature range of -45 to 85°C (-45,-15, 27, 55 and 85 °C) were performed for the first order filter. Both cases were accomplished: $TC_I = 0$ and $TC_I = 3000$ ppm/°C. Fig. 11 shows that biasing the trasnconductor at GZTC point along with suitable current temperature coefficient (TC_I) the average process variation (μ) of dominant pole holds constant regarding the temperature. Note that standard deviation (σ) around μ has negligible changes over entire temperature range since it is only dependent of manufacturing process variations [27].

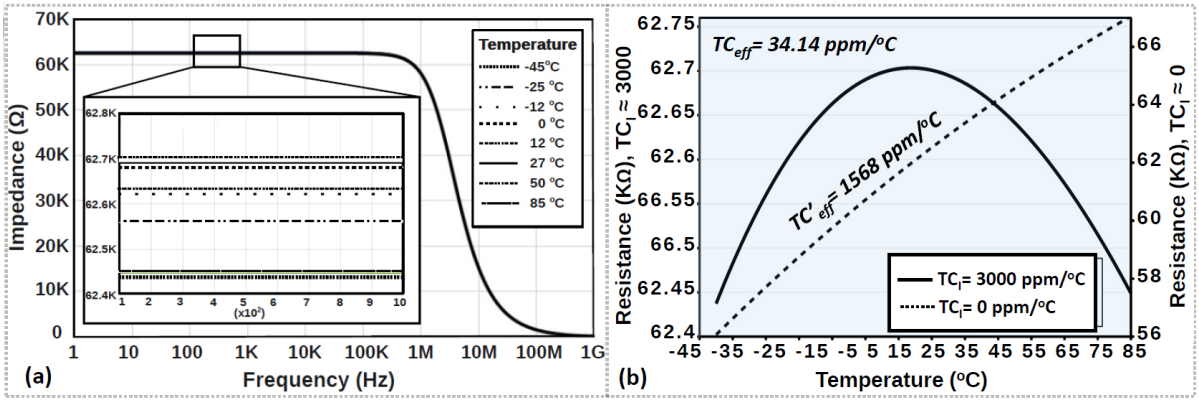

Figure 9. (a) Input impedance of single-ended resistor emulator (b) Equivalent Resistance vs. Temperature. Effective Temperature Coefficient is given by $TC_{eff} = \frac{max}{(T_{max}-T_{min})} \frac{REF_{min}}{R_{REF(T_0)}} R_{REF}-R$

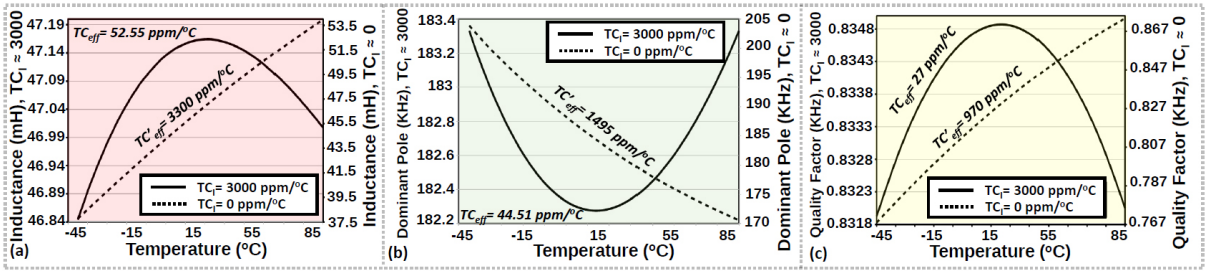

Figure 10. (a) Equivalent Inductance vs. Temperature (b) Dominant Pole vs. Temperature (c) Quality Factor vs. Temperature.

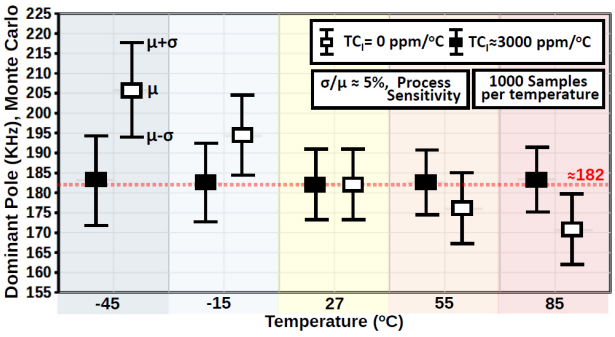

Figure 11. Dominant pole Monte Carlo simulations for a temperature range of -45 to 85*ºC*. For each temperature (-45,-15, 27, 55 and 85 *ºC*), 1000 samples were performed.

IV. CONCLUSIONS

A new analytical approach for the MOS transistor transconductance zero-temperature coefficient (GZTC) was presented using an all-region MOSFET model, since this effect occurs from moderate to strong inversion regions. This analysis was compared with the well-known bias ZTC MOSFET condition and it was shown that both effects are technology dependent. Also some example circuits were presented and designed using the GZTC technique (a single-ended resistor emulator, an impedance converter, a first order and a second order filter) in a 130 nm CMOS commercial process, presenting improved stability with temperature in their main performance parameters, from 27 ppm/˚C to 53 ppm/˚C.

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REFERENCES

[1] R. Geiger and E. Sanchez-Sinencio, “Active filter design using operational transconductance amplifiers: A tutorial,” *Circuits and Devices Magazine, IEEE*, vol. 1, no. 2, pp. 20–32, March 1985.

[2] B. Razavi, “The cross-coupled pair - part i [a circuit for all seasons],” *Solid-State Circuits Magazine, IEEE*, vol. 6, no. 3, pp. 7–10, Summer 2014.

[3] ——, “The cross-coupled pair - part ii [a circuit for all seasons],” *SolidState Circuits Magazine, IEEE*, vol. 6, no. 4, pp. 9–12, Fall 2014.

[4] ——, “The cross-coupled pair?part iii [a circuit for all seasons],” *SolidState Circuits Magazine, IEEE*, vol. 7, no. 1, pp. 10–13, winter 2015.

[5] J. Torres, M. El-Nozahi, A. Amer, S. Gopalraju, R. Abdullah, K. Entesari, and E. Sanchez-Sinencio, “Low drop-out voltage regulators: Capacitor-less architecture comparison,” *Circuits and Systems Magazine, IEEE*, vol. 14, no. 2, pp. 6–26, Secondquarter 2014.

[6] H. Geddada, C.-T. Fu, J. Silva-Martinez, and S. Taylor, “Wide-band inductorless low-noise transconductance amplifiers with high largesignal linearity,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 62, no. 7, pp. 1495–1505, July 2014.

[7] A. Burdett, “Ultra-low-power wireless systems: Energy-efficient radios for the internet of things,” *Solid-State Circuits Magazine, IEEE*, vol. 7, no. 2, pp. 18–28, Spring 2015.

[8] Y. Tsividis, Z. Czarnul, and S. Fang, “Mos transconductors and integrators with high linearity,” *Electronics Letters*, vol. 22, no. 5, pp. 245–246, February 1986.

[9] S. Koziel and S. Szczepanski, “Design of highly linear tunable cmos ota for continuous-time filters,” *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 49, no. 2, pp. 110–122, Feb 2002.

[10] A. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. Carvajal, “Lowvoltage super class ab cmos ota cells with very high slew rate and power efficiency,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 5, pp. 1068–1077, May 2005.

[11] M. El Kaamouchi, M. Moussa, J. Raskin, and D. Vanhoenacker-Janvier, “Zero-temperature-coefficient biasing point of 2.4-ghz lna in pd soi cmos technology,” in *Microwave Conference, 2007. European*, Oct 2007, pp. 1101–1104.

[12] D. Gomez, M. Sroka, and J. L. G. Jimenez, “Process and Temperature Compensation for RF Low-Noise Amplifiers and Mixers,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1204–1211, jun 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5356236

[13] Y. Wang and V. P. Chodavarapu, “High-temperature general purpose operational amplifier in IBM 0.13 µm CMOS process,” in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*. IEEE, jun 2014, pp. 1–2. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7061279

[14] ——, “Design of a CMOS readout circuit for widetemperature range capacitive MEMS sensors,” in *Fifteenth International Symposium on Quality Electronic Design*, vol. 9. IEEE, mar 2014, pp. 738–742. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6783400

[15] ——, “Design of CMOS capacitance to frequency converter for high-temperature MEMS sensors,” in *2013 IEEE SENSORS*. IEEE, nov 2013, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6688275 [16] K. S. Greig and V. P. Chodavarapu, “Extreme wide-temperature range 8-bit digital to analog converter in bulk CMOS process,” in *2014 IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE)*, no. 2. IEEE, may 2014, pp. 1–5. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6901016

[17] Y. Wang and V. P. Chodavarapu, “Design of a sigma-delta modulator in standard CMOS process for wide-temperature applications,” in *Sixteenth International Symposium on Quality Electronic Design*. IEEE, mar 2015, pp. 107–111. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7085408

[18] C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using AllRegion MOSFET Modeling*, 1st ed. Cambridge University Press, 2010.

[19] I. Filanovsky and A. Allam, “”mutual compensation of mobility and threshold voltage temperature effects with applications in cmos circuits”,” *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, no. 7, pp. 876–883, Jul. 2005.

[20] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, “Selfbiased cmos current reference based on the ztc operation condition,” in *Integrated Circuits and Systems Design (SBCCI), 2014 27th Symposium on*, Sept 2014, pp. 1–7.

[21] S. B. Chiah, X. Zhou, and L. Yuan, “Compact Zero-Temperature Coefficient Modeling Approach for MOSFETs Based on Unified Regional Modeling of Surface Potential,” *Electron Devices, IEEE Transactions on*, vol. 60, no. 7, pp. 2164–2170, July 2013.

[22] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, “MOSFET ZTC Condition Analysis for a Self-biased Current Reference design,” *Journal of Integrated Circuits and Systems*, vol. 10, no. 2, pp. 103–112, December 2015.

[23] M. Sze, *Physics of Semiconductor Device*. Wiley, 1981.

[24] F. Serra-Graells and J. Huertas, “Sub-1-v cmos proportional-to-absolute temperature references,” *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 1, pp. 84–88, Jan 2003.

[25] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Second Edition*. Wiley-IEEE Press, 2004.

[26] H. Gopal and M. Baghini, “Trimless, pvt insensitive voltage reference using compensation of beta and thermal voltage,” in *VLSI Design and 2014 13th International Conference on Embedded Systems, 2014 27th International Conference on*, Jan 2014, pp. 528–533.

[27] C. Galup-Montoro, M. Schneider, H. Klimach, and A. Arnaud, “A compact model of mosfet mismatch for circuit design,” *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 8, pp. 1649–1657, Aug 2005.