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A new Method for the Analysis of Radiation-induced Effects in 3D VLSI Face-to-Back LUTs

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***Abstract*— In recent years, three-dimensional IC (3D IC) has gained much attention as a promising approach to increase IC performance due to their several advantages in terms of integration density, power dissipation and achievable clock frequencies. However, the reliability of 3D ICs regarding soft errors induced by radiation is not investigated yet. In this work, we propose a method for evaluating the sensitivity of 3D ICs to Single Event Transient induced by Heavy Ions. The flow starts with identifying the characteristics of the generated transient pulses with respect to the radiation profile and 3D layout of the design. Secondly, our method provides a Dynamic Error Rate using a Simulation-based Fault Injection environment. Experimental results achieved applying the approach on a 15nm 3D configurable Look-Up-Table (LUT) designed on two tiers demonstrated the feasibility of the method, showing the vulnerability characterization of four different functional configurations using eight different types of heavy ions.**

Keywords—3D IC, Configurable Logic, Single Event Transient

I. Introduction

In recent years, three-dimensional IC (3D IC) has gained much attention as a promising approach to increase IC performance. In fact, by stacking multiple silicon layers with vertical connections by Through Silicon Vias (TSVs), 3D integration offers new opportunities for alternative designs and optimizations. 3D ICs are integrated circuits which implementation is distributed among several layers interconnected by short, vertical and fine-grained vias. Placing and routing circuits in three dimensions provides several advantages such as higher integration density, less power dissipation and higher achievable clock frequency. Additionally, the overall system-on-chip cost and performance can be optimized by integrating in dedicated tiers layers with different functionalities, e.g., dividing logic and memory or analog and digital functionalities [1][2]. In fact, one of the main applications that utilizes such benefits is the stacking of memory on logic. Current exploration is focused mainly in applications with regular structures, such as imagers, memory and field programmable gate arrays [3][4][5].

Beside all these promising features, the 3D ICs reliability has not been evaluated widely. In fact, decreasing the size of transistors induces a lower tolerance for soft errors. Typically, soft errors are caused by outer incident particles (e.g., heavy ions, protons, alphas and neutrons) and the soft error rate (SER) is proportional to the flux of incident particles. Thus, in multi-tiers circuits, different analysis on how SER is distributed in 3D ICs must be carried out and the soft error susceptibility of different dies should be investigated [6]. Due to the novelty of this technology, few studies have been made so far on the evaluation of its sensitivity to radiation, and the most of them, at the best of our knowledge, are addressing the 3D-memory dependability [7][8][9].

This work aims to provide an evaluation framework to identify the radiation vulnerability of 3D circuit implementing the Logic staked layers. Our approach is based on a tool chain composed by our developed tool, Rad Ray, which is able to evaluate the effect of a radiation particle interacting within a given device and compute the features of the generated Single Event Transient (SET) pulses. As a second part of the tool chain, we developed an Injection Environment that allows injecting SET pulses effect in the target layout and obtaining the failure rate. In order to provide this evaluation, we designed a 3D model of a configurable Look-Up-Table. This model together with the user and configuration memory elements is one of the primitive blocks building configurable devices. The 3D LUT is made of two tiers, one for the configuration memory and one for the multiplexers building the functional part of the design. We generate the effects produced by eight different ions and perform the fault injection using four different LUTs function configurations and we provide the vulnerability comparison.

II. Background

The 3D-integration technology process, which is gradually becoming more practical, consists in stacking several portions of an integrated circuits vertically with fine-grain 3D interconnects [1]. 3D ICs are made by layers of 2D chips placed on separate layers stacked on top of each other, as showed in Fig. 1.

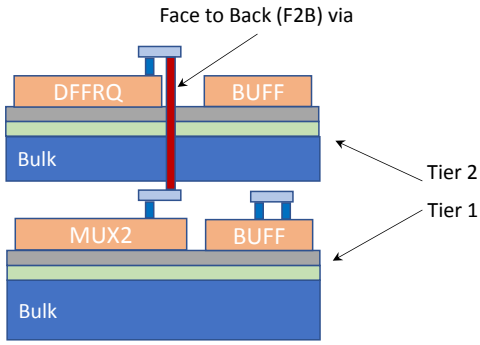

Fig. 1. An example of 3D Integrated Circuits section with two tiers and a Face to Back (F2B) interconnection via between a MUX2 and a DFFRQ cell.

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Considering that in 2D circuits most of the silicon area, power consumption and delays are due to wires, adding a dimension to the design implementation provides opportunities to shorten the interconnections to have less delay, faster clock frequency and higher integration density. In fact, the 3-D architecture offers more flexibility in system design, placement, and routing. For instance, if the gates of critical path are placed in adjacent layers, it leads to a shortened distance between them, with a significant reduction on RC delay. Additionally, it is possible to place circuit's portions with different voltage or power requirements in different layers allowing power saving techniques or separate in different tiers analog and digital components in mixed signal systems reducing electromagnetic interference [2].

A. *3D Face-to-Back Look-Up-Table Design*

The advent of 3-D architecture applied to reconfigurable devices like Field Programmable Gate Arrays (FPGAs) made the realization of reconfigurable devices adopting 3D VLSI based on two tiers feasible[10]. Radiation-effects on traditional FPGA devices have been widely explored in the past, especially in relation to the Single Event Transient (SET) phenomena [11], but no evaluation has been done yet on 3D devices. In order to design an efficient 3D Look-Up Table usable on 2-tiers 3D FPGAs, we designed a 5-inputs LUT placing a cascade of 2-inputs MUXes at the tier 1 using the traditional scheme illustrated in figure 2.

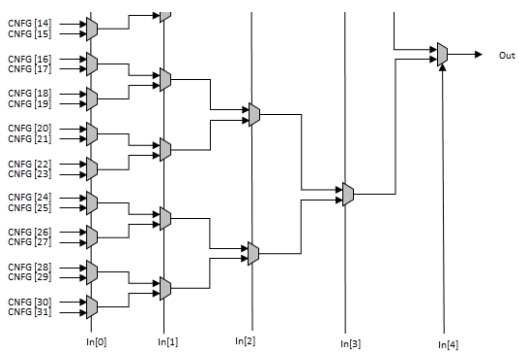

Fig. 2. A portion of the traditional LUT implementation scheme. Configuration bit (CNFG) feds the inputs of the first level of 2-inputs MUXs. LUT inputs are connected to the selectors of the respective MUX levels.

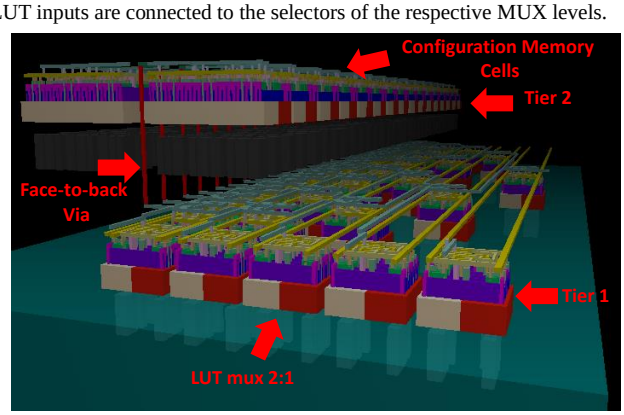

Fig. 3. A 3D rendering of the designed two tiers 5-inputs LUT using face-to-back vias interconnect between the configuration memory cells (on the top tier) and the LUT multiplexers (on the bottom tier). For the sake of clarity we did not show the Tier 2 bulk area.

The layout of a 2D LUT is characterized by configuration memory (CM) cells generally placed close to the inputs of the first 2-inputs MUX level and they are physically placed at the same VLSI tier. For the purpose of this work, we placed the 32 CM cells at the second tier and we connected each CM's output pin to the respective MUX configuration inputs using a face-to-back interconnection vias. As a result, we obtain a LUTs where the CM cells are partially overlapping the MUXes but the overall performances of the LUT is not affected since MUXs placement is optimized and not affected by the 3D structure of the LUT. A graphical rendering of the implemented 3D 5-inputs LUT is illustrated in Figure 3.

III. The Radiation-Effect Analysis Methodology

The Radiation Sensitivity evaluation proposed in this paper consists of two main stages, as summarized in Figure 4. The first stage is devoted to the characterization of the SET pulses with respect to the radiation profile and the post-implementation layout of the circuit under analysis. The core of this stage is related to a Monte Carlo-based radiation analysis tool which is able to generate the radiation-induced SET effect on the basis of the technology layout of the analyzed cell. The list of SET pulses is used by the second stage of the tool chain, the simulation-based fault injection environment. In this stage, the Dynamic Error Rate relative to the same list of SET is obtained by injecting them in the post-synthesis netlist of the circuit under analysis in order to evaluate the impact of the SET pulses to the behavioral functionality of the LUT under analysis.

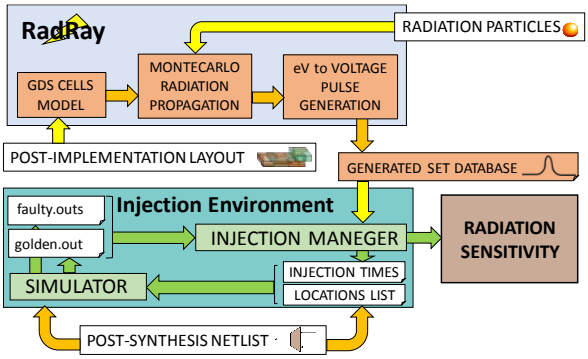

Fig. 4. The developed radiation-effect analysis methodology.

A. *Montecarlo-based Radiation Analysis: RadRay*

The developed *RadRay* tool elaborates the netlist layout cells in the form of GDS layout files with respect to the radiation profile of the mission which includes the type of the existing ions in the environment under the study, the energy and flux of the particles. The tool simulates the effect of a highly charged particle traversing the silicon junction of the device. The produced free mobile carriers are concentrated within the depletion region of a p-n junction in the transistor sensitive parts individuated by the RadRay algorithm. The eV transmitted by the particles, depending on the traversed section of the cell, can cause a voltage glitch that is propagated to the output of the transistor and finally, to the output of the cell, generating a SET effect into the circuit.

B. *Simulation-based Fault Injection*

The Fault Injection Environment is devoted to estimate the Dynamic Error Rate for the given circuit with respect to the SET pulses generated by a given incident particles. This is obtained by simulating the behavior of the circuit while each one of the SET pulses calculated by *RadRay* is injected in a random location of the netlist at random time and comparing the outcome with the golden circuit. To obtain this information, the synthesized netlist of the circuit is used to take into account not only the logic behavior but also the timing of the gate in the design considered. In fact, the broadening or the filtering of the SET pulse is related mainly to the logic and physical masking capability of the circuit.

```
// Fault List Generation
Read location_list
Read pulse_widths
Set fault_list[]
FOR each i in pulse_widths:
      fault_list[i]<=(pulse_widths[i],random(location_list))
ENDFOR
// Testbenches Generation
CALL write_tb(NONE,golden.tb) //do not insert fault
FOR each i in fault_list:
      //Insert faults[i] at Random time in simultion
      CALL write_tb(fault_list[i],faulty_i.tb)
ENDFOR
// Run Simulations
RUN golden.tb
Read golden_dump.vcd
FOR each faulty_i.tb:
      RUN faulty_i.tb
      Read faulty_i_dump.vcd
ENDFOR
// Ananlyze Results
FOR each faulty_i.vcd
      compare(golden.tb, faulty_i.vcd)
      log case fault_free
          'FF'
          case pulse_out
            'out_width, PIPB'
          case glitch
            'GLITCH'
          case undefined
            'UNKNOWN'
ENDFOR
```

Fig. 5. The pseudo-code of the simulation-based fault injection environment.

The whole injection campaign is automatically operated by the Fault Injection Manager (FIM). The FIM receives as inputs the list of SET pulses with their duration and the list of all the possible fault locations. The fault locations are considered as all the input ports of the gates in the design. From these two lists, the FIM is selecting randomly a location in the design and a SET pulse to generate a list of faults. For each element in the list of faults, a testbench for the design is created. In each testbench, the signal indicated by the location is affected by a pulse of the relative width in a random moment of the simulation. At the end of this stage, the FIM produces several testbench equal to the number of elements in the fault list. The FIM will also execute a script to automatically launch all simulations in the simulator and collects the dumps of the simulation outputs. When all the simulations have been executed, the FIM compares the outcome of the faulty simulation with the golden one and extract the number of injections that provoke a wrong output and the type of misbehavior occurred.

IV. Experimetntal Results

The 3D-VLSI LUT designed on two tiers has been realized using the Nan Gate Open Cell library [12] resized at 15 nm. The netlist of the LUT is composed of 31 MUX2_X1 (2 inputs and 1 output) with a total of 68 nets. The total number of wires composing the nets and the configuration memory cell face to back vias is 96, which corresponds to all the input signals of the MUXes. The Standard Delay Format (SDF) of the netlist has been obtained using Design Compiler. The SDF model has been modified according to the 3D cell delays obtained by the post-implementation layout in order to properly simulate the behavior of the physical design.

The radiation analysis has been performed instrumenting the Monte Carlo analysis tool with the Heavy Ion profile related to the facility of UCL [13]. The characteristics of the analyzed particles are reported in Table I where the type of Ions, energy, range and Linear Energy Transfer (LET) values are reported.

TABLE I. Particles Analyzed by the Monte Carlo RadRay Analysis tool

Ion	DUT Energy [MeV]	Range [um Si]	LET [MeV/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{22}Ne^{7+}$	238	202.0	3.3
$^{27}Al^{8+}$	250	131.2	5.7
$^{40}Ar^{12+}$	379	120.5	10.0
$^{56}Cr^{16+}$	513	107.6	16.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{84}Kr^{25+}$	769	94.2	32.4
$^{124}Xe^{35+}$	995	73.1	62.5

Once the radiation analysis has been performed, the location and event timing of the transient effects are used for the simulation-based fault injection environment in order to calculate the dynamic error rate and evaluate the sensitivity of different LUT functional configurations.

Two different Fault Injections campaigns have been carried out, one for the MUXs architecture and the other one for the Configuration Memory. The first campaign has been developed feeding the Fault Injection Manager (FIM) with the location list relative to all the signals that feed the internal MUXs and the SET characterizations obtained with radiation analysis in the MUX layer. The second campaign has been carried out with the radiation analysis results on the Configuration Memory tier and the inputs of the first layer of MUXes as locations list. Both two campaigns have been executed for the radiation profile consisting of the 8 types of ions used by the radiation analysis.

To evaluate the behavior of the LUT, 5 different function configurations have been evaluated: 5 Inputs AND, OR, XOR and XNOR, and one NOT configuration. For each configuration, a golden testbench have been developed. Each testbench has a fixed configuration and the inputs signals of the LUTs switch all the possible 2^5 combinations. Starting from the golden one, the FIM automatically creates 10,000 faulty test-benches by inserting a pulse in a random location and time with respect to the transient list provided by the radiation analysis. The outcome of each simulation is automatically saved in a *vcd* file, a standard file that contains all the simulation waveform information (i.e. rising and falling edge event and time). At the end of each simulation the faulty *vcd* file is compared with the one obtained with the golden simulation and the results of the comparison are compacted in a comprehensive report.

The radiation analysis results on the 3D-LUT layout are illustrated in Figure 6. In particular, the cross-section per cm^2

has been reported on the MUX2 and CM tiers. The result shows that for low energy heavy ions, the cross-sections of CM and MUX2 are equivalent, vice versa, with the increasing of the heavy ions energy, the configuration memory tier results almost twice sensitive than the MUX2 tier. This difference should be related to the partial geometrical overlap of the configuration memory cells with respect of the MUXes on the different tiers: some particles are crossing both tiers provoking multiple transient effects.

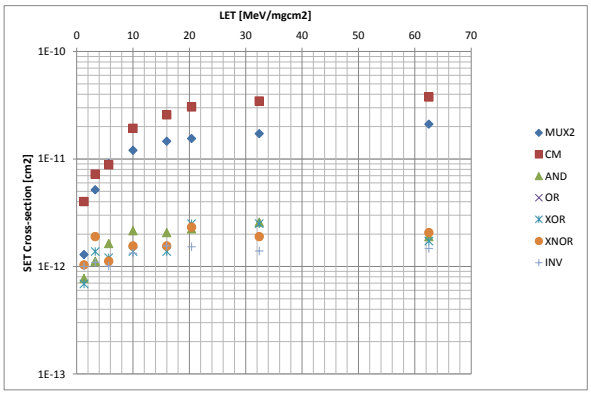

Fig. 6. Single Event Transient (SET) cross-section [cm^2] for static radiation analysis (MUX2 and CM) and after computing the dynamic analysis for five LUT configuration (AND, OR, XOR, XNOR and INV).

Fig. 7. MUX Layer and Configuration Memory Layer Error Rate for AND, OR, XOR, OR, XNOR and NOT functions for the 8 selected Heavy Ions.

The dynamic fault simulation analysis results are reported in Figure 6 and in Figure 7. In details, figure 7 reports the distribution of the injection of 10,000 transient effects generated by the radiation analysis into the simulation model. Interestingly, the distribution of the error rate is approximately equivalent between the logic function analyzed. With the obvious exception of the OR function, the LUT configuration at AND, XOR, XNOR and INV provides the similar error rate. However, LUT functions result more sensitive to transient effects generated into the MUXes tier.

As second relevant results, it has been possible to observe cross-section derating with respect to the static analysis performed on the MUX2 and CM. As reported in Figure 6, the dynamic cross-section of the 3D-LUT is around one order of magnitude less than the static cross-section..

V. Conclusion and Future Work

In this paper, we proposed a novel methodology to analyze the radiation-induced transient effects on novel 3D double tiers reconfigurable Look-Up-Tables (LUTs). A design of double tiers 5-inputs LUT has been developed using face-to-back interconnection via between the configuration memory and the logic tiers. The design has been used as benchmark of the developed analysis method that allows to achieve static and dynamic cross-section of the LUT thus demonstrating the feasibility of the approach. For future work, we plan to investigate 3D routing reconfigurable architecture including more than two tiers and evaluating different interconnection via such as face to face and TSV interface.

References

[1] K. Banerjee, S. J. Souri, P. Kapur and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," in Proceedings of the IEEE, vol. 89, no. 5, pp. 602-633, May 2001

[2] L. Zhou, C. Wakayama and C. -. R. Shi, "CASCADE: A Standard Supercell Design Methodology With Congestion-Driven Placement for Three-Dimensional Interconnect-Heavy Very Large-Scale Integrated Circuits," in IEEE Transactions on CAD, vol. 26, no. 7, pp. 1270-1282, July 2007.

[3] T. Tanaka, H. Kino, R. Nakazawa, K. Kiyoyama, H. Ohno and M. Koyanagi, "Ultrafast parallel reconfiguration of 3D-stacked reconfigurable spin logic chip with on-chip SPRAM (SPin-transfer torque RAM)," 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, 2012, pp. 169-170.

[4] F. Furuta et al., "Scalable 3D-FPGA using wafer-to-wafer TSV interconnect of 15 Tbps/W, 3.3 Tbps/mm2," 2013 Symposium on VLSI Circuits, Kyoto, 2013, pp. C24-C25.

[5] S. G. Singapura, R. Kannan and V. K. Prasanna, "On-chip memory efficient data layout for 2D FFT on 3D memory integrated FPGA," 2016 IEEE High Performance Extreme Computing Conference, Waltham, MA, 2016, pp. 1-7.

[6] H. Han, J. Chung and J. Yang, "READ: Reliability Enhancement in 3D-Memory Exploiting Asymmetric SER Distribution," in IEEE Transactions on Computers, vol. 67, no. 8, pp. 1193-1201, 1 Aug. 2018.

[7] M. Bagatin et al., "Effects of Heavy-Ion Irradiation on Vertical 3-D NAND Flash Memories," in IEEE Tran. Nuc. Science, vol. 65, no. 1, pp. 318-325, Jan. 2018.

[8] M. Taouil, M. Masadeh, S. Hamdioui and E. J. Marinissen, "Interconnect test for 3D stacked memory-on-logic," 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2014, pp. 1-6.

[9] M. Sato, R. Egawa, H. Takizawa and H. Kobayashi, "On-chip checkpointing with 3D-stacked memories," 2014 International 3D Systems Integration Conference (3DIC), Kinsdale, 2014, pp. 1-6

[10] Q. Zhao, Y. Iwai, M. Amagasaki, M. Iida and T. Sueyoshi, "A novel reconfigurable logic device base on 3D stack technology," 2011 IEEE International 3D Systems Integration Conference (3DIC), 2011, Osaka, 2012, pp. 1-4.

[11] L. Sterpone, N. Battezzati and V. Ferlet-Cavrois, "Analysis of SET Propagation in Flash-Based FPGAs by Means of Electrical Pulse Injection," in IEEE Transactions on Nuclear Science, vol. 57, no. 4, pp. 1820-1826, Aug. 2010.

[12] L. Gong, Y. Xu, Z. Zhang, W. Shi and R. K. F. Teng, "An open 45nm PD-SOI standard cell library based on verified BSIM SOI spice model with predictive technology," 2013 IEEE 10th International Conference on ASIC, Shenzhen, 2013, pp. 1-4.

[13] A. O. Akhmetov et al., "IC SEE Comparative Studies at UCL and JINR Heavy Ion Accelerators," 2016 IEEE Radiation Effects Data Workshop (REDW), Portland, OR, USA, 2016, pp. 1-4.