High Voltage Temperature Humidity Bias Test (THB) customized system and methodologies for reliability assessment of power semiconductor devices

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D. Cimmino[a,b], R. Busca[a,b], S. Ferrero[a], F. Pirri[a], G. Richieri[b], R. Carta[b]

[a] DISAT, Polytechnic of Turin, *Turin, Italy*
[b] *Vishay Intertechnology Inc., Borgaro Torinese, Italy*

Abstract

High Voltage Temperature Humidity Bias Test (THB-HV) is currently the state of the art test method for reliability evaluation of power devices in high humidity environments at high voltage. These conditions have become especially significant in the case of power modules for the automotive industry and other applications in harsh environments. In this research work, a custom system for active monitoring of THB-HV testing is developed and customized, in order to evaluate different testing methodologies, intercept device degradation in real time, and allow for a controlled and more accurate failure analysis of the DUTs.

1. Introduction

One of the key challenges of our century is the transition towards a green and sustainable electric power based society. Hence, the reliability of modern applications in the fields of transportation, power generation and conversion, becomes a major issue that needs to be addressed. In particular, when we think about automotive or harsh environments applications like offshore wind turbines [1], we can better understand the consequences of a possible failure on the field, directly impacting the safety of the user or the quality of the service, as well as bringing increasing management and maintenance costs for both companies and final users.

In these applications, the typical elements of power circuitry, such as diodes and IGBTs, are exposed to high humidity, high voltage and high temperatures at the same time. The combined effects of these stressors give rise to specific failure modes and cause the failure of the single device with consequences on the entire system.

An emblematic example is the one of integrated IGBTs and diode in power modules. These devices, aside from the surface passivation of each chip and a thick permeable layer of silicone gel, have no effective protection against humidity penetration, especially if the enclosure of the circuit is directly exposed to environmental factors. In these conditions, the combined effect of humidity and high voltage, triggers multiple failure mechanisms such as metallization corrosion, formation of dendrites and outgassing [2]. Although several works have been published involving HV-THB testing, our study focuses on devices with rated blocking voltage below 1000 V, a range that has not been investigated by most authors, focusing on IGBTs and diodes rating up to 6.5kV [3] , while our research activity focuses only on 650V rated power diode samples. In addition, the testing methodology is not always the same, nor the type of control is approached in the same way as in our test system with respect to previous works. In particular, as described in chapter 2, we complement our approach including the use of an additional voltage ramp to start the test. Moreover, as we describe it in section 3.3, our methodology is applied to the study of several passivation schemes, allowing extended analysis of the failure mode, and the selection of the best technological solution among the ones implemented in our sample set.

1.1. Current Testing Methodologies

The current standard automotive THB test (H3TRB) sets the conditions of the test at 85 °C, 85% relative humidity (R.H.), and a maximum reverse bias of 100V [4], with a no failure requirement of 1000 hours for product qualification. Previous works on THB-HV testing [5] highlight the importance of raising the voltage level, in some cases up to 90% of

* Corresponding author. davide.cimminopolito.it
Tel: +39 346 5859817

the device nominal voltage, in order to accelerate the test and evaluate the DUTs ruggedness against the presence of the previously described failure modes.

Moreover, the management of the test itself can introduce stress factors in addition to the main ones, so standardizing the test methodology becomes fundamental in order to get as much information as possible from the test.

For these reasons, the combination of real time monitoring of the devices with automatic PSU control, paves the way to a better experimental evaluation of the devices during and after the failure. Consequently, as it will be shown in the following sections, it is possible to gather better intel about the nature of the DUTs while avoiding critical failure. The latter is a critical step for a test that is not yet an official standard and still requires careful evaluation.

2. Methodology and test system

2.1. System Architecture

The measurement system is described in Fig.1. A control and monitoring unit, realized with a National Instruments PXIe-1085 supporting the LabVIEW programming environment. The PXI includes a digital multimeter (DMM) and 4 PXIe 2527 switches. A power supply unit (PSU) Elektroautomatik PS9000, with a 750 V maximum voltage output, is controlled via USB and connected to the monitoring unit.

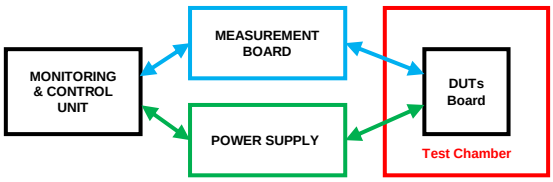

Fig. 1. System architecture.

This configuration allows for both data-logging and active monitoring of the DUTs. In our experimental activity, we only considered power diodes so the system is configured to monitor the leakage current of each device. The final biasing and monitoring circuit is shown in Fig.2. The diodes are reverse biased by the PSU, and the DMM performs the voltage measurement through the switch. The latter cycles through the selected channels, and returns the voltage drop on each resistor, thus allowing leakage current monitoring of the DUTs.

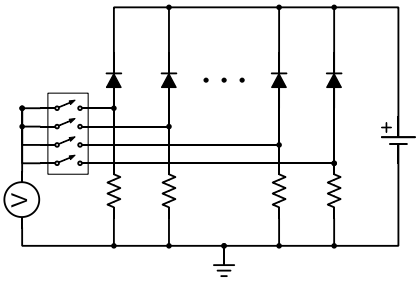

Fig. 2. Schematic of the measurement circuit.

2.2. Software Implementations

Due to the nature of the DUTs and the test, some custom features have been implemented in order to achieve monitoring and control of the THB-HV test. The core loop of the LabVIEW program performs a measurement of all the selected channels with the defined speed and resolution, which are both fully customizable to multiple class of devices. The real time data are then processed and visualized at each measurement, so that changes in the behaviour of the devices can be identified right from the beginning of the test.

The main control features of the system are based on the *percentage* threshold and *absolute* threshold of the measured current value. Both these options have the possibility to interrupt the test when the actual leakage value of the device overcomes the selected limit, thus saving them from critical damage. These controls act on each individual channel, and as soon as one channel triggers the condition its number is returned to the user, the bias is removed and the test is stopped.

Apart from monitoring and high voltage, an additional feature has been added to the system, in order to study the effects of how the voltage is initially applied to the DUTs, which is not part of the standard H3TRB methodology. This additional feature is the possibility to ramp the voltage up to the target DC bias of the test. The voltage ramp brings all devices to the desired bias level, and the duration and the step increase of the voltage can be controlled individually. Eventually, in order to avoid condensation, the DUTs are inserted into the chamber at ambient temperature, and then the chamber is ramped up to the nominal conditions of humidity and temperature, only at that point bias is applied [2]. As such, with the use of a ramp, we added an additional control to evaluate the test methodology and its effects on the devices.

2.3. Test Conditions and DUTs

Firstly, before the test, all DUTs undergo a curvetracer measurement at room temperature, determining the initial conditions of the reverse I-V characteristics. DUTs are positioned in the climatic chamber, which is then ramped up to 85°C and 85% R.H. conditions. After waiting for 30 minutes, the voltage ramp is applied with a duration of 30 minutes. When the ramp reaches the selected voltage level, the test is officially started, and the regime conditions are shown in Table 1.

At selected time steps of 168, 500, 1000 hours (or more if needed) all DUTs are removed from the chamber, and after 12 h of rest at room conditions, a curvetracer measurement is performed. This process is repeated at each time step until a device exceeds the selected threshold criteria, or the test is deemed as over. Each DUT has been tested after each test step, with a Keysight B1505A curvetracer, assessing the actual status of the I-V reverse characteristics, and allowing for highly detailed electrical and failure analysis evaluations.

Table 1
Set of stressors applied during the test.

Parameter	Value
Temperature	85°C
Relative Humidity	85%
Voltage	80% V_{nom}

All tested DUTs are 650V power diodes in standard MTP dual die power modules. These samples were prepared with the purpose of evaluating the nature of the failure mode and several termination passivation schemes.

3. System evaluation and results discussion

3.1. Monitoring of the leakage current

A typical curve of 650V with 80% voltage rating applied is reported in Fig. 3. At the beginning of the test, all devices exhibit a slow initial increasing and decreasing evolution of the leakage current. This phenomenon can be attributed to moisture penetration and interface charge relocation, and in particular to local charge distribution inside the termination of the devices, when interacting with the applied electric field. After the initial phase, typically lasting around 10 h, all devices stabilize asymptotically toward a stable current level.

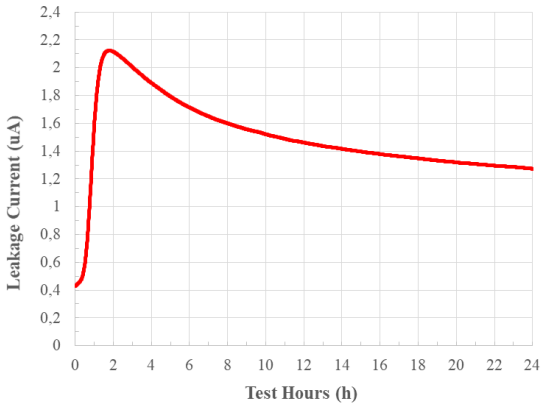

Fig. 3. Leakage current evolution in the first 24 hours of the test for a 650V diode polarized at 80% V_{nom}

At this point, as in section 2.2, control can be switched to percentage threshold mode. In this way the reference value is set to the regime level, and control is performed more coherently with the testing methodology and the nature of the DUTs.
This kind of phenomenon is mostly present only at the first start of the test, and thanks to our software implementation, the use of an optimized voltage ramp has helped the devices reach the regime level with a smooth evolution.

3.2. Curvetracer Analysis

As discussed in section 2.3., in order to identify and understand the kind of degradation that affects the devices, each test is complemented with an I-V analysis of the reverse characteristics of the diodes, before and after each step of the test session. Fig. 4 shows an example where the electrical characteristics of the DUTs are mostly unaffected by the stress conditions.

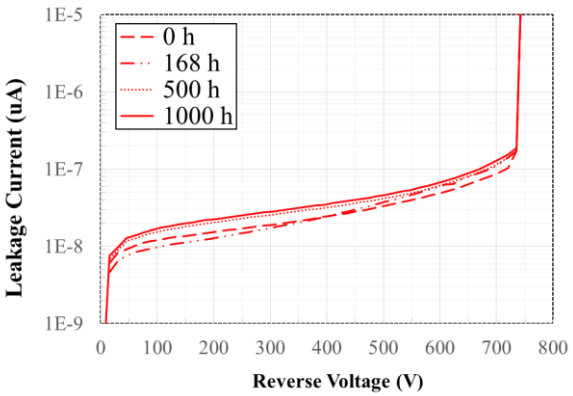

Fig. 4. I-V reverse characteristic of a 650V diode, tested at 0h, 168h, 500h and 1000h, exhibiting no electrical degradation.

During the test, the monitoring presented a stable leakage current level up to 1000h. This stability is then confirmed by the curvetracer analysis, the shape of the characteristic remains the same even after 1000h of testing, and further optical and SEM inspections confirm the absence of morphological or physical wear of the device.

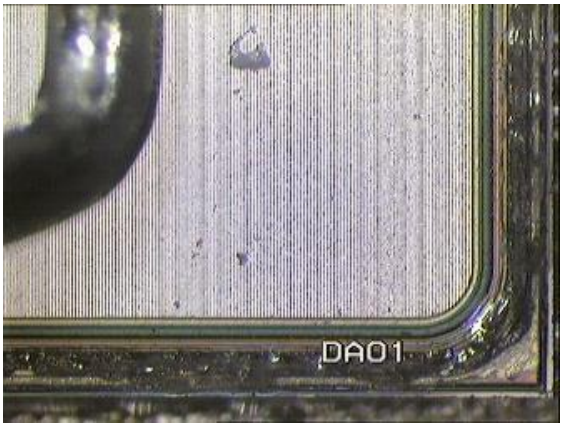

Fig. 5. Optical inspection of a 650V tested diode after 168h at 80% V_{nom} shows consistent lifting of the secondary passivation layer on the whole device edge termination, due to moisture penetration.

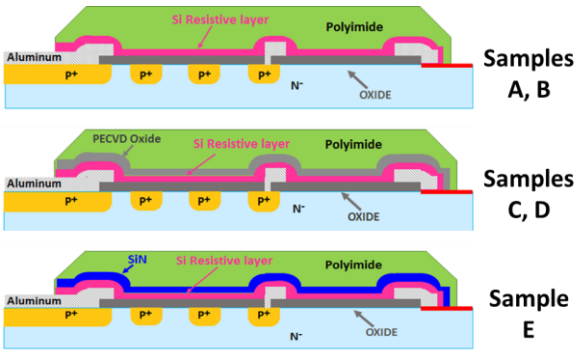

Fig. 6. Sample structures involved in the testing of passivation schemes resulting in the SEM/FIB analysis reported in Fig. 7. A combination of Oxide – LTO and resistive silicon is used as a primary passivation layer, while secondary passivation differs according to each device group. All samples have been realized with an upper polyimide layer, under which an additional insulating layer has been added, being PECVD Oxide for samples C and D, and SiN for sample E.

3.3. Failure Analysis

As already highlighted, thanks to the threshold control, device degradation is intercepted in time,

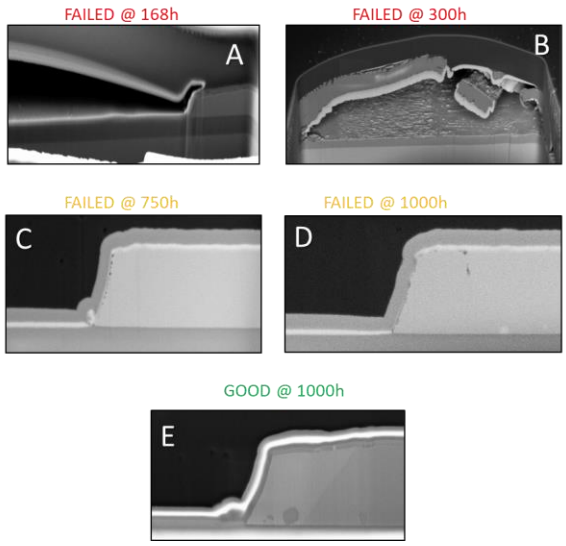

Fig. 7. SEM cross-section of selected DUTs termination. Both samples A and B show significant secondary passivation lifting, **which** involv**es** also the underlying layers. Samples C and D show small voids at the interface between primary and secondary passivation layers, while sample E shows no degradation at all.

allowing for a more accurate failure analysis of the DUTs. After the initial testing, the analysis flow continues with an optical inspection of the selected DUTs, followed by a FIB/SEM analysis. One example of optical inspection is reported in Fig. 5, performed on a DUT failed at 168h. In such case, the leakage monitoring shows electrical degradation, but only due to the inspection we can link this phenomenon to the consistent morphological variation of the surface. The curvetracer analysis also confirms a significant variation of the breakdown voltage (BV) limit of the reverse I-V characteristic.
This variation can be identified as the cause of leakage drift observed during the monitoring phase, confirming what has been evidenced in previous studies [6].
The actual nature and entity of degradation induced by the test is then analysed through FIB/SEM in order to complete the methodology flow
For this purpose, a set of 5 passivation schemes have been tested under HV-THB on sample devices, with the purpose of understanding differences in failure mode induced by different passivation materials, with the aim to enable further analysis thanks to our control system. All selected samples have a standard metal field plate field limiting ring termination structure, where the primary level passivation consists of a compound structure including thermal oxide – LTO and a resistive silicon layer, while the secondary passivation layer is structured as shown in Fig. 6. All

samples have been realized with an upper polyimide layer, under which an additional insulating layer has been added, a PECVD Oxide for samples C and D, and SiN for sample E.

In sample A, device degradation is visible as polyimide lifting with the formation of “bubbles” on the surface of the die, as reported in Fig. 6. This effect is due to gas formation caused by electro-chemical migration phenomena at the interface between the resistive silicon and oxide layers. At high electric fields, a resistive silicon layer degradation appears to be the main factor of device failure, acting in combination with surface moisture permeating through the polyimide layer. Final degradation and expansion of the bubble can be attributed to the formation of leakage current paths generating additional stress due to joule heating. In sample B, which was hold in test for 300 hours, degradation is more severe and extending down to the aluminium metal field plate, where electrochemical migration generates erosion of the aluminum layer. Differently from sample A and B, optical inspection performed on samples C and D does not reveal any sign of physical degradation, for this reason a FIB/SEM analysis becomes fundamental in determining the fine details of failure mode, as expected by degradation of the characteristics seen during electrical testing. For the same reason, in samples C and D, it is possible to see the formation of holes at the interface between resistive silicon and oxide layers, appearing at the field peaking point of the termination structure.

In the case of sample E, electrical testing and optical inspection do not show any sign of degradation after 1000 hours of testing. This result is confirmed by the FIB/SEM analysis, and is justified by the presence of the SiN layer, which remarkably increases shielding against the combined effect of high voltage and humidity, enhancing the overall performance of the sample in HV-THB test and consequently its ruggedness.

4. Conclusions

The THB-HV highlights particular failure modes due to the interaction of high voltage and humidity at high temperature, as such it is becoming increasingly significant in assessing the reliability of power devices. We have developed and evaluated a system and a methodology capable of giving coherent and detailed information regarding the ruggedness of high voltage power diodes and enabling further study on reliability testing and design enhancement. Additional software controls have been added in order to perform a stable and non-invasive test and carefully follow the electrical evolution of the DUTs. While avoiding any critical failure, this methodology paves the way to a highly detailed failure analysis of the devices and their internal structures, while giving remarkable insights on the enhancement of secondary passivation structures.

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