Doctoral Dissertation
Doctoral Program in Energy Enginering (31.th cycle)

On-line Junction Temperature Estimation of SiC Power MOSFETs

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May 2, 2019

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Turin, May 2, 2019

Summary

The ability to monitor the junction temperature of power devices during the operation of a power converter will be a key enabler towards higher performance and reliability of power electronics. Starting from the well-known dependency of the R_{ON} with the junction temperature of SiC power MOSFETs, innovative solutions are proposed in order to obtain a high-dynamic estimation of the junction temperature on board of a real converter. After the initial commissioning of the power module performed directly in the field, the device temperature is real-time observed during current controlled operation of the converter. Furthermore, this technique provides precious information about the state of health of the power modules. A proof of concept test rig and a 3-phase custom inverter, designed of for Formula SAE Electric have been designed, built and tested to validate the proposed solution. The results of the thesis demonstrate the effectiveness and feasibility of the proposed methodology, in terms of extra performance and augmented reliability of the power modules. Additional studies on lifetime prediction strategies are ongoing.

Acknowledgements

I am infinitely beholden to my supervisor, Prof. Gianmario Pellegrino, for his invaluable support, expert advice and for helping me numerous time through the complex process of completing my doctoral degree. I am equally grateful to my co-supervisor, Prof. Eric Armando for his fantastic expertise and indispensable input that helped steer my research in the right direction on countless occasions. I am truly thankful to my beloved family and dear friends for supporting me throughout my doctorate.

"The history of science shows that theories are perishable. With every new truth that is revealed we get a better understanding of Nature and our conceptions and views are modified."

Nikola Tesla

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List of Abbreviations

ADC	Analog to Digital Converter
API	Application Program Interface
DAC	Digital to Analog Converter
DBC	Direct Bonded Copper substrate
DMA	Direct Memory Access
FMC	Flexible Memory Controller
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
GPIO	General-Purpose Input/Output
GUI	Graphical User Interface
IC	Integrated Circuit
IR	Infrared Radiation
MCU	MicroController Unit
POC	Proof Of Concept
SOA	Safe Operating Area
SPI	Serial Peripheral Interface
SPICE	Simulation Program with Integrated Circuit Emphasis
SVM	Space Vector Modulation
SWD	Serial Wire Debug
TSEP	Thermo-Sensitive Electrical Parameter
USART	Universal synchronous and asynchronous receiver-transmitter

Chapter 1

Introduction

The first studies on Silicon-Carbide (SiC) semiconductors began in 1955, when the first methodologies for growing a pure crystal were presented [1]. At the time SiC was more popular than Si and Ge. However, due to the difficulty in obtaining high purity grade wafer, the SiC was abandoned until the 70'. In 1978 Tairov and Tsvetkov made the first high purity SiC wafer. In 1987 a new process for obtaining high purity SiC wafers at low temperature was developed. Cree launched the first commercial SiC LED and SiC wafer, respectively in 1989 and 1991. In the early 2000's the first SiC diodes became available on the market. In 2011 Cree launched the first commercial 1200 V SiC MOSFET [2].

Fig. 1.1 summarizes the main areas of use of the power semiconductor technologies today available on the market.

For many years, Si IGBT has been the traditional choice for power electronic applications, where high breakdown voltages and high currents are required. It has been widely used in power electronic application such as AC motor drives, UPS, power conversion for renewable energy(wind and solar). The IGBT has been developed in the 1980s and since that it has been continually improved [4]. Nowadays, IGBT devices continue to be used widely despite the number of studies pointing out the advantages of SiC MOSFETs over IGBTs [5], [6].

In IGBT devices low conduction resistances and high breakdown voltages are achieved by injecting minority carriers into the drift region. However, when the device is turned-OFF the minority carriers takes time to recombine, thus generating a "slow" commutation with a tail current.

In contrast, Silicon MOSFETs are devices based on majority carriers that permit to achieve high speed commutations. However, they have lower breakdown voltages and higher conduction resistances. During the year the Si MOSFET technology has been continuously improved and taken to its limits with the introduction of the Si-super-junction MOSFET. Fig. 1.2 shows the area specific resistance as a function of the blocking voltage. Si MOSFETs and Si super junction MOSFETs are only available for breakdown voltages up to 900 V. In turn, they are not suitable for

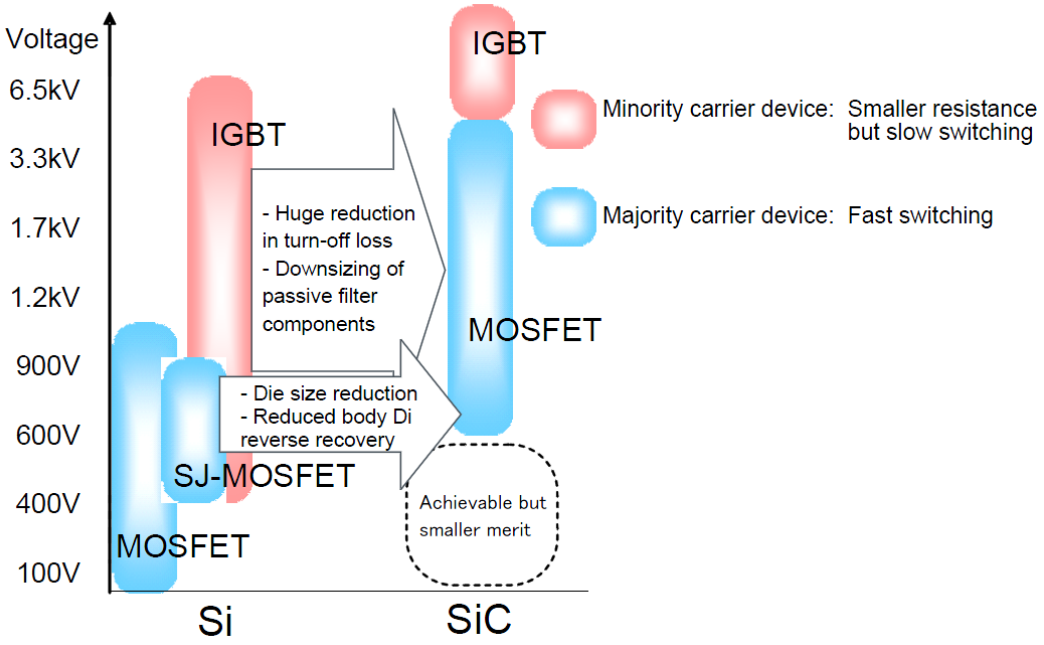


Fig. 1.1: Si vs SiC devices: areas of use and possible benefits [3].

medium and high power applications. Compared to Si, SiC has ten times the dielectric breakdown field strength. In turn, high voltage SiC power MOSFETs are feasible. SiC MOSFETs combine the desirable characteristics of IGBT and Si MOSFET.

SiC MOSFETs devices offer a series of advantages compared to their silicon counterparts. They permit to achieve lower conduction and switching losses, higher operating temperatures, higher breakdown voltages, better thermal stability and better thermal conductivity [7], [8]. SiC diodes are now widely used in high efficiency applications while the SiC MOSFETs still have obstacles in terms of market penetration. Nearly a decade after the introduction of the 1200 V SiC MOSFET, its application is still armed by the high price of the devices and by many unsolved challenges such us: high dv/dt, EMI emission [9], reliability, reduced surge capability [10], reduced thermal inertia and non standard gate drivers. SiC technology is critical to realizing the next generation of high efficiency power electronic converters. SiC devices permit to realize extremely compact and efficient power applications. In the last years a wide range of SiC MOSFET power modules has hit the market, making SiC semiconductors more competitive. The main advantages in using a power module respect to discrete devices are the higher power density, the easier heat extraction, the lower part count, the optimized layout (parasitics reduction) and higher reliability. Due to the low thermal inertia and to the high power density, accurate thermal management is mandatory to ensure reliability and take full advantage of new SiC devices and modules.

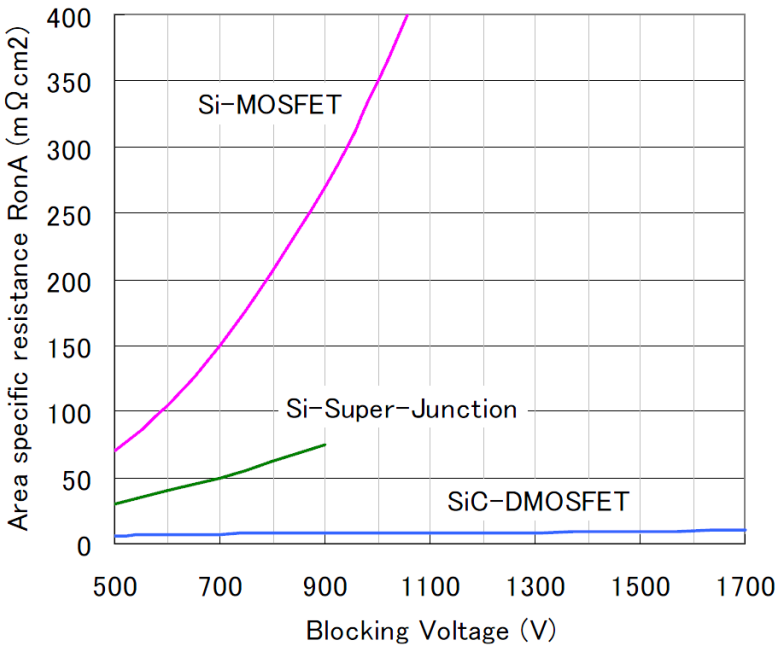


Fig. 1.2: Si vs SiC devices: R_{ON} at various breakdown voltages. [3].

1.1 Scope of the Thesis

The aim of this thesis is to provide a methodology to estimate the junction temperature of SiC power MOSFET modules implementable in hard switching industrial converters. An H-bridge proof of concept power converter and a three phase high power density inverter have been built to demonstrate the feasibility of the proposed methodology. Moreover, the presented methodology with minor modifications can be used for evaluating the health state of the power devices.

Section 1.2 contains the list of the published papers during the PhD program. Papers labelled as (c) and (g) concern the sensorless control of syncronous reluctance motor drives fed by matrix converter, with focus on the compensation of the converter voltage errors. This work is the result of a collaboration with the University of Nottingham, that the author visited for a semester. The initial plan was to investigate the SiC MOSFET matrix converter and to compare its performance with a Si IGBT counterpart. Such initial plan was later modified due to the non availability of both matrix converters. Although a consistent amount of time was dedicated to this activity, this is not reported in this thesis for the sake of clarity and brevity.

1.2 Published Papers

Journal papers:

(a) **F. Stella**, G. Pellegrino, E. Armando and D. Daprà, "Online Junction Temperature Estimation of SiC PowermosfetsThrough On-State Voltage Mapping," in IEEE Transactions on Industry Applications, vol. 54, no. 4, pp. 3453-3462, July-Aug. 2018. doi: 10.1109/TIA.2018.2812710

(b) **F. Stella**, O. Olanrewaju, Z. Yang, A. Castellazzi, G. Pellegrino, Experimentally validated methodology for real-time temperature cycle tracking in SiC power modules, Microelectronics Reliability, Volumes 88–90, 2018, Pages 615-619, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2018.07.072.

(c) **F. Stella**, A. Yousefi-Talouki, S. Odhano, G. Pellegrino and P. Zanchetta, "An Accurate Self-Commissioning Technique for Matrix Converters Applied to Sensorless Control of Synchronous Reluctance Motor Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics.
doi: 10.1109/JESTPE.2018.2851142

Conference papers:

(d) **F. Stella**, G. Pellegrino, E. Armando and D. Daprà, "Advanced testing of SiC power MOSFET modules for electric motor drives," 2017 IEEE International Electric Machines and Drives Conference (IEMDC), Miami, FL, 2017, pp. 1-8. doi: 10.1109/IEMDC.2017.8002314

(e) **F. Stella**, G. Pellegrino and E. Armando, "Coordinated On-line Junction Temperature Estimation and Prognostic of SiC Power Modules," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 1907-1913. doi: 10.1109/ECCE.2018.8557850

(f) **F. Stella**, G. Pellegrino, E. Armando and D. Daprà, "On-line temperature estimation of SiC power MOSFET modules through on-state resistance mapping," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 5907-5914. doi: 10.1109/ECCE.2017.8096976

(g) A. Yousefi-Talouki, **F. Stella**, S. Odhano, L. de Lilo, A. Trentin, G. Pellegrino and P. Zanchetta, "Sensorless control of matrix converter-fed synchronous reluctance motor drives," 2017 IEEE International Symposium on Sensorless Control for Electrical Drives (SLED), Catania, 2017, pp. 181-186. doi: 10.1109/SLED.2017.8078421

Chapter 2

Junction Temperature Measurement and Estimation

The main methods to estimate and to measure the junction temperature are presented in this chapter.

2.1 Direct Measurements Techniques

2.1.1 Physical Sensors

The junction temperature of a semiconductor can be measured using a thermo-sensitive material that can be put in direct contact or in proximity to the die. In power electronic, thermistor and thermocouples are widely used. Most of the power modules already integrate an internal thermistor, however only one thermistor per module is usually present. The embedded thermistor can only measure the temperature of the DBC without being able to give any information about the junction temperature. In literature, many solutions were presented where the temperature sensor is placed in direct contact with the chip [11], [12] and [13]. The direct contact permits the transfer of thermal energy from the device under test to the probe thus measuring the temperature with a high level of accuracy. However, this energy transfer affects the temperature of the device under test modifying the thermal transfer path. Depending on the dimensions and on the type of contact between the probe and the device a delay and an attenuation of the temperature measurement have to be expected due to the probe thermal inertia. It is possible to adopt ultra small thermocouples with an external diameter of less than a millimetre as shown in [14], [15] and [15] . These extra small thermocouples can be glued directly on the chip surface, however the precision is low and the dynamic response is not good. Another solution is to use microprobes that thanks to their small dimension do not alter the thermal capacitance of the measured system [16]. Microprobes permit to achieve a good level of precision and a high level of dynamic. Placing a

thermal sensor in direct contact with the chip may cause insulation problems, thus compromising the reliability of the device. In many cases, the greater reliability obtained thanks to the knowledge of the junction temperature, is not sufficient to compensate the lower reliability due to the presence of the sensor.

2.1.2 Optical Sensors

An alternative method to directly measure the junction temperature of a semiconductor is to take advantage of the correlation between the optical proprieties of a material and its temperature. Different optical proprieties have been presented in literature like laser deflection [17], [18], luminescence, Raman spectroscopy [19], refraction index [20] , thermoreflectance [21]. Dealing with the power electronics the preferred choice is the observation of the infrared radiation. The use of the IR camera permits to thermally map the whole chip surface so that is possible to detect the presence of local hotspots [22], [23], [24]. The temperature gradient across the device is not negligible and can reach tens of degrees depending on the semiconductor technology, the chip dimensions and the load conditions. Techniques like the laser deflection permit to measure the temperature distribution inside the die. However, there are drawbacks, like the necessity to provide visual access to the die inside the module. To make the chip visible from the optical system is necessary to remove the dielectric gel and depending by the adopted technique, the surface of the die need to be treated (e.g. IR thermography requires the surface to be black painted to obtain accurate measurements). In many cases no high voltage operations can be made. Moreover, any modification to the package can affect the working conditions of the chip. An alternative solution is to place optical fibers in direct contact with the surface of the chip without removing the dielectric. However, optical fibers only allow a local temperature measurement, without being able to give any information about the temperature gradient across the chip. Most of the optical methods require a considerable amount of hardware and computational time. To conclude, optical methods, compared to other methodologies have important advantages, however their use is mostly limited to a laboratory environment. Thanks to their precision and reliability, optical methods are often used to validate temperature estimation techniques, like the ones that rely on electro-thermal models or on TSEPs.

2.2 Indirect Measurement Techniques

2.2.1 Model Based Estimate

Thermal models are powerful tools, that can be used for real-time junction temperature estimation or during the design phase of a converter. For single chip devices, a typical thermal model is usually represented using a Cauer network

Fig. 2.1(b) or a Foster network Fig. 2.1(a). The Cauer network reflects the real device structure with thermal capacitances and intermediary thermal resistances. Each layer of the power module can be represented with an RC model (chip, chip solder, substrate, and base plate). The Cauer network nodes are connected to the ground by a capacitor that represent the thermal capacitance of the layer. Each node of the network represents the temperature of the intermediate layers. The Cauer network however, is computationally complex to implement compared to the Foster network. The Foster network is composed by a series of resistors and capacitors connected in parallel, however the individual RC no longer represents the layer sequence. The network nodes have no correlation with the physical structure of the device. In fact the Foster network is a mathematical representation of the device and it has nothing to do with its physical representation. Usually, the datasheet of a device provides the transient thermal curve, from with is possible to obtain the R and C parameters of the Foster network. However, to have a precise model, the Foster network elements have to be computed experimentally. One way to do that is to measure the cooling thermal transient of the device. The analytical expression of a Foster network can be easily written in time domain (2.1) or in Laplace domain (2.2), where Z_{th} is the transient thermal impedance.

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \cdot (1 - e^{-\frac{t}{R_i \cdot C_i}}) \tag{2.1}$$

$$Z_{th}(t) = \frac{k_1}{s + p_1} + \frac{k_2}{s + p_2} + \ \ldots \frac{k_n}{s + p_n} \tag{2.2}$$

$$k_i = \frac{1}{C_1}, \quad p_i = \frac{1}{R_i \cdot C_i} \tag{2.3}$$

Typically a power module includes more than one device (e.g. MOSFETs and the antiparallel diodes) that contributes to the total heat generation. The cross coupling effect can be taken into account by adding negative RC components to the Foster network [25] and [26]. With the aging of the component there is a degradation of the thermal path and the thermal network needs to be updated. In [27] the thermal model is updated with the aging of the the component. The thermal resistance is supposed to increase linearly with the aging of the component. Although thermal capacitance is also affected by the aging of the component, its variation is significantly less than that in thermal resistance and in many cases its variation can be neglected.

Other factors can affect the thermal path. E.g. in case of liquid heatsink the thermal path depends on the flow rate of the coolant. Though the thermal path of the component is known, it is still necessary to compute the power losses of the device. The device datasheet provides the conduction and the switching losses measured under precise working conditions. E.g. The switching losses of a

MOSFET depend on the gate resistance, the junction temperature, the commutated voltage and the commutated current. It is not trivial to compute the power losses when the working condition are different from those reported in the datasheet. "Hybrid" solutions where thermal networks and other methods are used conjointly to increase the accuracy of the temperature estimation. In [26] a thermal network model and a TSEP are used conjointly.

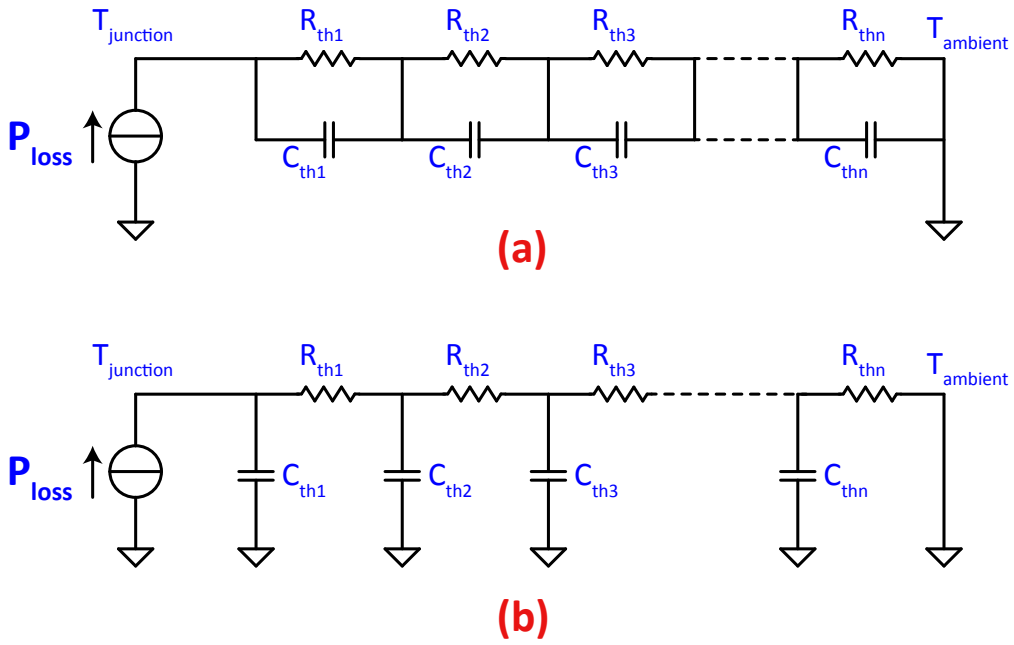


Fig. 2.1: Thermal RC models: (a) Foster network. (b) Cauer network.

2.2.2 TSEPs Parameters

TSEPs (Temperature Sensitive Electrical Parameters) based methods are one of the most promising way for estimating the junction temperature in power semiconductors [28]. Depending on the type of semiconductor different TSEPs can be used, in this section the analysis is mainly focused on N-channel power MOSFETs, however most of this techniques can be used also for IGBTs and diodes.

2.2.2.1 Low Calibrated Current Injection

A few mA current is injected into the device and the voltage drop caused by the current is measured. This is one of the most used methods because thanks to the low current injection the device self heating is negligible. This TSEP is commonly used in power electronic where most of the devices have a PN junction. For MOSFETs, it is possible to inject a calibrated current between source and drain when the semiconductor is commanded open. This permit to measure the threshold

voltage of the body diode that presents a good sensitivity with the temperature [29], [30] and [31]. An alternative solution is to inject a low current between drain and source while the MOSFET is in ON state and then to measure the variation of the conduction resistance with the temperature [29]. However, due to the power MOSFETs low ohmic resistance, the voltage drop is extremely small and hardly measurable.

2.2.2.2 Turn-ON Delay

The delay between the gate voltage signal imposed by the gate driver and the start of conduction of the device can be measured and used as a TSEP. This method can be applied to MOSFETs and IGBTs [32],[33], [34]. Different implementations are possible. E.g. In [35] V_{GE} and i_{CE} of an IGBT are monitored using two digital to analog converters. The V_{GE} rise, triggers a 100 MHz counter that is stopped when the collector current reaches a predefined level. In this example the delay time is around 1500 ns with a temperature sensitivity of 2 ns/°C. The turn-ON delay differently from the turn-OFF delay is not affected by the device current. For wide bandgap devices like SiC MOSFETs, the turn-ON delay time can be few tens of ns, in turn the time variations are hardly measurable. One solution is to slow down the commutations by increasing the gate resistance. However, this can result in an unacceptable loss of efficiency.

2.2.2.3 Turn-OFF Delay

Similarly to the turn-ON delay, also the turn-OFF delay can be used as a TSEP [35] and [36]. Differently from the turn-ON delay, this method depends on the currents in the device before the switching. In [36] the junction temperature of a SiC MOSFET (rated 1200 V and 24 A) is estimated by measuring the turn-OFF delay. When the gate resistance is zero the sensitivity of the methodology is only 0.02 ns/ °C, making the temperature estimation impossible. To increase the sensitivity the commutation has to be slowed down. In [36] the gate driver resistance is increased to 150/300 Ω, thus increasing the sensitivity by a factor of about 30/60. However, this cause also an increase of the switching losses. The proposed method uses an improved gate driver that slows down the turn-OFF only when the temperature estimation is needed. Power devices have thermal time constants of hundreds of ms, in turn it is not necessary to estimate their junction temperature at every commutation.

2.2.2.4 Saturation Current

There is a well know dependency of the electron mobility with the temperature [37], so that is possible to use the saturation current as a TSEP [38], [39], [40], [41].

The MOSFET/IGBG is commanded close with a V_{GS}/V_{GE} that is slighter higher than the threshold voltage and the resulting saturation current (i_{DS}/i_{CE}) is measured. This method, unlike others, is easy to implement because it does not require to measure currents in a very short timescale. However it can not be used during the normal operations of a converter. In turn, alternative solutions have been developed. In [42] the saturation current of a SiC MOSFET is dynamically measured. During the turn-ON the device go trough a saturation region. i_{DS} and V_{GS} are measured during the turn-ON commutation, this permits to obtain an estimation of the junction temperature during the normal converter operations. This solution can be used in hard switching converter, however it is necessary to measure voltages and currents in a very short timescale.

2.2.2.5 di/dt

The turn-ON commutation current slope can be measured and used as a TSEP [33], [35], [31]. This technique can be used with converters operating under hard switching conditions. However, it requires to measure commutation currents in a very short timescale.

2.2.2.6 High Current Injection

During the conduction state of the device, its current and its voltage drop (v_{DS} in case of MOSFET or v_{CE} in case of IGBT) can be measured. For a fixed current, the V_{ON} of the device depends on its junction temperature. However, the correlation between the voltage drop and the junction temperature is not linear. This TSEP can be used for IGBTs [43], [44] and for MOSFETs [45], [31]. In [45] a Si MOSFET DC/DC hard switching converter is presented. The V_{ON} and the i_{DS} of each MOSFETs are measured during the normal operations of the converter and the conduction resistance R_{ON} is computed. The obtained R_{ON} is then compared to a look-up table and used to estimate the junction temperature. According to [46] R_{ON} is antiproportional to the mobility of electrons μ_n. The relation between the R_{ON} and the temperature is expressed in (2.4), (2.5) and (2.6), where q is the elementary charge, N_D is the donor concentration and T is the temperature in Kelvin. Equation (2.6) shows that the R_{ON} variation with the temperatue can be represented using an exponential equation. However this is just an approximated model where the resistance of the channel is neglected, a good model should also take into account the variation of the ON-state resistance with the current. A SiC MOSFET compared to a Si MOSFET will present a smaller sensitivity of R_{ON} with the temperature. In the particular case shown in [45] the exponent of the equation is equal to 2.6 however this value can change depending on the MOSFET characteristics.

$$R_{ON} \propto \frac{1}{q\mu_n(T)N_D} \tag{2.4}$$

$$\mu_n(T) = \mu_n(300K)\left(\frac{T}{300K}\right)^{-x} \tag{2.5}$$

$$R_{ON} \propto \left(\frac{T}{300K}\right)^{x} \tag{2.6}$$

In [45] the dependency of the R_{ON} with the temperature is neglected and only the variation of the resistance with the temperature is considered, this decrease the precision of the estimation. As shown in Table 2.1 the R_{ON} is composed by the sum of different resistances, and only the n$^-$-layer follows the temperature dependency shown in (2.6). The impact of the other resistances is small if compared to the resistance of the n$^-$-layer, however the other resistances have a different thermal coefficient. Moreover, the different components of the device can be at different temperatures. E.g. The bonding wires during the normal operations of the device are likely to be at lower temperature respect to the junction and their resistance will vary according to the temperature with a coefficient that depends on the material. It is not enough to just measure the R_{ON} to estimate the junction temperature, it is necessary to have a look-up table that permits to correlate the two quantities. Usually the datasheet of the component provides $R_{ON}(T)$, however this value is usually based on the worst case scenario and the temperature estimation can became extremely inaccurate. An alternative solution is to characterize the component with the use of dedicated equipment like a curve tracer and then to place the component in the converter. This solution is not practical and the variation of the contact resistance due to the mounting process can lead to errors (few mΩ are enough to have tens of degrees of error on temperature estimation).

Table 2.1: Composition of the R_{ON} of a 600 V MOSFET [47].

Package	0.5 %
Source Layer	0.5 %
Channel	1.5 %
Accumulation Layer	0.5 %
n$^-$ Layer	96.5 %
Substrate	0.5 %

2.2.2.7 TSEPs Conclusions

The main TSEPs have been analysed, however other solutions are feasible. TSEPs based techniques can be used conjoint with a thermal model to increase

precision and reliability. Temperature estimation by TSEPs is today the most promising way to carry out measurements on packaged devices. Most of the described techniques have been developed in a laboratory environment and they are not suitable to be implemented on a commercial application. This thesis is focused on the estimation of the junction temperature for commercial applications. To estimate the junction temperature two problems need to be solved:

- TSEP measurement.
- TSEP calibration.

Measuring voltages and currents in a very short timescale can be challenging. This is the case of TSEP techniques that require to measure turn-OFF delays, turn-ON delays and current slopes (di/dt). For "slow" devices like IGBTs under certain conditions is possible to measure these quantities. However, in wide bandgap devices it is not realistic to suppose to measure currents and voltages that vary in tens of nanosecond with a discretization of less than one nanosecond. These measures are very sensitive to the parasitics and require the use of dedicated laboratory equipments like oscilloscopes and measurements probes. A possible work around is to slow down the commutations of the device, the drawback is the loss of efficiency that in most of the cases is unacceptable. Alternatively, the commutation can be slowed down only when the estimation of the junction temperature is needed as shown in [36]. This requires to design custom gate drivers and to modify the modulator. E.g. If the commutation is slowed down the death time need to be increased.

Techniques based on the injection of a low calibrated current do not require to measure currents and voltages in a very short timescale. This techniques can be used with IGBTs and diodes during the forward conduction or with MOSFETs during the interdiction state to measure the threshold voltage of the body diode. However, in most of switching converters, it is not possible to inject a calibrated current in the device during the normal operations. E.g. In a two level switching converter using power MOSFETs, it is not possible to inject a calibrated current between source and drain during the interdiction state of the device (the device is subject to the full DC-link voltage).

Techniques that require the measure of the saturation current can be used during the commutation of the device or during the conduction state. The first solution can be implemented in hard switching converters but like the previous solutions requires to measure currents and voltages in a very short timescale. The second solution require to set a small voltage between gate and the source and then to measure the saturation current, this solution is not implementable in a classical two level converter.

Techniques that require to measure the voltage drop during the conduction of a high current are feasible with regards to the acquisition time. They can be used during the normal operations of a switching converter.

To obtain a temperature estimation is necessary to calibrate the estimator, depending on the used technique the process can be more or less complex. TSEPs that have a linear temperature dependency are easier to calibrate, because they require to test the device only in a limited number of points.

Usually, the calibration process is carried out in a controlled environment with the use of calibrated equipments. To obtain a precise temperature estimation every device needs to be calibrated separately.

TSEPs are often compared in terms of sensitivity [28], [31] , however in the author's opinion these comparisons can be misleading. E.g. measuring a voltage with an error of 1% can be easy if the measurement window is on the order of µs but can be hard if the measurement window is on the order of ns. In turn, the main TSEPs based techniques have not been compared in terms of sensitivity.

2.2.3 Proposed Technique Based on V_{ON} Sampling

The main objective of this thesis is the junction temperature estimation for SiC power MOSFET modules with focus on industrial applications (power switching converters, either DC/AC or DC/DC). The proposed technique was present in [48], [49]. It utilizes the ON-state voltage measurement with high current injection illustrated in the section earlier. Starting from such well know TSEP based technique, normally used in a laboratory environment, innovative solutions are proposed in order to be able to obtain a reliable estimation of the junction temperature also in a real case scenario.

After an initial commissioning of the power module performed directly on the converter, the look-up table $\theta_J(I_{DS}, V_{ON})$ is built. This is then used for the on-line estimation and limitation of the junction temperature.

The strengths of the proposed methodology are:

- The TSEP calibration can be run directly on the converter without additional laboratory equipment like oscilloscopes and curve tracers.
- The hardware modifications are minor and easy to implement.
- The additional circuitry is low cost and off the shelf.
- Temperature detection does not affect the operation of the converter.
- Temperature detection has a fast dynamic response and high sampling rate.
- No complex computation is required.

Fig. 2.2 represents the principle of operation of the proposed V_{ON} based technique.

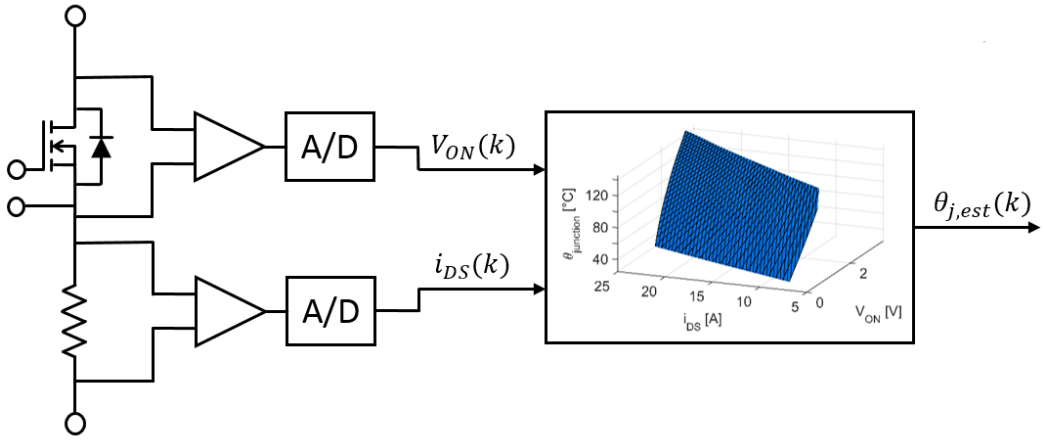


Fig. 2.2: Temperature estimator functional block using $\theta_J(V_{ON}, i_{DS})$.

Chapter 3

Proof of Concept Demonstrator

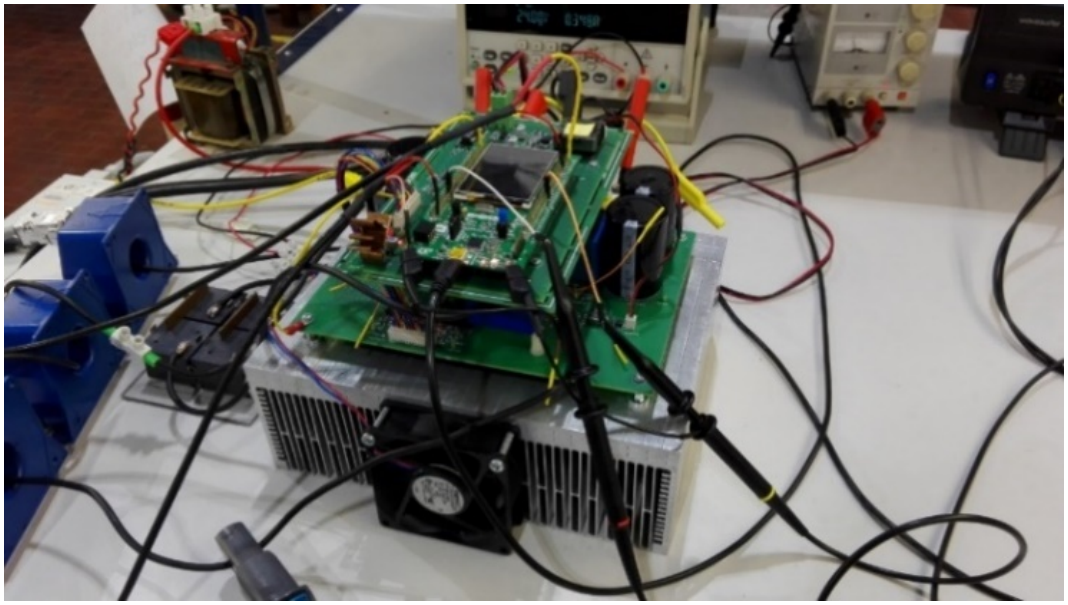


Fig. 3.1: Proof of concept demonstrator.

To validate the proposed methodology a proof of concept test rig has been designed. The converter shown in Fig. 3.1 makes use of a power module containing four SiC MOSFETs connected in H-bridge configuration. The power module operates under hard switching conditions and the junction temperature of one of the four MOSFETs is on-line estimated at every PWM period. The demonstrator permits to validate the proposed methodology while emulating real working conditions.

3.1 Power Modules Under Test

Four SiC power MOSFETs are contained in a custom "emipak-2B" package, produced by Vishay, shown in Fig. 3.2. The internal layout of the power module is shown in Fig. 3.3. The four MOSFETs are in purple. The blue label "Th" indicates the embedded NTC sensor used to measure the DBC temperature, here labelled NTC1. The two internal capacitors added to minimize the power loop stray inductance are depicted in green.

Like in most of the semiconductors used for power electronic applications, the source signal pins are separated from the source power pins. The same package with the same configuration is provided by Vishay with dies made by different manufacturers. Two different dies from two different manufacturers have been tested in this thesis.

Fig. 3.2: Power module package.

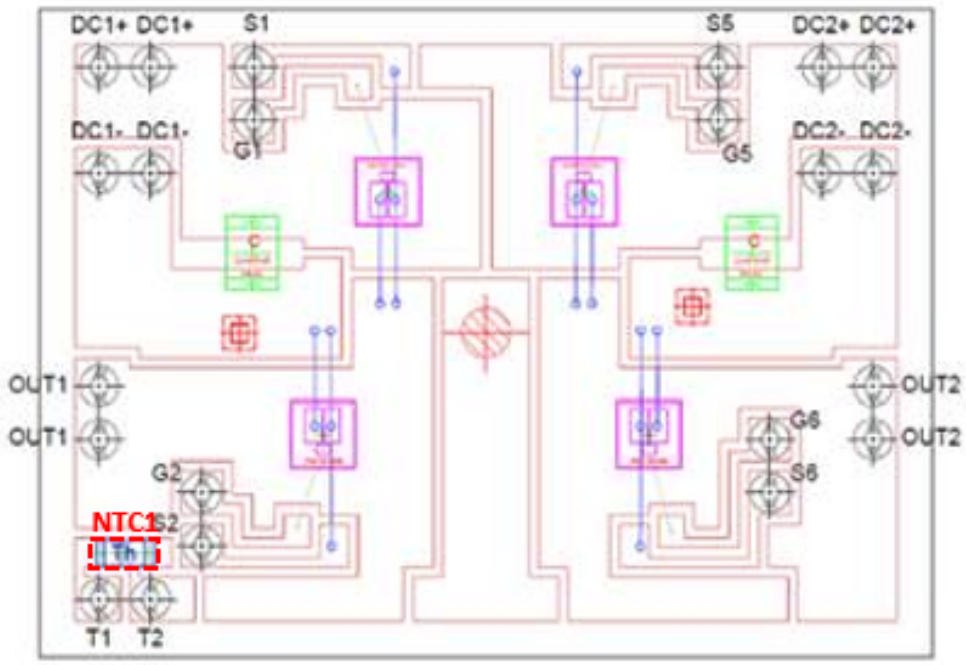


Fig. 3.3: Layout of power module (courtesy of Vishay Semiconductor Italiana). In green the two internal local capacitors. In blue the internal NTC thermistor (label "Th"), for measurement of case temperature.

The ratings of the two power modules under test are reported in Table 3.1 and Table 3.2. Both modules have a nominal breakdown voltage of 1200 V and a maximum junction temperature of 175 °C. The maximum allowable DC current for a case temperature of 80°C is 26 A for module#1 and 19 A for module#2. The typical conduction resistance for a current of 20 A and a junction temperature of 25 °C is 71 mΩ for module#1 and 78 mΩ for module#2. The R_{ON} for a drain current of 20 A and a junction temperature of 25 °C is 105 mΩ for module#1 and 103 mΩ for module#2. Even if the nominal current of the two modules is similar the dies have been made by different producers that use a different manufacturing process. The two dies show a different variation of the R_{ON} with the temperature as shown in Section 4.5. Furthermore the two dies have different switching characteristics as shown in Section 3.4.2.

Table 3.1: Power Module, type#1 (from datasheet).

Rated Current (T_{case}=80°C)	26 A
Breakdown Voltage	1200 V
R_{ON}(θ_j=25 °C, I_{DS}=20 A)	71 $m\Omega$
$C_{internal}$	2 x 47 nF
Maximum Junction Temperature	175 $°C$
C_{iss} (V_{DS}=400 V, f=1 MHz)	1700 pF
C_{oss} (V_{DS}=400 V, f=1 MHz)	130 pF
C_{rss} (V_{DS}=400 V, f=1 MHz)	25 pF

Table 3.2: Power Module, type#2 (from datasheet).

Rated Current (T_{case}=80°C)	19 A
Breakdown Voltage	1200 V
R_{ON}(θ_j=25 °C, I_{DS}=20 A)	78 $m\Omega$
$C_{internal}$	2 x 47 nF
Maximum Junction Temperature	175 $°C$
C_{iss} (V_{DS}=1000 V, f=1 MHz)	950 pF
C_{oss} (V_{DS}=1000 V, f=1 MHz)	80 pF
C_{rss} (V_{DS}=1000 V, f=1 MHz)	7.6 pF

3.2 Regenerative Test Operation

The schematic of the power section of the proposed test rig is shown in Fig. 3.5. The internal part of the power module is represented in black while external connections and components are represented in blue. The quantities shown in red are measured online at each PWM period. θ_{NTC1} represents the measure of the embedded NTC thermistor while θ_{NTC2} represents the measure of a second thermistor that has been added to validate the proposed junction temperature estimation technique as explained in Section 4.4.2. The MOSFET SW1L is fully monitored to estimate its junction temperature, it will be called also the **switch under test**. The voltage drop (v_{DS}) during the conduction state and the voltage between gate and source (v_{GS}) of the switch under test are measured for each PWM cycle. The bus voltage (v_{BUS}), the load current(i_{LOAD}) and the switches currents (i_{SW1L} and i_{SW2L}) are also measured. i_{LOAD} is measured through a closed loop hall sensor while i_{SW1L} and i_{SW2L} are measured through two shunt resistors that permit to achieve a higher measurement bandwidth. Due to the presence of the power module internal

capacitance, the shunt resistors can't measure exactly the current in the switches especially during the commutations. However when the turn-ON transitory is over, the current flowing in the internal capacitances respect to the current flowing in the shunt resistors is negligible. The power module is connected in H-bridge configuration and it is supplying a purely inductive load. The current in the LOAD is closed-loop controlled by LEG2 while LEG1 is open loop controlled at a fixed duty-cycle to emulate a constant voltage source. The control schematic is shown in Fig. 3.4.

The average current in the switch under test is:

$$I_{SW1L} = I_{LOAD}\,(1 - D_1) \tag{3.1}$$

The instantaneous current in the switch under test is:

$$i_{SW1L}(t) = i_{LOAD} \cdot q_{1L} \tag{3.2}$$

This configuration permits to mimic real operating conditions while absorbing from the DC-link just a fraction of the output power. The DC power source needs to provide only the losses of the system, this permits to test high current power modules without the need of an expensive high current power supply. Moreover this configuration permits to do some considerations on the efficiency of the system by measuring only the input power to the DC-link.

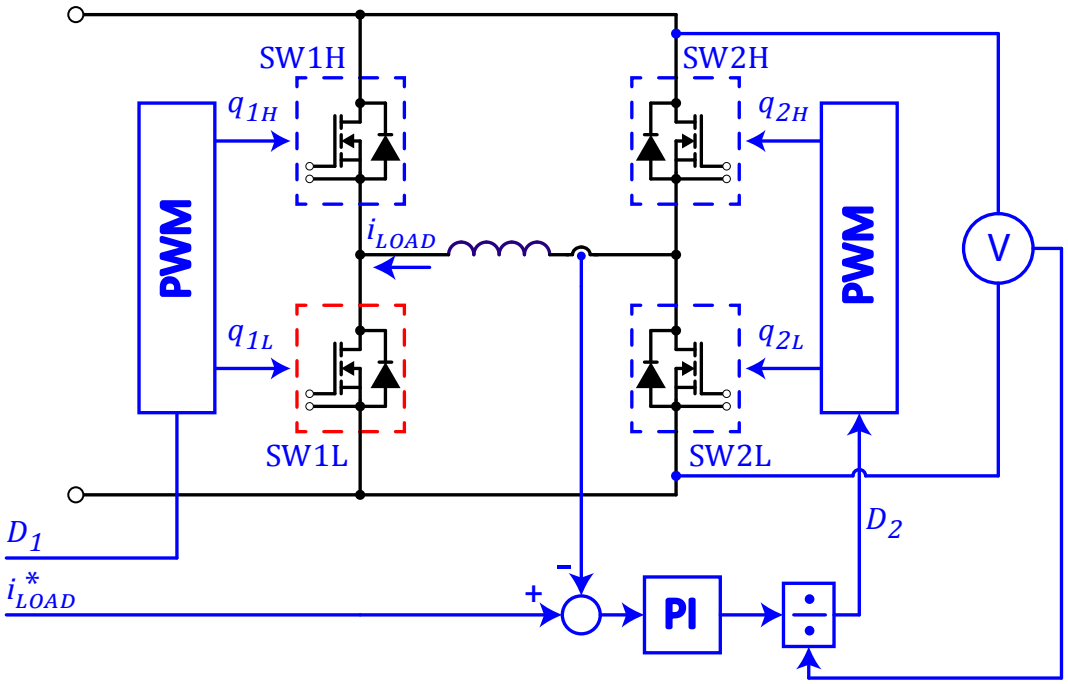


Fig. 3.4: Control schematic. LEG1 is open-loop controlled while LEG2 is used in closed-loop current control.

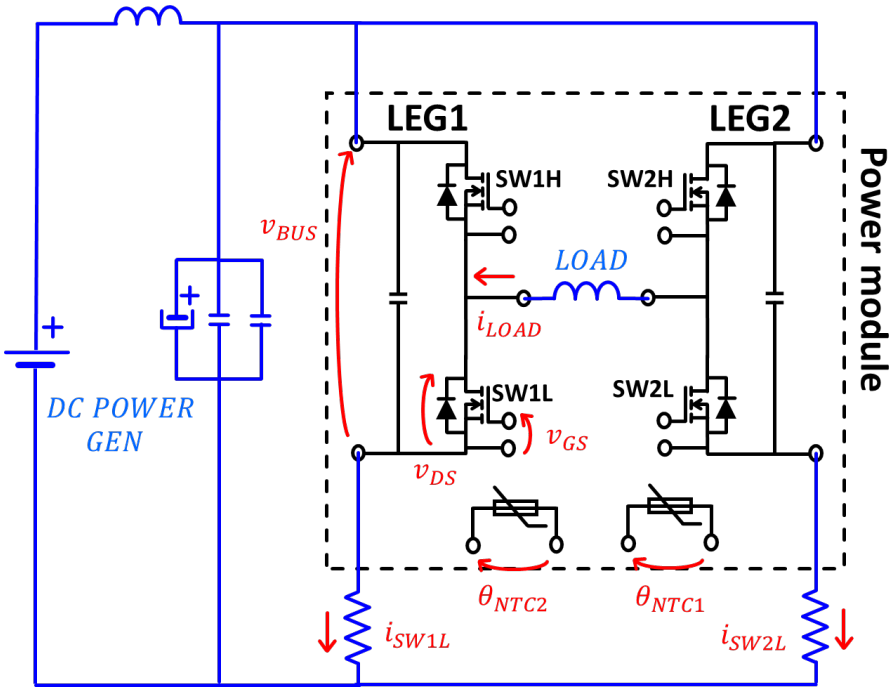


Fig. 3.5: Schematic diagram of the proposed setup: red quantities are measured online.

3.3 3D Layout

Fig. 3.6 shows the 3D-layout of the test rig. From top to bottom, the control board, the two driver boards, the power board, the power module and part of the heatsink are visible. The heatsink is better visible in Fig. 3.1. This arrangement was chosen to keep the gate driver circuitry and the measurement circuitry as close as possible to the pins of the power module. In turn, this layout minimizes the parasitic inductance of the gate-driver circuitry.

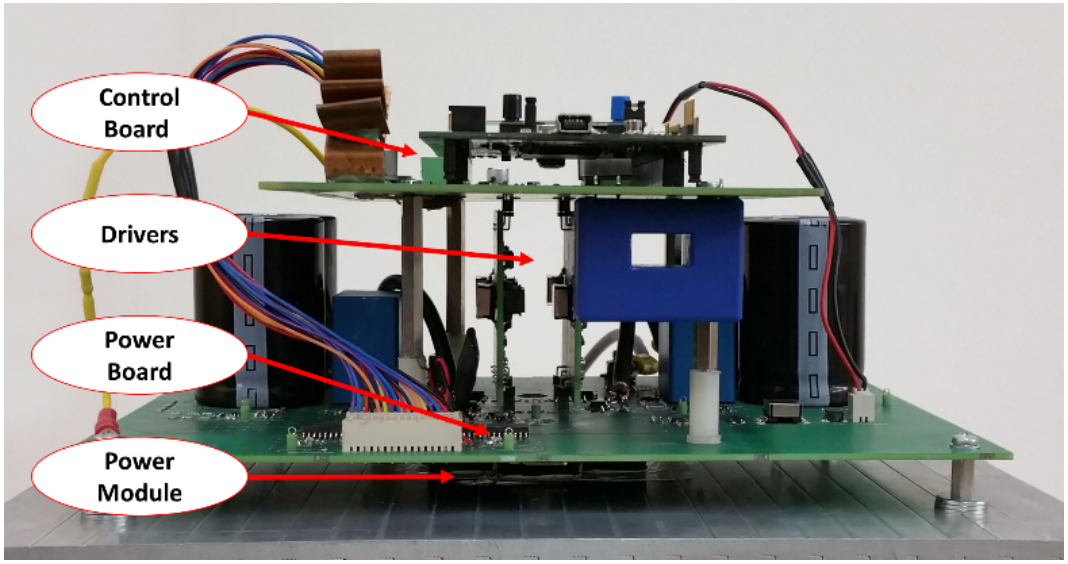


Fig. 3.6: Overview of the proposed setup.

3.3.1 Control Board

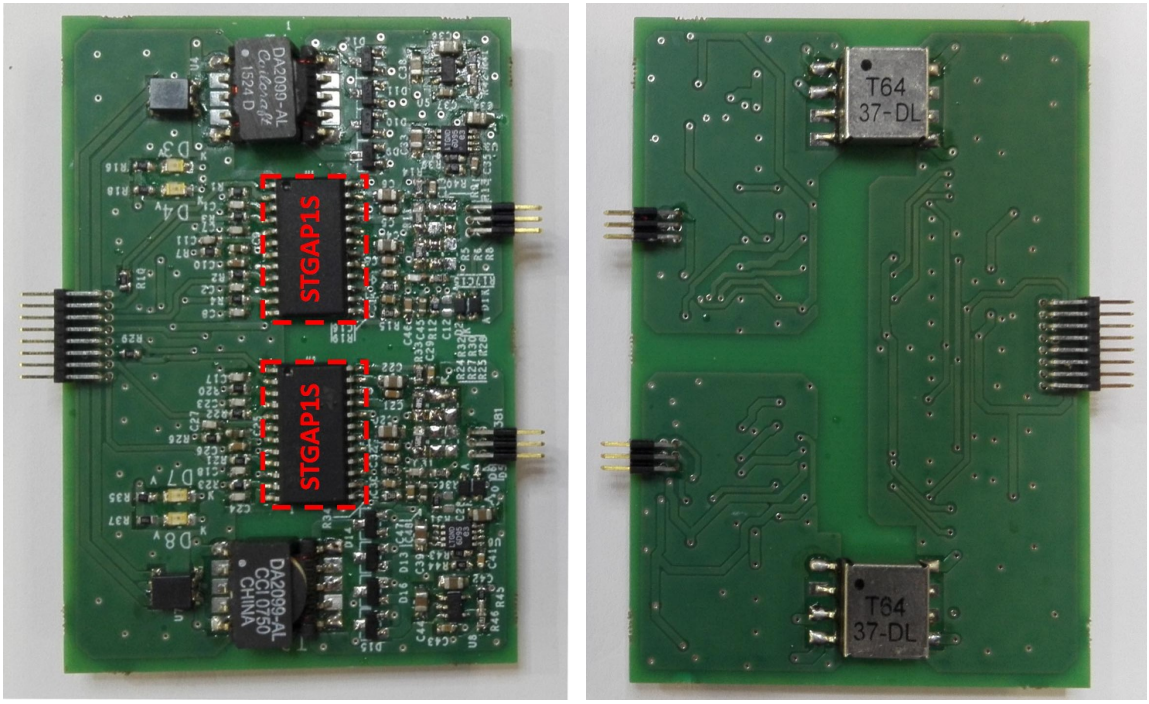
The control board houses the development board STM32F429-Discovery by STMicroelectronics. The development board comes with the STM32F429ZI microcontroller, embedding an ARM M4-core with clock frequency up to 180 MHz. This microcontroller is meant for industry applications. The Discovery board houses also a 64 Mbit SDRAM memory used as a buffer during PC communications and a debugger/programmer interface (ST-LINK/V2) provided by STMicroelectronics. The choice of using a development board permitted to save time and money when designing the PCB. The control board houses the closed-loop Hall effect current transducer used to closed-loop control i_{LOAD} as shown in Fig. 3.5. The signal coming from the current sensor and the embedded NTC1 are sampled using the ADCs of the microcontroller.

A 100 kHz SWPS (Switched Mode Power Supply) is used to supply an high frequency bus. Such high frequency bus provides insulated power supply to the gate-drive circuitry and to the measurement systems.

Fig. 3.7: Overview of the control board.

3.3.2 Driver Boards

Two driver boards, one for each leg of the module are present. Each driver board contains two independent STGAP1S gate drivers. The STGAP1S is a isolated, single gate-driver with a output current capability of 5 A and common mode transient immunity of 50 kV/µs. The driver output is rail-to-rail and can provide negative voltages. The SiC MOSFETs under test are driven by a V_{GS} ranging +20 V and -5 V. The device can be programmed and monitored through an SPI line. Advanced protections are available such as two level turn-OFF, Miller clamp, desaturation detection, 2-level turn-OFF, v_{DS} over voltage protection. The ability to program via SPI the protection threshold levels can be useful when different devices are tested. E.g. When a different power module is tested, it is possible to modify the level of intervention of the desaturation protection. Insulated supply is provided by the HF SMPS as said.



(a) Top view. (b) Bottom view.

Fig. 3.8: Overview of the driver board.

Table 3.3: STGAP1S main features.

Maximum isolation working voltage	1500 V
Maximum transient overvoltage	4000 V
Driver current capability	5 A
Transient Immunity	50 $kV/\mu s$
Input/output propagation delay	100 ns

3.3.3 Power Board

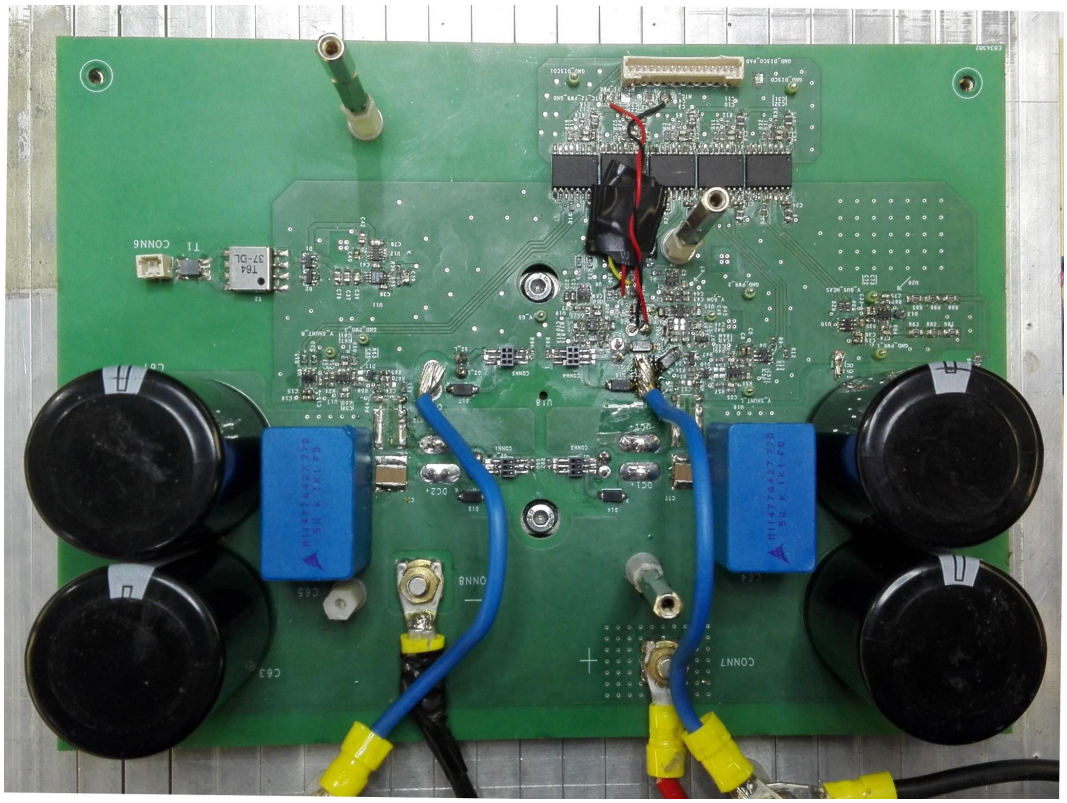


Fig. 3.9: Overview of the driver board.

The power board shown in Fig. 3.9 houses the DC-link capacitors and the measurement systems. When wide-bandgap devices are used special care has to be paid to the parasitic inductances of the DC-link. To avoid over-voltages and resonances during the commutations, the DC-link capacitors have to be placed as close as possible to power module DC pins (Fig. 3.3). As shown in Fig. 3.9 three types of capacitors have been used.

Electrolitic caps (black cylindrical, two per side) film caps (blue one for side) and ceramic caps (SMD, oner per side).

Ceramic capacitors have a high resonance frequency and a low ESR, thus enable to filter the high frequency components due to the commutation. Electrolytic capacitors allow to achieve high values of capacitance (they have a higher energy density respect to ceramic capacitors), however when compared to ceramic capacitors they have a higher ESR and a lower resonance frequency. Electrolitic capacitors can be used to filter low frequency components, moreover their "high" ESR can help to dump current oscillations of the DC-link. Film capacitors have features that are on the middle between a ceramic and an electrolytic capacitor.

Overall, the power board hosts two ceramic capacitors model C2225X154KDRACTU (Table 3.6) with a total capacitance of 300 nF, two film capacitors model B32774D0505K000 (Table 3.5) with a total capacitance of 10 µF and four electrolytic capacitors model B43544A5567M000 (Table 3.4) connected two by two in series with a total capacitance of 560 µF.

With reference to Fig. 3.5 the measured quantities v_{BUS}, i_{SW1L}, i_{SW2L}, v_{GS} and v_{DS} are sampled using 12 bit ADCs placed on the power board and then transmitted to the control board via dedicated opto-isolated SPI channels. The measurement system has been placed as close as possible to the source of the signal to be sampled in order to improve its noise immunity. This aspect is really important when working with wide-bandgap semiconductors that can generate strong EMI emissions. Each ADC has its own analog conditioning circuitry, but only the one used to measure v_{DS} will be examined in detail in Section 3.3.5. The measurement systems is supplied by the HF SMPS.

Table 3.4: Electrolytic capacitor.

Model	B43544A5567M000
Manufacturer	EPCOS
Nominal Capacitance	560 µF
Nominal Voltage	450 V
ESR$_{typ}$(f=100 Hz)	180 $m\Omega$
Z$_{max}$(f=10 kHz)	280 $m\Omega$
N$_{capacitors}$	4

Table 3.5: Film capacitor.

Model	B32774D0505K000
Manufacturer	TDK
Nominal Capacitance	5 µF
Nominal Voltage	1100 V
ESR$_{typ}$(f=10 kHz)	10.9 $m\Omega$
ESL$_{typ}$(f=10 kHz)	27 nH
N$_{capacitors}$	2

Table 3.6: Ceramic capacitor.

Model	C2225X154KDRACTU
Manufacturer	KEMET
Nominal Capacitance	150 nF
Nominal Voltage	1000 V
Dielectric	X7R
$\mathbf{N_{capacitors}}$	2

3.3.4 Heatsink with Resistors and Inductors Load

The heatsink, the four heating resistors and the load inductors are visible in Fig. 3.10. The heatsink is purposely oversized: this configuration allows a large "thermal inertia". Two additional cooling fans are (not visible in the figure) are mounted on the heatsink. The four heating resistors are supplied using an external power source. They can be used to heat the heatsink during the commissioning test of the power module, as will be addressed in the next chapter. Up to eight ferrite core inductors (model AGP4233-223ME) can be connected in series and used as the load of the regenerative H-bridge. The specifications of the inductors, produced by Coilcraft, are reported in Table 3.7.

Table 3.7: Ferrite Inductor.

Model	AGP4233-223ME
Manufacturer	COILCRAFT
Nominal Inductance	22 µH
$\mathbf{I_{SAT}}$**(10% drop)**	32.8 A
$\mathbf{I_{RMS}}$**(40°C rise)**	34 A
Nominal DC Resistance	2.8 $m\Omega$
Self Resonant Frequency	12 MHz
$\mathbf{N_{inductors}}$	$1-8$

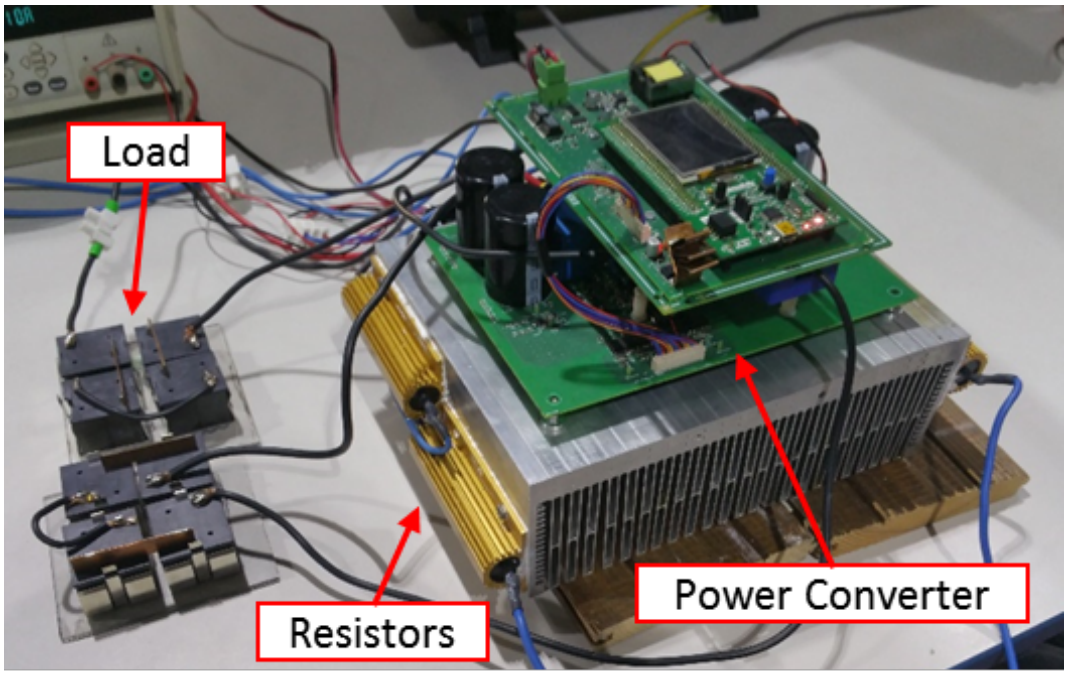


Fig. 3.10: Heatsink with four heating resistors (two on the left side and two on the right side) and the inductive load composed of eight ferrite inductors. The two additional cooling fans are on the back of the heatsink (not visible in figure).

3.3.5 V_{ON} Measurement System

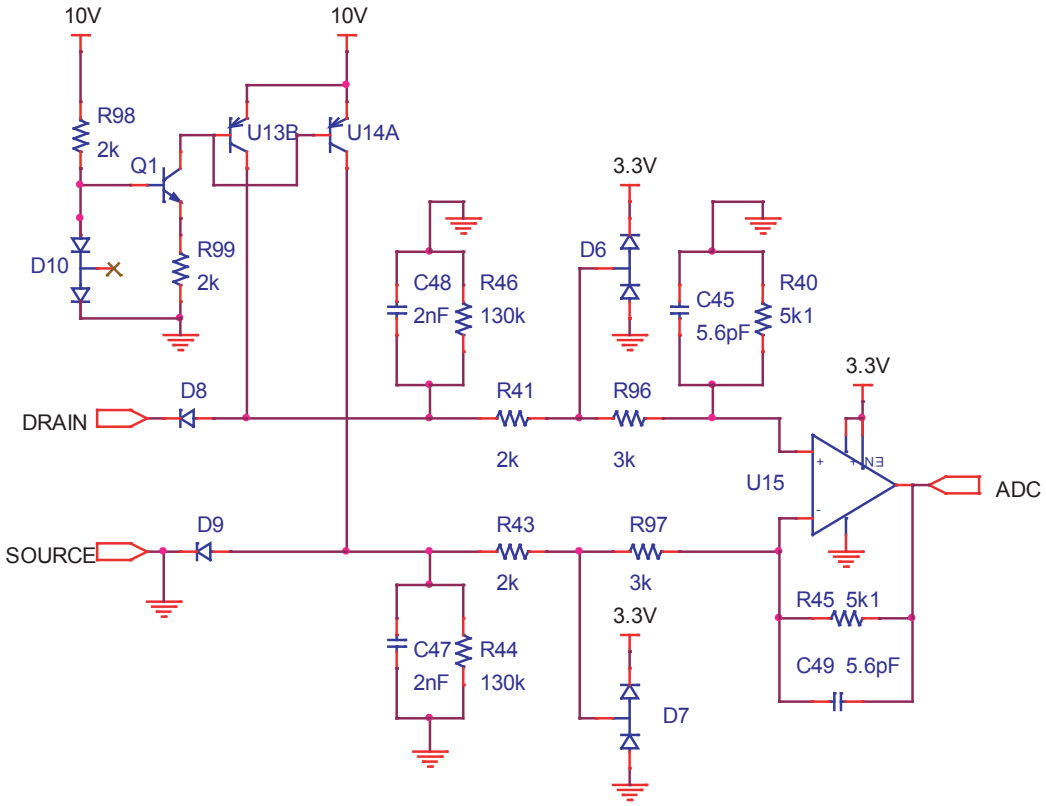


Fig. 3.11: Schematic of the analog conditioning stage dedicated to the V_{ON} measurement.

Special care has to be paid to the system for measuring the voltage drop of the MOSFET SW1L during his conduction state. The analog signal conditioning system consists of an operational amplifier in differential configuration. The gain of the system can be analytically computed:

$$G_{DS} = \frac{V_{ADC}}{V_{DRAIN} - V_{SOURCE}} = \frac{R_{45}}{R_{97} + R_{43}} = \frac{5100}{2000 + 3000} = 1.02 \qquad (3.3)$$

The two feedback capacitors (C49-C45) low-pass filter the V_{ON}= $V_D - V_S$ signal, with a cut off frequency of:

$$f_{cut-off,VON} = \frac{1}{2\pi R_{45} C_{49}} = \frac{1}{2\pi \cdot 5100 \cdot 5.6e-12} = 5\ MHz \qquad (3.4)$$

A second RC filter (not visible in the schematic) has been placed between the analog output of the operational amplifier and the analog to digital converter. The cut of frequency of the RC filter is:

$$f_{cut-off,out} = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 56 \cdot 270e-12} = 10.5\ MHz \tag{3.5}$$

The diode D8 protects the analog circuitry from the high voltage: when SW1L is in ON-state v_{DS} is few volts, however when it is in OFF-state the v_{DS} rise up to the DC-link voltage. A second diode D9 was added to compensate the voltage drop of diode D8. When SW1L is ON the two diodes are polarized with the same current by a mirrored current generator. The npn transistor (Q1) acts as a current reference while the two matched pnp transistors (U13B U13A) act as a current mirror.

The diodes D6 and D7 further protect the input of the operational amplifier by clamping the input voltage. Indeed, when SW1L is OFF the anode voltage of D8 rise to 10 V.

During the turn-OFF of SW1L the v_{DS} varies quickly and the diode D8 gets reverse biased, injecting an impulsive current in the measurement system because of the reverse recovery and the parasitics. The capacitors C48, C47, and the resistors R44 and R46 act as "dampers", avoiding the propagation of the noise to the other measurement systems.

The analog output of the measurement system is read by a 12-bit ADC model AD7276, placed in the immediate proximity of the analog conditioning circuit. The ADC transmits the acquired data to the control board through a galvanic insulate SPI.

This measurement system can sample only positive values of V_{ON}, an improved version able to sample also negative values of V_{ON} is presented in Section 6.2.7.

In Fig. 3.13 the A/D converter input has been measured when SW1L is operating at 50% duty cycle (f_{sw}=10 kHz). V_{ON} is sampled in correspondence of the blue arrows. The output of the operational amplifier alternates between linear state (SW1L ON) and saturation state (SW1L OFF).

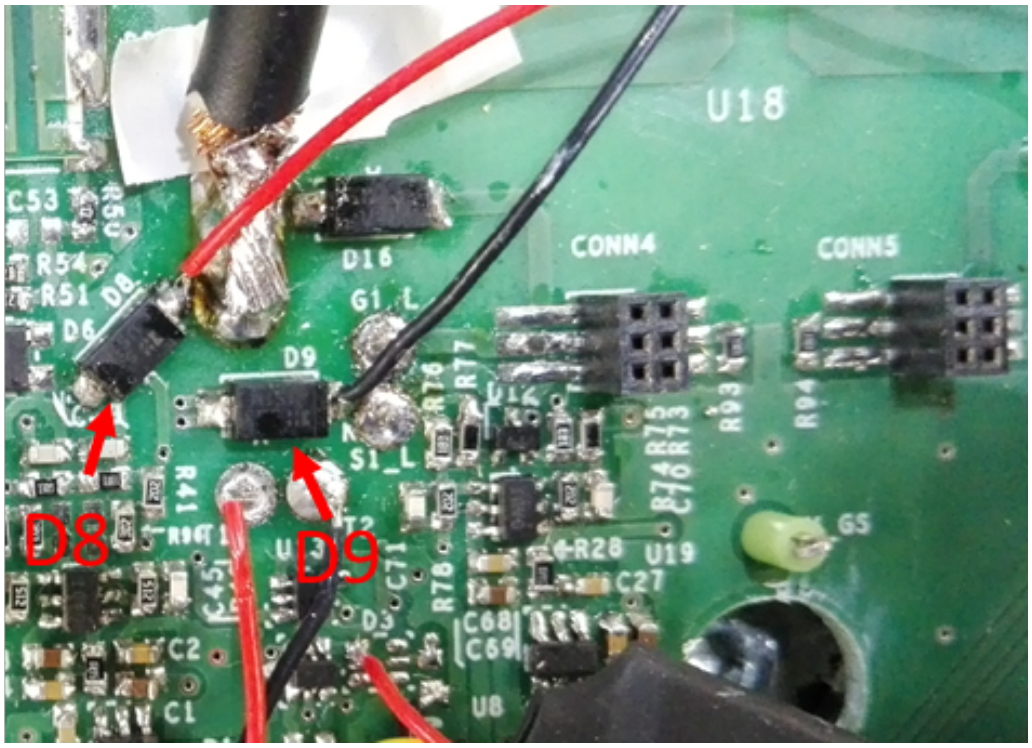


Fig. 3.12: Detail of the PCB board with the two diodes very close to eachother.

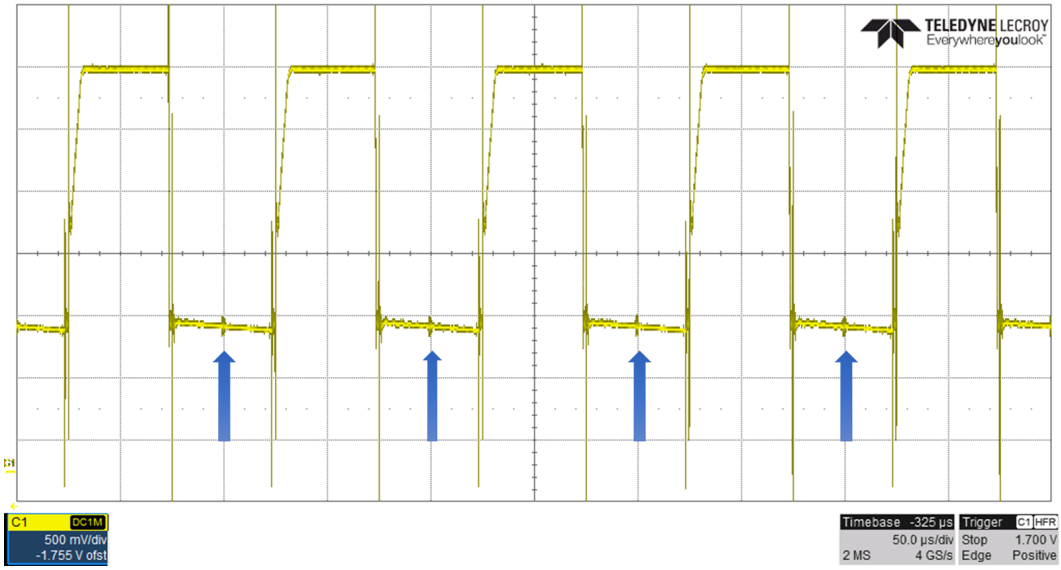


Fig. 3.13: Input voltage to the A/D converter. $V_{A/D}$=500 mV/div t=50 µs/div

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3.4 EMI Aspects

3.4.1 High dv/dt Related Problems

SiC power MOSFETs permit to reduce drastically the commutation losses by reducing the switching times. However high dv/dt may cause problems like: switching over voltages, electromagnetic emissions, line reflections and so on. When long cables or electrical machines are used conjoint to wide-bandgap devices additional problems can occur. Electrical machines can suffer from common mode currents, partial discharges in the windings and premature aging of the insulations [50], [51]. If power converter is connected to the load through a long cable, then over voltages due to the fast switching transients are generated at the end of the cable [52], [53].

3.4.2 dv/dt Analysis

Part of this analysis was presented in [54]. Module#1 and module#2 have been tested with different values of gate resistance. To obtain an accurate measurement at high bandwidth, two single ended probes have been connected respectively to the source and to the drain of SW1L. The two grounds of the single ended probes have been connected to the negative pole of the DC bus. The voltages reported in Fig. 3.14,Fig. 3.15, Fig. 3.16 and Fig. 3.17 have been obtained by subtracting the measured voltages by the two probes. Fig. 3.14 and Fig. 3.16 show the voltage commutations of the switch SW1L of module#1 at turn-OFF and at turn-ON. Fig. 3.15 and Fig. 3.17 show the voltage commutations of the switch SW1L of module#2 at turn-OFF and at turn-ON. The maximum voltage slew rate at turn-ON and at turn-OFF has been examined, the obtained results have been summarized in TableTable 3.8. The tests have been carried with a DC-link voltage of 520 V. The maximum slew rate voltage for module#1 is about 31 kV/µs, it has been obtained during turn-ON with a drain current of 10 A and a gate resistance of 5 Ω. The maximum slew rate voltage for module#2 is about 50.5 kV µs, it has been obtained during the turn-ON with a drain current of 5 A and a gate resistor of 15 Ω. Lower values of gate resistance where tested on module#2 but the gate driver went in fault state due to the excessive voltage slew rate. According to Table 3.3 the maximum transient immunity of the installed gate driver is 50 kV/µs. Thanks to the embedded internal capacitor and to the good design of the DC-link, over voltages are limited. The only case when there is a significant over voltage is during the turn-OFF of module#2 with a gate resistance of 15 Ω and a drain current of 25 A . In this case as shown in Fig. 3.15 the peak voltage during the turn-OFF reached 630 V corresponding to an over voltage of 110 V. Also the turn-ON can be critical, Fig. 3.17, shows that module#2 during the turn-ON commutation with a drain current of 25 A and a gate resistance of 15 Ω experience resonance phenomena. These resonances are likely due to the reverse recovery of the body diode of the MOSFET

SW1H.

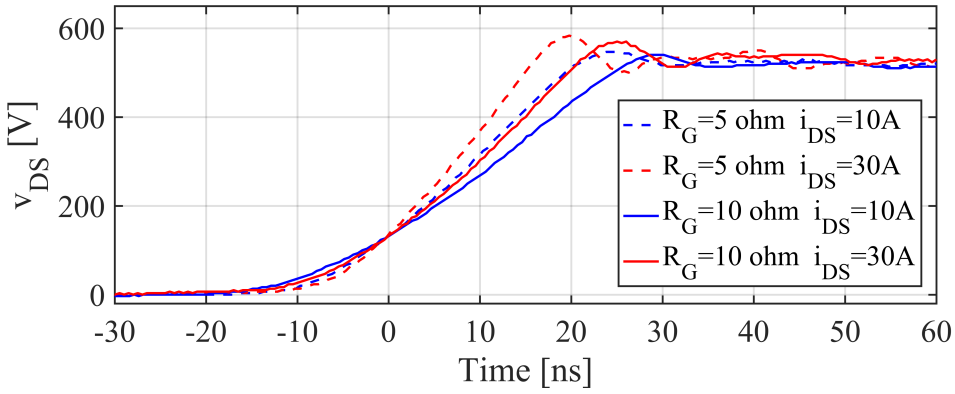


Fig. 3.14: Module#1 turn-OFF, behavior of v_{DS} for different values of gate resistor.

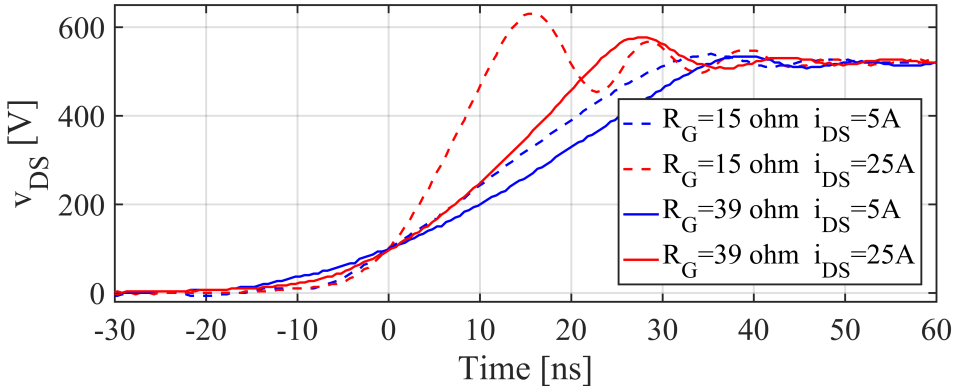


Fig. 3.15: Module#2 turn-OFF, behavior of v_{DS} for different values of gate resistor.

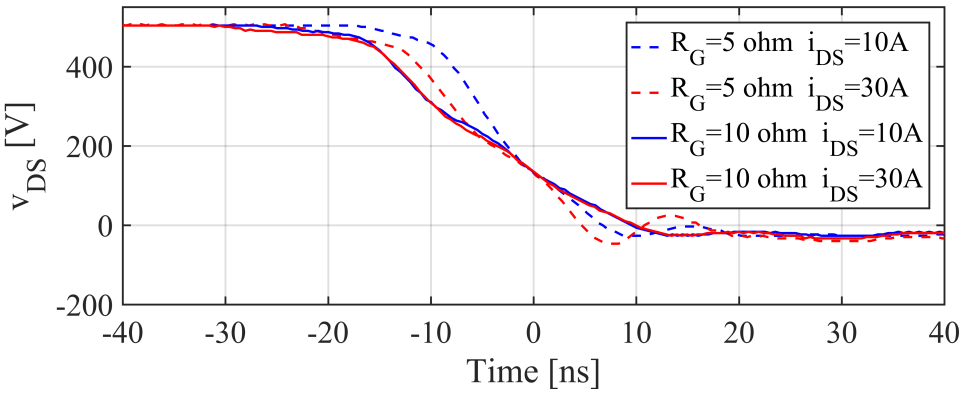


Fig. 3.16: Module#1 turn-ON, behavior of v_{DS} for different values of gate resistor.

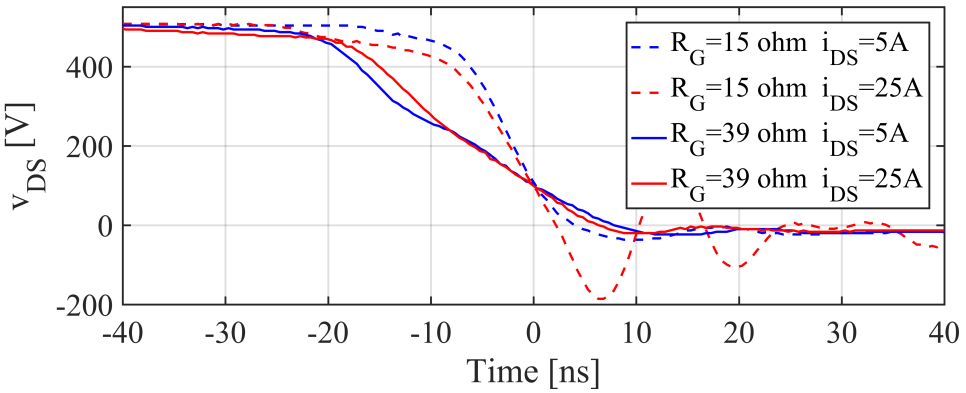


Fig. 3.17: Module#2 turn-ON, behavior of v_{DS} for different values of gate resistor.

Power Module #1		
Turn-ON	Rg=10 Ω	19.5 kV/µs (10 A) //// 19.5 kV/µs (30 A)
	Rg=5 Ω	31 kV/µs (10 A) //// 24 kV/µs (30 A)
Turn-OFF	Rg=10 Ω	14.5 kV/µs (10 A) //// 17.5 kV/µs (30 A)
	Rg=5 Ω	18 kV/µs (10 A) //// 23 kV/µs (30 A)
Power Module #2		
Turn-ON	Rg=39 Ω	17 kV/µs (5 A) //// 20.5 kV/µs (25 A)
	Rg=15 Ω	50.5 kV/µs (5 A) //// 41.5 kV/µs (25 A)
Turn-OFF	Rg=39 Ω	12.5 kV/µs (5 A) //// 18 kV/µs (25 A)
	Rg=15 Ω	15.5 kV/µs (5 A) //// 37.2 kV/µs (25 A)

Table 3.8: Summary results collected dv/dt test. Maximum dv/dt for the two modules under test, measured at different values of drain current.

Chapter 4

Results from POC Demostrator

4.1 Commissioning Test

The commissioning test permits to obtain the table $\theta_J(i_{DS}, V_{ON})$ of the MOSFET SW1L (switch under test), that can then be used for the on-line junction temperature estimation during the normal operations of the converter.

4.1.1 Commissioning Test Description

The characterization of the switch under test is done by imposing a series of short current pulses to the load at different junction temperatures. The short duration of the current pulses ensures that the junction temperature does not vary significantly respect to the DBC temperature (as described in Section 4.1.2). For module#1 35 current pulses from 1 A to 35 A are imposed, while for module#2 28 current pulses from 1 A to 28 A are imposed. The current pulses are imposed for different temperatures values, from 145 °C to room temperature.

The commissioning test can be summarized as follows:

1. The heatsink is heated using the external resistors shown in Fig. 3.10. When the temperature measured by the embedded NTC1 sensor reaches 145°C the resistors are turned OFF and the heatsink starts cooling naturally.

2. A set of current pulses (Fig. 4.1) of short duration and of growing amplitude from 1 A to the maximum target current is imposed by the converter to the load and thus to the switch under test SW1L.

3. When the temperature measured with the NTC1 drops by 5°C the control algorithm automatically executes a new set of current pulses.

4. The test stops when the heatsink reaches the room temperature.

The total duration of the commissioning test for this setup is around 20 minutes, as the temperature lowers the cooling process slows down, so the fans on the heat sink can be turned-ON to speed up the cooling process. Fig. 4.2 shows the obtained samples from the commissioning of module#2. Starting from the top, the first plot shows the junction temperature that thanks to the short duration of the current pulses can be considered equal to the temperature of the DBC (measured by NTC1). The second plot shows the V_{ON} samples corresponding to the current samples reported in the third plot. The R_{ON} correspondent to each operating point can be easily obtained dividing the V_{ON} for the corresponding drain current.

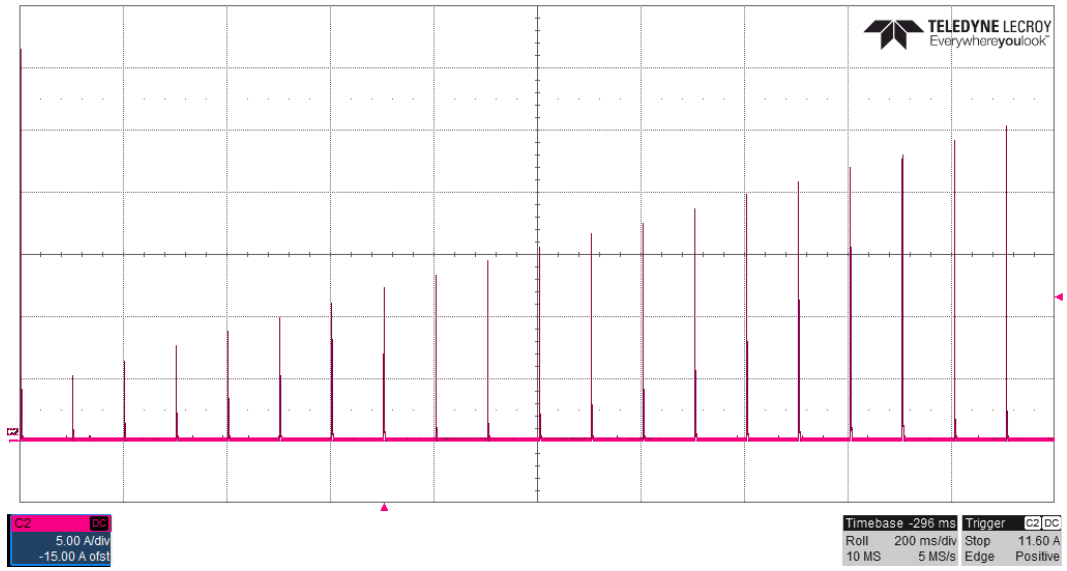


Fig. 4.1: Impulsive current test for mapping the MOSFET under test. The current pulses are equally distributed in time, one pulse every 100 ms. The current pulses are of growing amplitude from 1 A up to the maximum target current. i_{SW1L}=5 A/div t=200 ms/div.

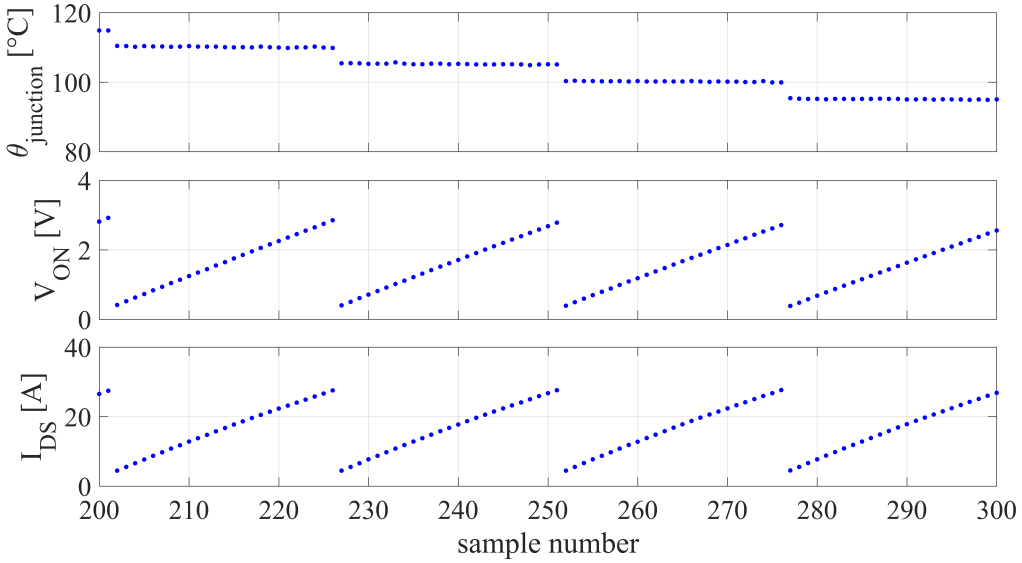


Fig. 4.2: Results of the commissioning: 28 current and voltage values per temperature value.

4.1.2 Difference between θ_J and NTC Measurement

As said, the short duration of the current pulses ensures that during the commissioning test θ_J of the switch under test equals the temperature of the DBC. The following considerations apply to module#2, but similar ones can be made for module#1. The junction temperature rise due to the current pulse test is evaluated in the worst case scenario conditions, where i_{DS} is 28 A and θ_J is 145 °C. For this test the modulation frequency is 10 kHz, the load inductance is 88 µH and the v_{BUS} is 75 V. Fig. 4.3 shows the load current during one current pulse identification. For purpose of presentation, the current pulse test has been divided into sectors. The switches configurations correspondent to the different sectors are shown in Fig. 4.4. The switch SW1L is in conduction in sectors 1,3 and 4. In sectors 1 and 3, the load is subject to the full DC-link voltage, and the load current rises quickly. In sectors 2 and 4 the load current is free-wheeling and remains circa constant. The V_{ON} and the i_{DS} of the switch SW1L are sampled at time SP1. Shortly after the end of sector 4, all the switches are turned-OFF and the load current returns to zero. The underlying simplifying assumptions are:

- The R_{ON} of SW1L is constant in each sector.
- The timespan of sectors 1 and 3 is conservatively considered T/4.
- Switching losses are negligible as the pulse test has been conducted at a reduced v_{BUS} voltage of 75 V.

In sector 1 the load current rises from 0 A to 14 A with a ramp shape. In this sector the resistance is supposed to be 0.143 Ω, computed from the datasheet curves shown in Fig. 4.5, at 14 A. The losses in the switch SW1L for this sector are 0.233 mJ as shown in (4.1).

$$\begin{aligned} E_{loss,1} &= \int_0^{T/4} R_{14A} \cdot i^2 \, dt \\ &= R_{14A} \cdot \int_0^{T/4} \frac{I_{T/4}}{T/4} \cdot t \, dt \\ &= R_{14A} \cdot \frac{1}{3} \cdot I_{T/4}^2 \cdot \frac{T}{4} \\ &= 0.143 \cdot \frac{1}{3} \cdot 14^2 \cdot \frac{100 \cdot 10^{-6}}{4} = 0.233 \; mJ \end{aligned} \tag{4.1}$$

In sector 3 the current ramps from 14 A to 28 A . The R_{ON} for this sector is 0.161 Ω, again from datasheet, at 28 A. The losses in the switch SW1L for this sector are 1.84 mJ as shown in (4.2).

$$\begin{aligned} E_{loss,3} &= \int_0^{T/4} R_{28A} \cdot i^2 \, dt \\ &= R_{28A} \cdot \int_0^{T/4} (I_0 + \frac{I_{T/4} - I_0}{T/4} \cdot t)^2 \, dt \\ &= R_{28A} \cdot \frac{T}{4} \cdot \left(I_0^2 + \frac{1}{3} \cdot (I_{T/4} - I_0)^2 \cdot + I_0 \cdot (I_{T/4} - I_0) \right) \\ &= 0.161 \cdot \frac{100 \cdot 10^{-6}}{4} \cdot \left(14^2 + \frac{1}{3} \cdot (28 - 14)^2 + 14 \cdot (28 - 14) \right) \\ &= 1.84 \; mJ \end{aligned} \tag{4.2}$$

In sector 4 the current is constant at 28 A. The R_{ON} remains the same. The losses in the switch SW1L for this sector are 1.58 mJ as shown in (4.3).

$$\begin{aligned} E_{loss,4} &= \int_0^{T/8} R_{28A} \cdot i^2 \, dt \\ &= R_{28A} \cdot \int_0^{T/8} I_{T/8}^2 \, dt \\ &= R_{28A} \cdot \frac{T}{8} \cdot I_{T/8}^2 \\ &= 0.161 \cdot \frac{100 \cdot 10^{-6}}{8} \cdot 28^2 = 1.58 \; mJ \end{aligned} \tag{4.3}$$

Altogether, 3.65 mJ of losses are generated in 68 µs. Fig. 4.6 shows the characteristic of the transient thermal impedance reported in the datasheet of module#2.

The transient thermal impedance for a DC pulse duration of 68 µs is 0.03 °C/W. Therefore, the junction temperature rise after the 28 A pulse test equals 1.75 °C.

$$\begin{aligned}\Delta\theta_{j,SW1L} &= \frac{E_{loss,1} + E_{loss,3} + E_{loss,4}}{5/8 \cdot T} \cdot Z_{th,62\mu s} \\ &= \frac{(0.233 + 1.84 + 1.58) \cdot 10^{-3}}{62.5 \cdot 10^{-6}} \cdot 0.03 = 1.75\ ^{\circ}C \end{aligned} \tag{4.4}$$

Between this current pulse and the next one there is an idle time of at least 100 ms, so to cancel any residual temperature perturbation. This ensures that θ_J returns to the $\theta_{DBC} = \theta_{NTC1}$, before the next pulse occurs.

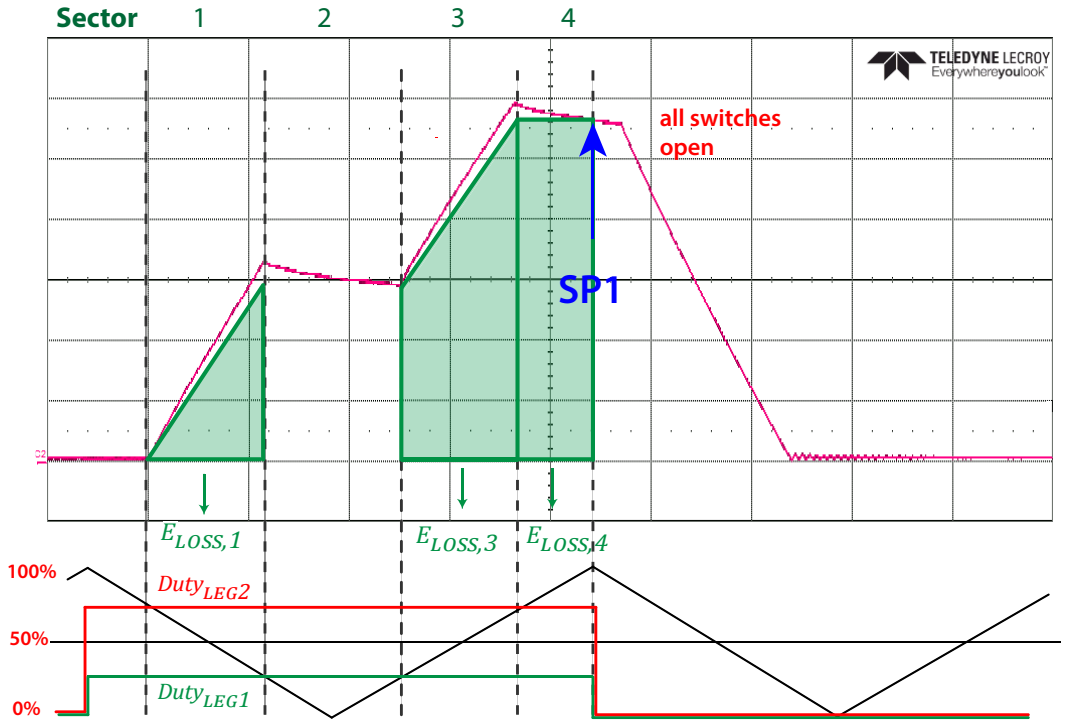


Fig. 4.3: Top: load current during the current pulse test at 28 A. ($i_S W1L$=5 A/div t=20 µs/div.) Bottom: corresponding reference duty cycles and triangular carrier.

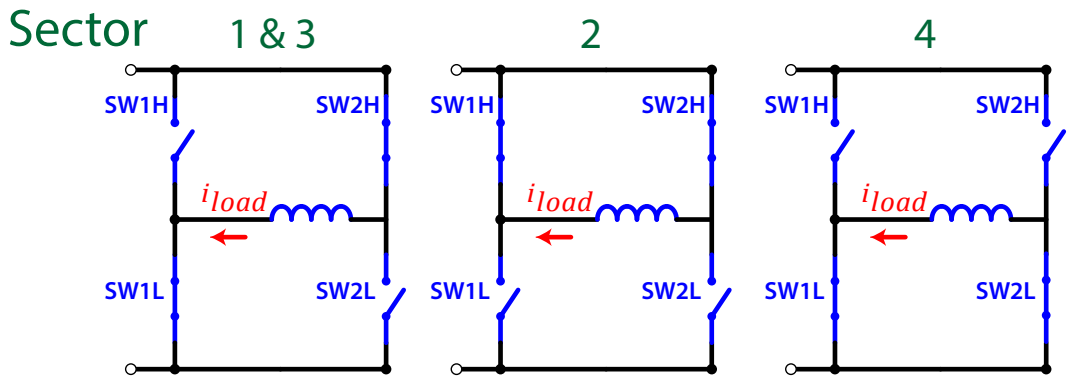


Fig. 4.4: H-bridge switches state.

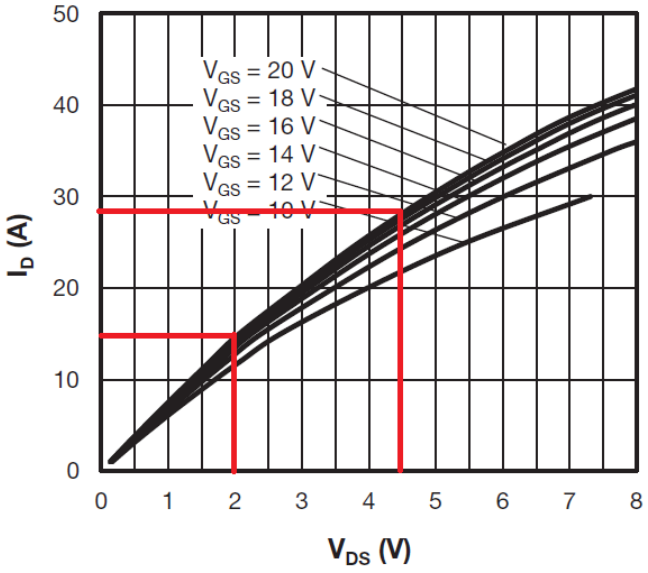


Fig. 4.5: Typical Drain-to-Source current output characteristics at θ_J= 150 °C (courtesy of Vishay Semiconductor Italiana).

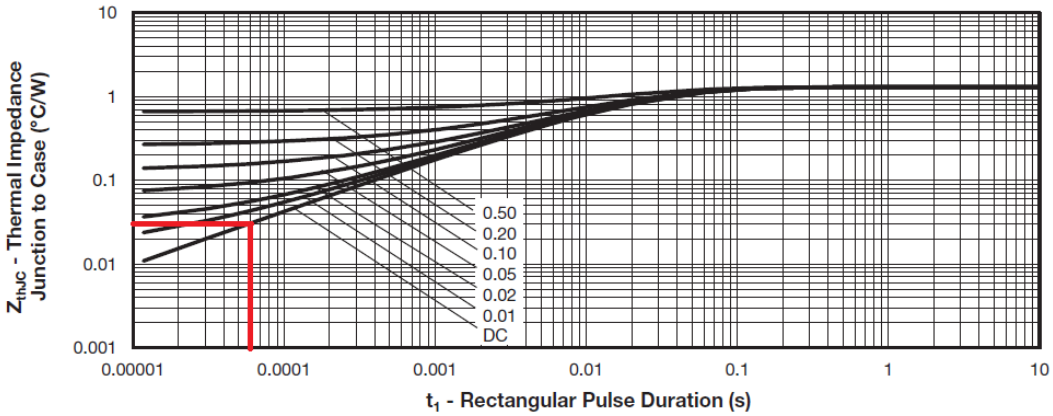


Fig. 4.6: Maximum thermal impedance Junction-to-Case Characteristic (courtesy of Vishay Semiconductor Italiana).

4.1.3 Data Manipulation

The data obtained from the commissioning test shown in Fig. 4.2 can be reorganized and represented in a 3D-plot as shown in Fig. 4.7. In this case V_{ON} and i_{DS} are considered inputs and θ_J the output. The data obtained experimentally need to be reorganized so to have regularly spaced input vectors. 4.8 show the same data reorganized in the form $\theta_J(R_{ON}, i_{DS})$. The two representations are equivalent, however the second one is easier to interpolate. The surface of $\theta_J(R_{ON}, i_{DS})$ can be easily interpolated by a second degree polynomial function.

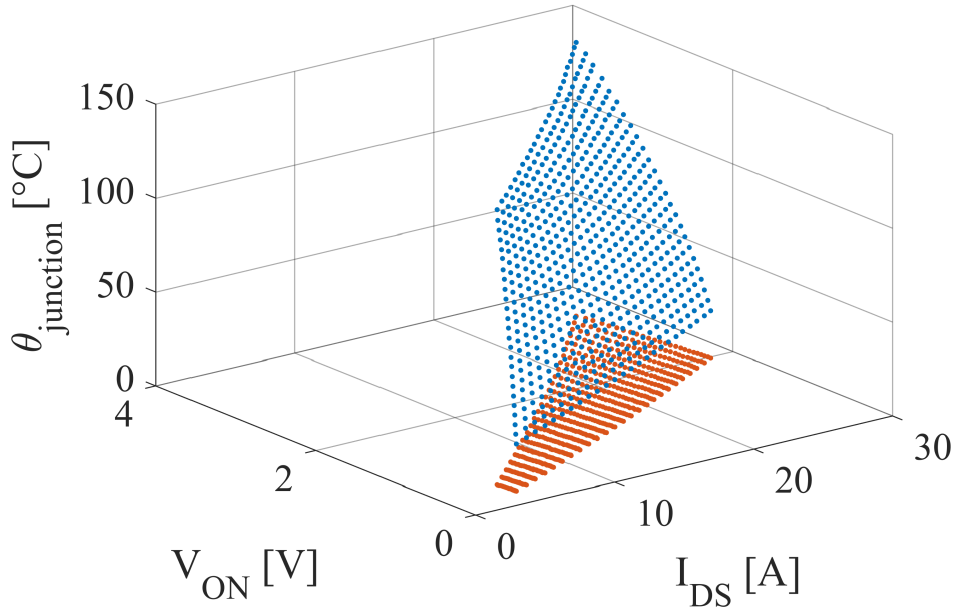


Fig. 4.7: Experimental data reorganized for having $\theta_J(V_{ON}, i_{DS})$.

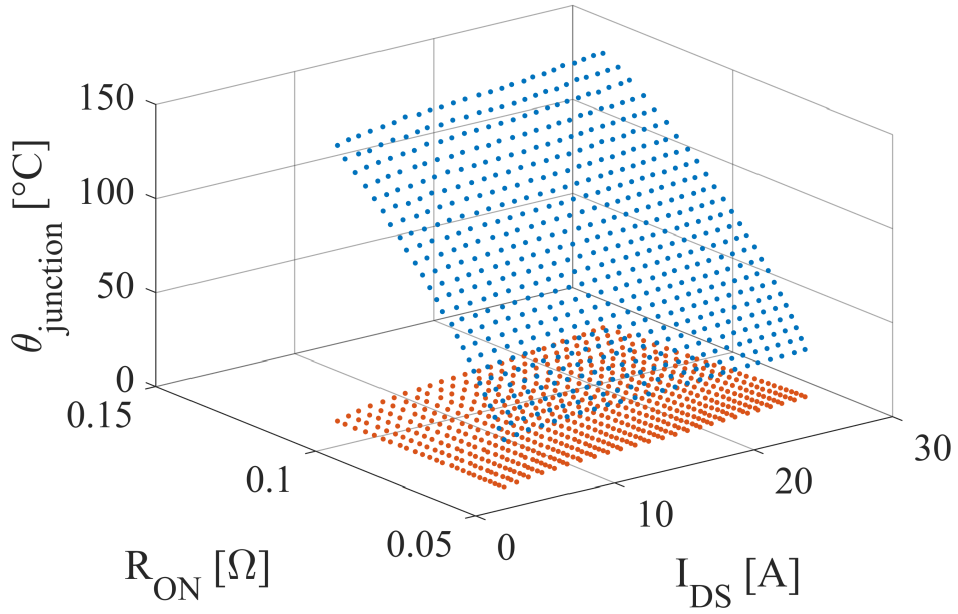


Fig. 4.8: Experimental data reorganized for having $\theta_J(R_{ON}, i_{DS})$.

4.1.4 Measured vs Datasheet R_{ON}

Fig. 4.9 shows the variation of the R_{ON} as a function of the junction temperature. The datasheet of the power module provides $R_{ON}(\theta_J, i_{DS}= 20\,A)$, however the typical characteristic curve provided in the datasheet is precautionary. The real $R_{ON}(\theta_J, i_{DS}= 20\,A)$ obtained from the commissioning test is sensibly lower than the one provided in the datasheet as shown in Fig. 4.9. The small difference between the datasheet values and the real values (around 1-2 mΩ in this case) for most applications is not critical, however the R_{ON} provided by the datasheet can't be used to estimate the junction temperature. According to Fig. 4.9 a 2 mΩ variation of the R_{ON} corresponds to a 60 °C variation of the junction temperature. The conduction resistance depends also on the temperature as shown in Fig. 4.10. For a certain θ_J value, R_{ON} increases approximately linearly with increasing i_{DS}. In conclusion, the junction temperature can't be estimated only as a function of R_{ON}, also the i_{DS} dependency has to be considered.

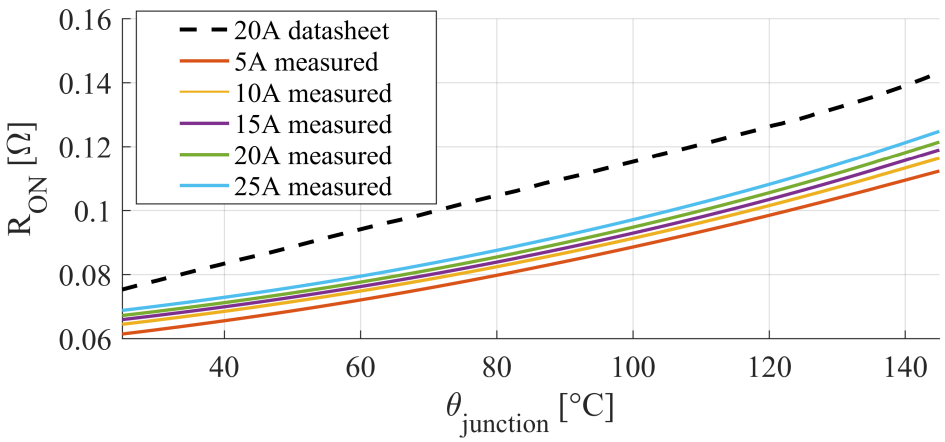


Fig. 4.9: Measured values of R_{ON} as a function of junction temperature. The black dashed line represents the R_{ON} provided in the datasheet while the continuous lines respresents the V_{ON} measured experimentally.

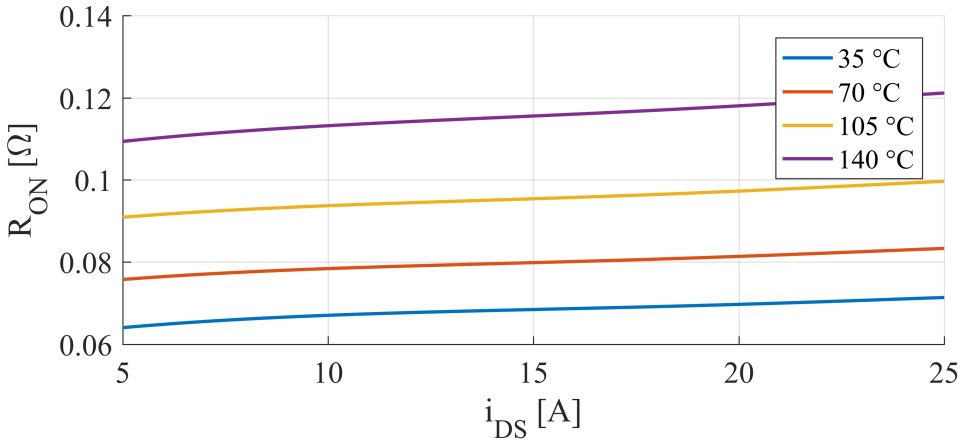


Fig. 4.10: Measured values of R_{ON} as a function of current.

4.2 On-line Junction Temperature Estimation

While the converter is normally operating under hard switching conditions, V_{ON} and i_{DS} are measured at each PWM period and thanks to the previously obtained look-up table the junction temperature can be estimated. 4.11 shows the functional block of the temperature estimator when the look-up table is used in the form of $\theta_J(R_{ON}, i_{DS})$. A new value of $\theta_{J,est}$ is obtained at every PWM period, so for a switching frequency of 10 kHz the value of $\theta_{J,est}$ is updated every 100 µs.

Fig. 4.12 shows $\theta_{J,est}$ for module#2 under square-wave load current. The blue dashed line represents the DBC temperature measured by the NTC1 sensor, the blue continuous line represents the estimated junction temperature and the red continuous line represents the load current. When the MOSFET current steps from 7.5 A to 25 A, the temperature rises from 80 °C to 140 °C in one second. By looking at the time variation of $\theta_{J,est}$, it can be observed that the dynamics of the thermal transient is dominated by multiple thermal constants due to the different layers materials of the power module. The results show that the fast variation of the junction temperature can't be measured using the embedded NTC thermistor.

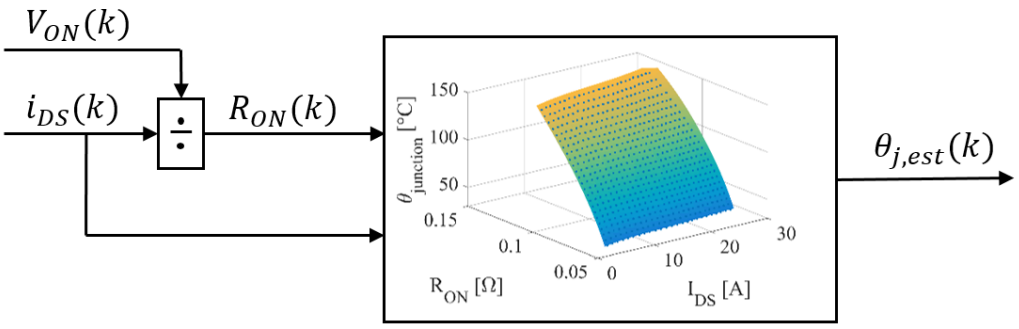


Fig. 4.11: Temperature estimator functional block using $\theta_J(R_{ON}, i_{DS})$.

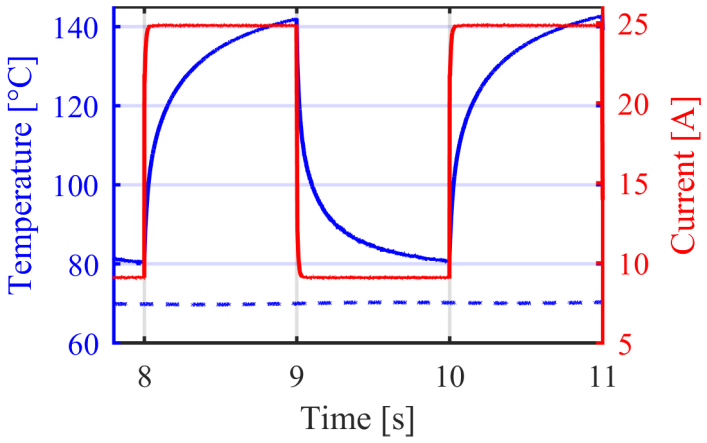


Fig. 4.12: On-line estimation of SW1L junction temperature (blue), with square-wave load current (red). Dashed blue line: DBC substrate temperature, measured from NTC1.

Fig. 4.13 shows the response of the junction temperature estimate for module#1, under different load waveforms. Once again, the temperature response shows multiple time constants, the quickest of which is below 0.1 s.

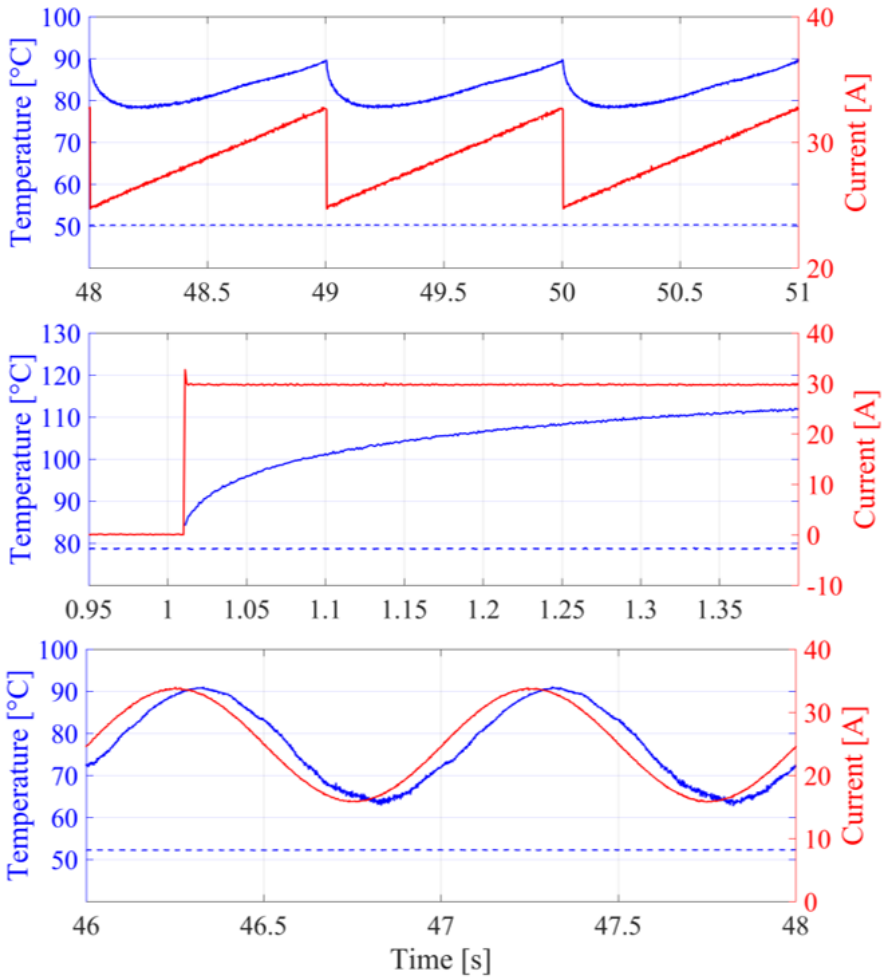


Fig. 4.13: On-line estimation of SW1L junction temperature (blue), at different load currents (red). Dashed blue line: DBC substrate temperature, measured from NTC1.

4.3 Closed-Loop Temperature Control

The estimated junction temperature of the switch under test can be actively limited in closed-loop. A PI regulator is used to saturate the maximum load current when $\theta_{J,est}$ exceeds the limit set by the user. An example of implementation is shown in Fig. 4.14. The results obtained using the module#2 in active temperature limitation are reported in the following. In Fig. 4.15 the load current represented in yellow is initially set to 18 A DC. After 14 s, a 0.5 Hz sinusoidal current (4 A peak to peak) is superimposed to the DC component. The DBC temperature is indicated with a red dashed line. This remains approximately constant during the

whole test (around 40 °C). The estimated junction temperature is represented in blue while the maximum allowed junction temperature is represented by a black dashed line. During the test the temperature threshold is lowered to trigger the temperature control: the junction temperature is automatically limited by limiting the maximum amount current in the switch.

As described in the previous section, LEG1 is open-loop controlled at a fixed duty cycle while the load current is closed-loop controlled by LEG2. Different combinations of duty cycles and load currents have been tested. In Fig. 4.15 and Fig. 4.16 the LEG1 duty cycle is set to 0% (SW1L always close) while LEG2 controls the load current. In the first case the sinusoidal current component has a frequency of 0.5 Hz while in the second case it has a frequency of 1 Hz. The thermal capacitance of the device filters the temperature swing when the frequency of the AC current component increases. This case is representative of the operations of a motor drive. Indeed, very low-speed operation of the machine corresponds low electrical frequency, thus producing high temperature swings. On the other hand, high speed operation corresponds to a higher electrical frequency, where the swing is lower and the the device can accept higher values of current.

In Fig. 4.17 and Fig. 4.18 the LEG1 duty cycle is set to 50% (SW1L is in conduction 50% of the time) while the LEG2 is controlling the load current. In this case the conduction losses are equally split between SW1L and SW1H and the junction temperature limit is never reached. Thanks to the active temperature limitation the converter can work safely, within its SOA.

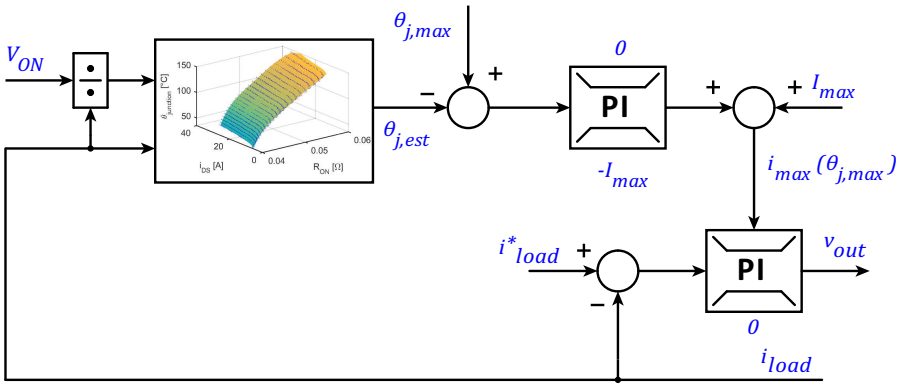


Fig. 4.14: Functional block for the temperature limitation.

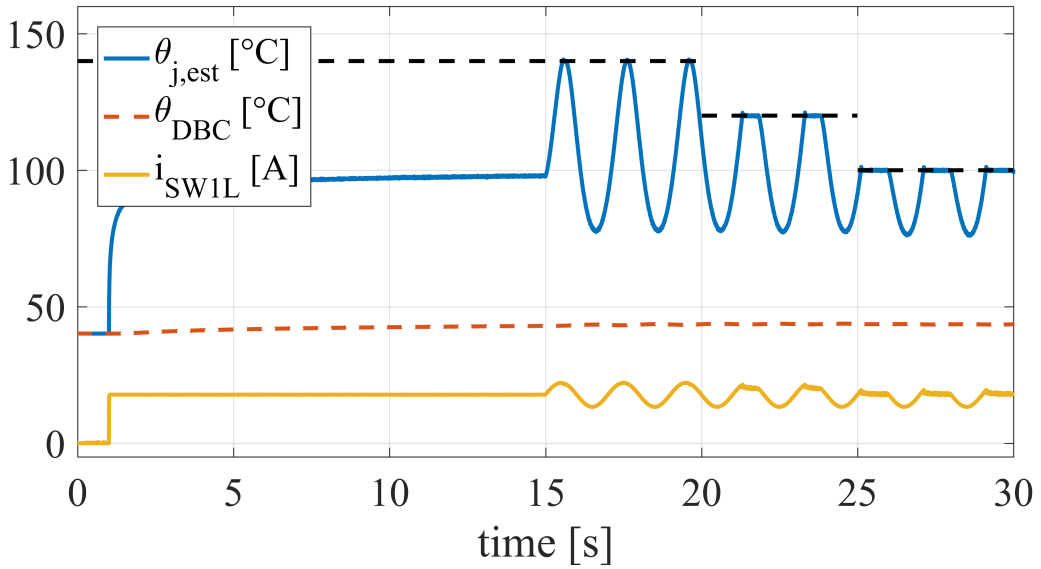


Fig. 4.15: Online junction temperature limitation, duty-cycle LEG1=0% (SW1L always close). AC current frequency 0.5Hz.

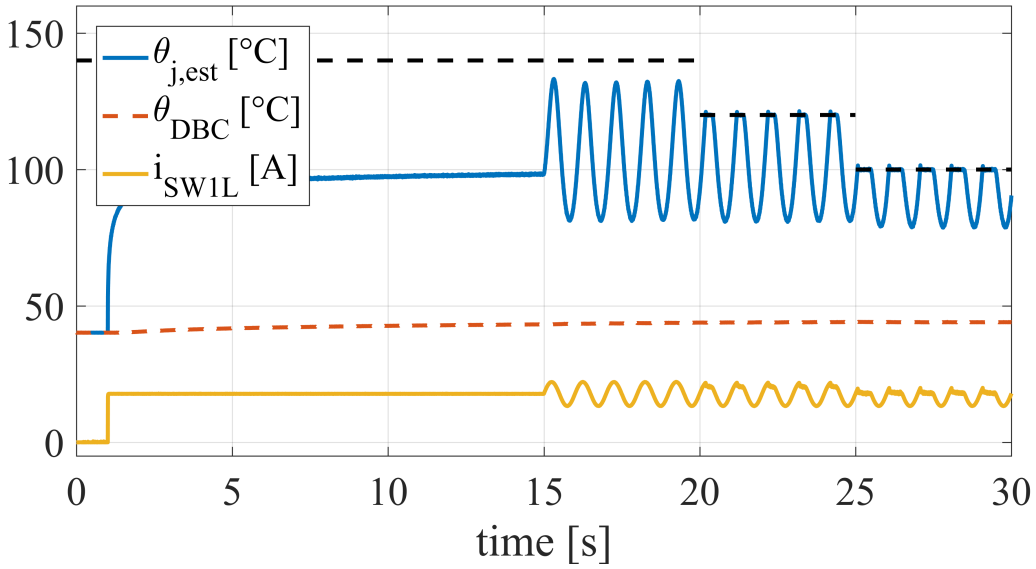


Fig. 4.16: Online junction temperature limitation, duty-cycle LEG1=0% (SW1L always close). AC current frequency 1Hz.

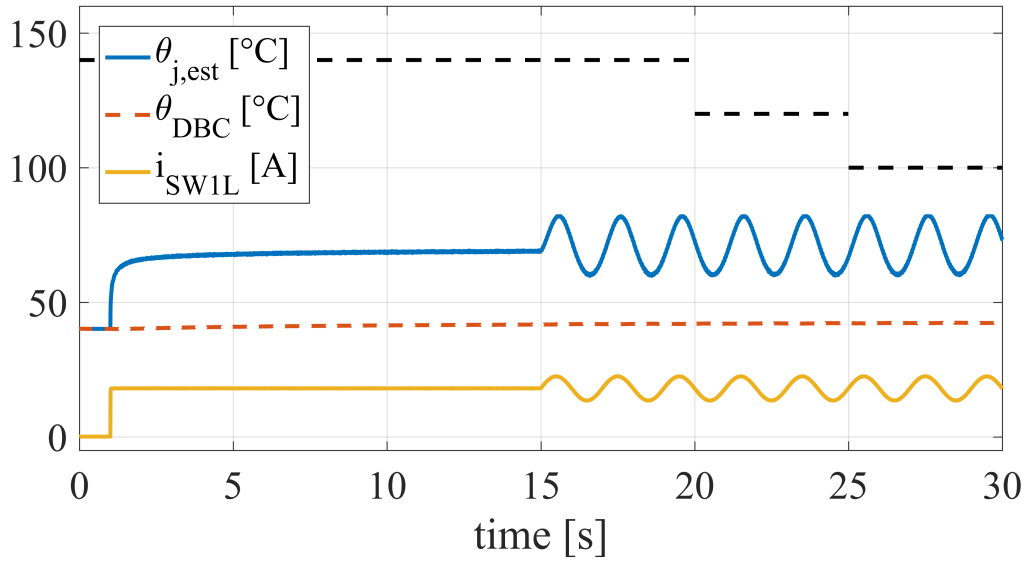


Fig. 4.17: Online junction temperature limitation, duty-cycle LEG1=50% (SW1L close 50% of the time). AC current frequency 0.5Hz.

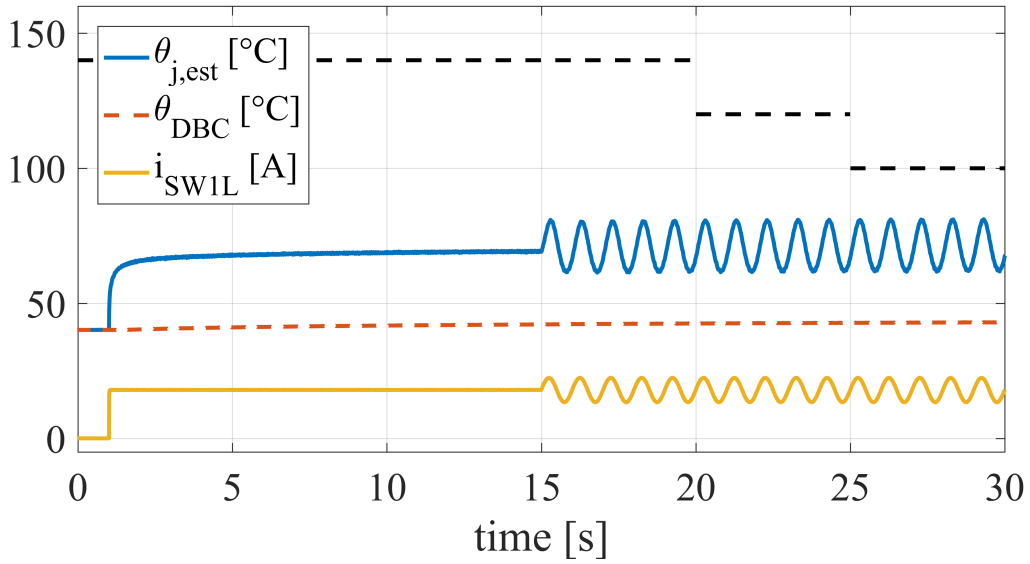


Fig. 4.18: Online junction temperature estimation, average duty-cycle LEG1=50% (SW1L aclose 50% of the time). AC current frequency 1Hz.

4.4 Validation of the Proposed Technique

Different tests have been conducted to validate the accuracy and the robustness of the proposed technique.

4.4.1 Thermal Camera Validation

IR tomography has been used to validate the proposed methodology [22]. A CEPID Titanium infrared camera has been used. The insulating gel covering SW1L has been removed and the surface of the die has been black painted. Subsequently the test rig layout has been modified so to permit visual access to the switch under test. An overview of the modified test rig with the thermal camera and the black painted die is shown in Fig. 4.19. Due to the gel removal the validation tests have been conducted at a reduced temperature, to avoid the voltage breakdown of the MOSFET under test. Following the modification of the test rig layout, the DC-link capacitors are no longer in the immediate proximity of the pins of the power module, thus during the turn-OFF phase of the MOSFETs over-voltages can reach hundreds of volts. Consequently LEG1 duty cycle has been kept to zero, thus SW1L is always ON. The shown results are related to module#2.

The two pictures of Fig. 4.20 show the infrared images of the chip under test while it is conducting two different currents values. The edges of the chip are difficult to see from the pictures, so they have been highlighted by a black dashed line. The dimensions of the chip are 3.1 mm for 3.36 mm, however despite the small size, during the normal operations of the converter the temperature gradient across the device is anything but negligible. Fig. 4.20a shows the thermal image of the chip during the heating phase while Fig. 4.20b shows the chip during the cooling phase. In 4.20a the temperature gradient between the hotspot and the borders is around 35 °C. The presence of the bonding wires helps the extraction of the heat from the center of the chip, however this generates an even more irregular distribution of the temperature as shown in Fig. 4.20b. Due to the bonding wires the hotspot is not located exactly in the center of the chip. In Fig. 4.21 a 0.1 Hz square wave current (yellow) ranging from 15 A to 23 A is commanded to the load. The temperature measured using the embedded NTC1 (red) is constant (around 35 °C) during the test. The estimated temperature is reported in blue, while the average temperature on the surface of the chip measured by the IR camera is reported in a green dashed line. The average and the estimated temperatures have a good matching especially for high currents. When the drain current lowers from 23 A to 15 A the estimation became less accurate. The purple dashed line represents the temperature of the hotspot measured by the IR camera. The mismatching between the estimated and maximum temperature is modest for low currents, but increases for high currents. In this case for a 23 A, drain current the difference between estimated and hotspot temperatures reached 12 °C. The proposed method permits

to estimate correctly the **average** temperature across the chip, however it is not able to provide any information about the maximum temperature across the chip. The converter designer has to take an appropriate safety margin if the proposed method is used for actively limit the maximum junction temperature.

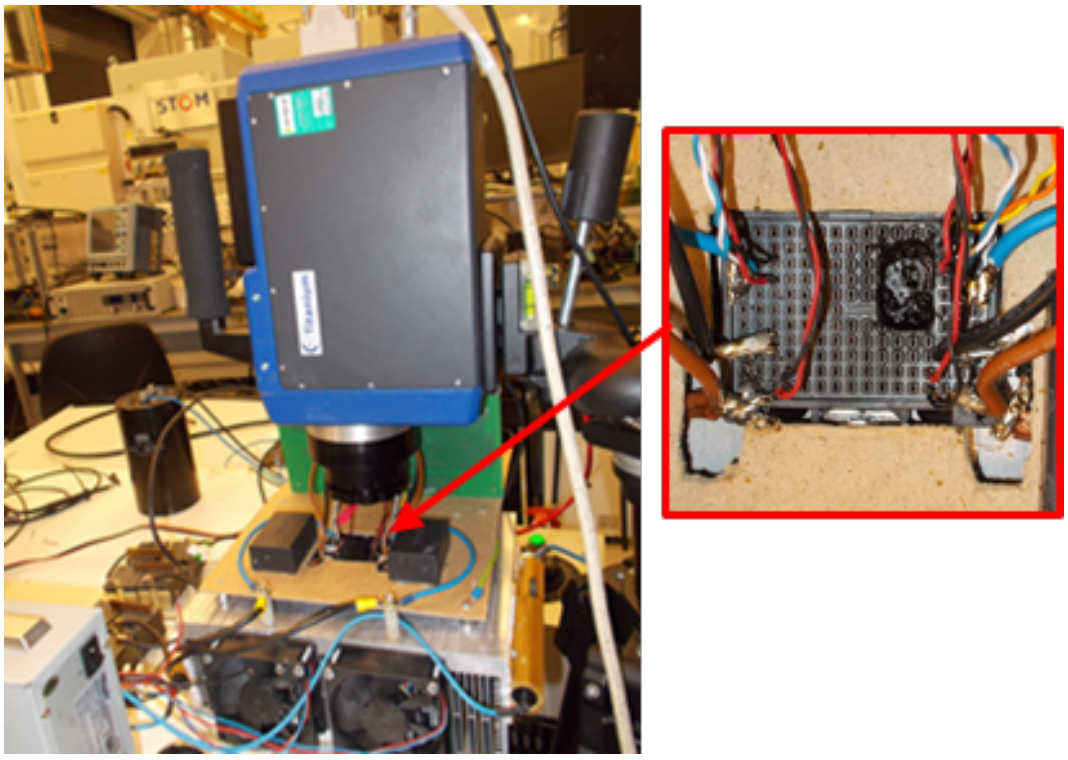
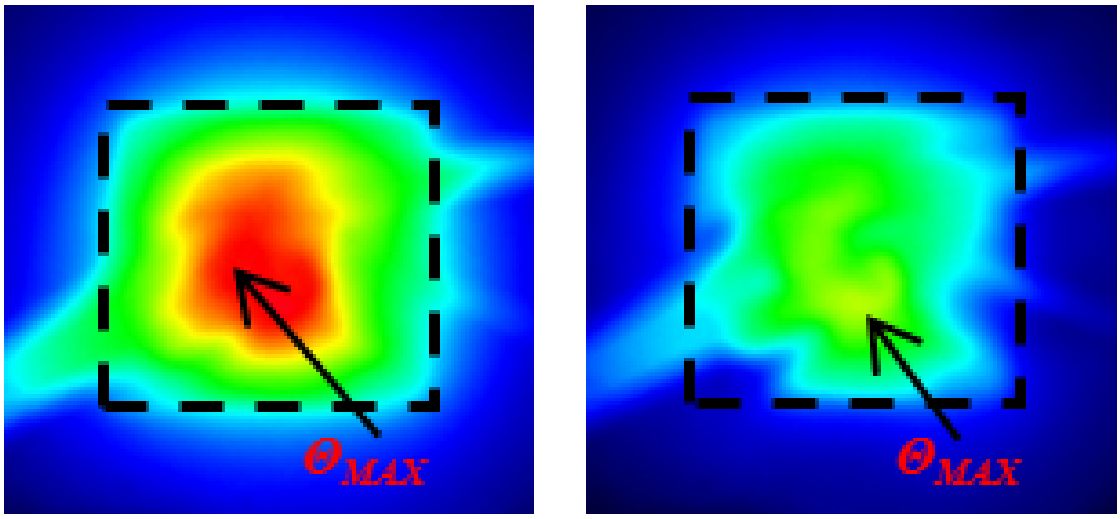


Fig. 4.19: Test rig with modified layout and thermal camera.



(a) Heating phase. (b) Cooling phase.

Fig. 4.20: Thermal image of the chip SW1L. The black dashed line indicate the die area.

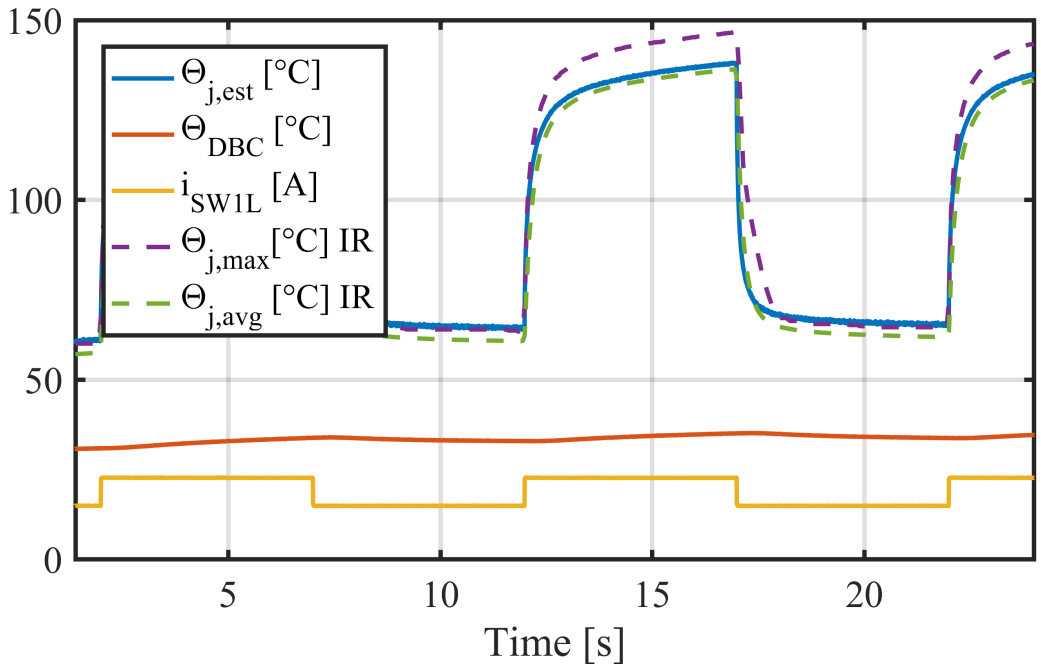


Fig. 4.21: Validation with IR camera: comparison estimated temperature (blue) and measured temperature (dashed). Maximum and average measurements are reported.

4.4.2 Comparison with an Adjacent Thermistor

A second thermistor (labeled as NTC2 in Fig. 3.5) has been placed in contact with the device under test. Fig. 4.22 shows that NTC2 has been placed right under the bonding wires of the switch SW1L. Fig. 4.23 reports the measured and estimated temperature response to a 25 A current step. The comparison shows that the NTC2 thermistor outputs a lower temperature value. In steady state the temperature measured by NTC2 is 45 °C lower than the estimated temperature. Due to the sensor thermal capacitance and to the thermal impedance between the sensor and the die, the measured temperature is delayed. The delay is clearly visible in Fig. 4.24, where to a 20 A DC current a 5 A peak sinusoidal component is overlapped. Both estimated and measured temperatures have a sinusoidal shape, but the measured temperature is attenuated and delayed compared to the estimated one. Fig. 4.23 and Fig. 4.24 clearly show that although NTC2 is placed as close as possible to the die, it is not able to measure the intimate junction temperature of the die.

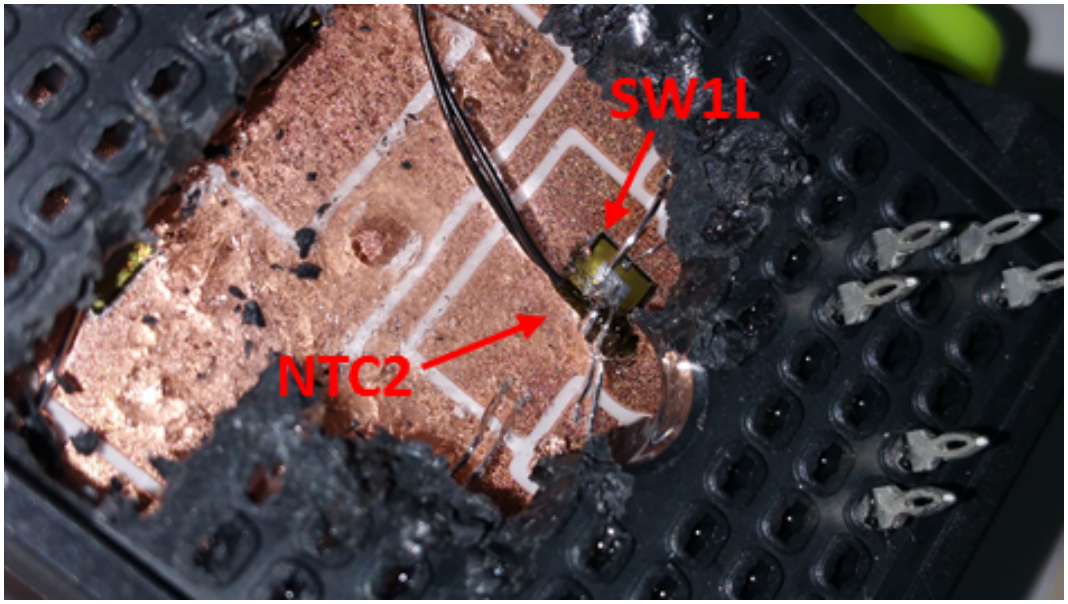


Fig. 4.22: Placement of NTC2 thermistor under the bonding wires of the die under test.

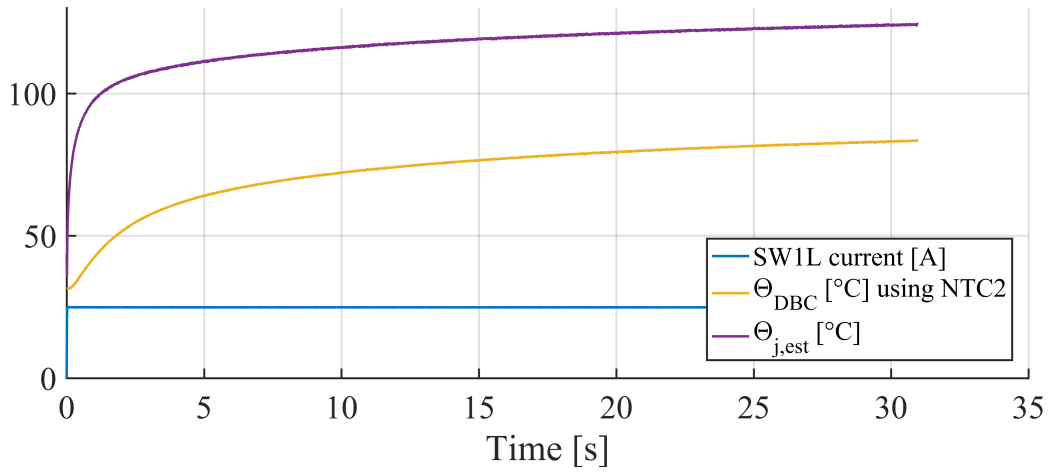


Fig. 4.23: Current step of 25 A. Comparison between junction temperature estimate and direct-contact measurement with NTC2.

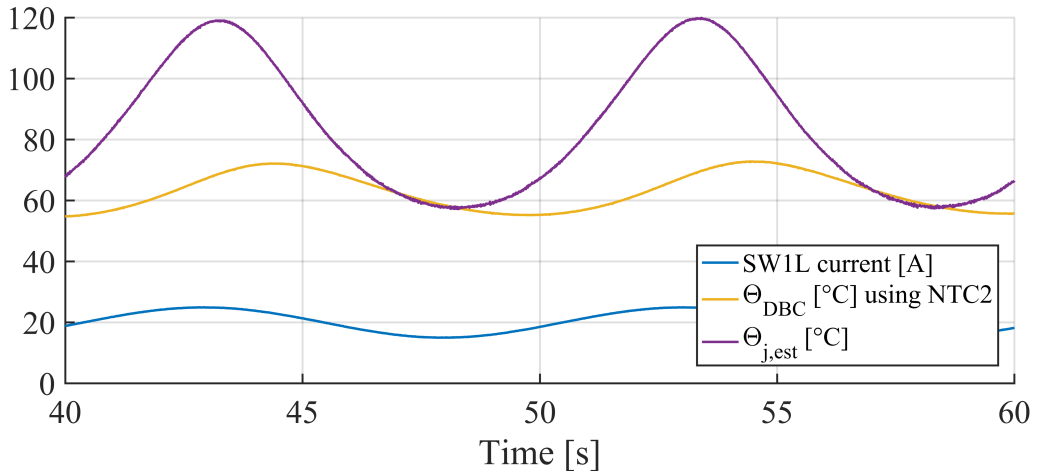


Fig. 4.24: AC current at 0.1 Hz superimposed to 20 A DC. Comparison between junction temperature estimate and direct-contact measurement with NTC2.

4.4.3 Insensitivity of Commissioning to the NTC Placement

The commissioning test has been repeated, using the local NTC2 thermistor. The results show that the "new" look-up table computed using NTC2 is identical to the "old" look-up table computed using NTC1. Fig. 4.25 and Fig. 4.26 show that the temperature estimates obtained using the two look-up tables are superimposed. The two plots show that the look-up tables obtained during the commissioning

test are insensitive to the position of the NTC sensor within the power module. Further validating the foundation of the commissioning method. Consequently, the embedded NTC1 sensor inside the power module is sufficient to characterize the device and no additional thermistors are required.

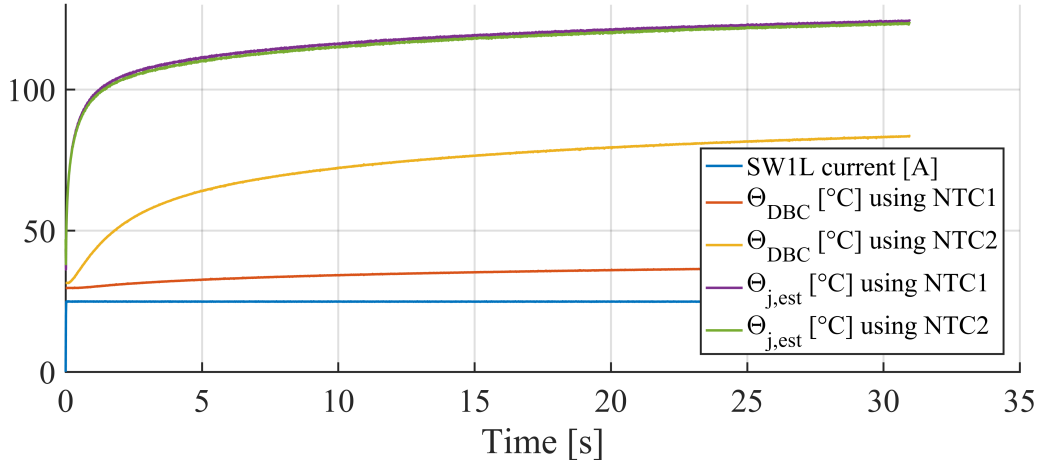


Fig. 4.25: Junction temperature estimation during a current step of 25A.

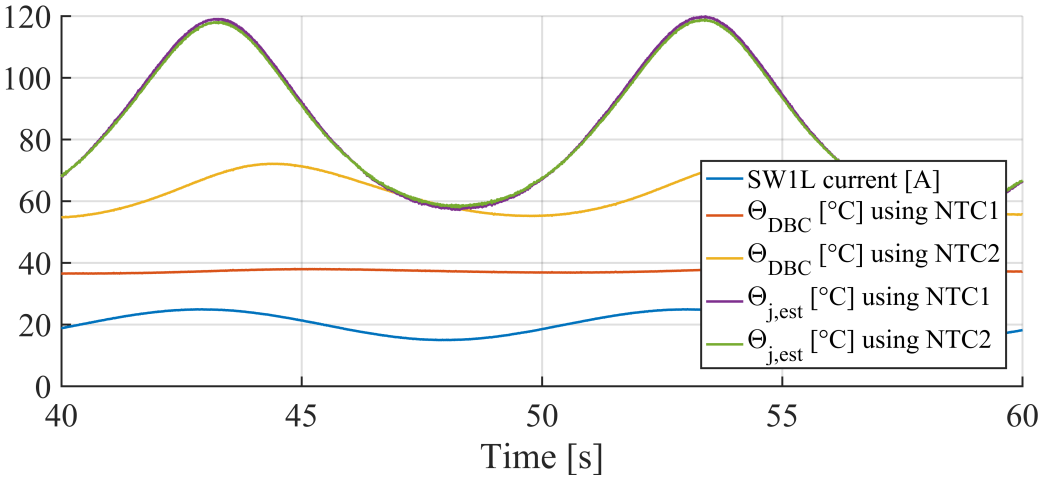


Fig. 4.26: Junction temperature estimation with sinusoidal current reference.

4.4.4 Commissioning Test Repeatability

The commissioning test has been repeated three times and three new look-up tables have been obtained. In Fig. 4.27 a square wave current has been commanded to the load and the temperate has been estimated using the three look-up tables.

The results coming from the three look-up tables are overlapped. A small discrepancy in the three temperature estimates is present at low currents, this is due to the problems in measuring the V_{ON} when the current and consequently the voltage drop are low.

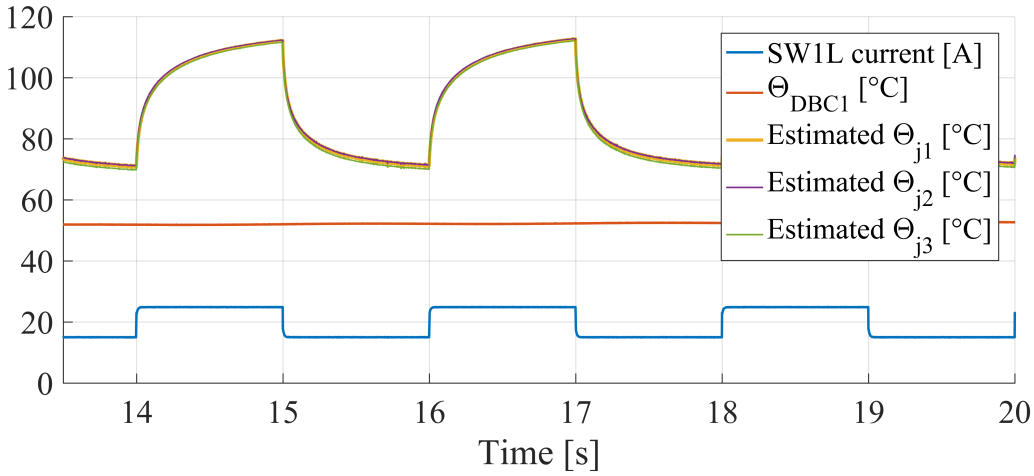


Fig. 4.27: Temperature estimation using three different look-up-tables, made during three different tests.

4.5 Comparison Between Dies from Different Manufacturers

Depending on the manufacturer, variations of R_{ON} with respect to temperature can be significantly different. To obtain a correct estimation of the junction temperature, R_{ON} has to increase sufficiently when the temperature of the device increases. However, if the R_{ON} variation with respect to temperature is too pronounced, the device thermal runaway is likely to occur. In this section, R_{ON} sensitivity with respect to the temperature of module#1 and module#2 is compared. Fig. 4.28 shows $R_{ON}(\theta_J\ , i_{DS})$ for module#1 while Fig. 4.29 $R_{ON}(\theta_J\ , i_{DS})$ for module#2, both maps have been obtained during the commissioning test. As reported in Table 3.1 and Table 3.2, the rated DC current at a case temperature of 80 °C is 26 A for module#1 and 19 A for module#2. While the rated resistance at a junction temperature of 25 °C is 71 mΩ for module#1 and 78 mΩ for module#2. Though the two modules have a different nominal current, some comparisons can still be made in percentage terms. When the temperature of module#1 rises from 35 °C to 145 °C (i_{DS}= 26 A), R_{ON} increases by 36% as shown in Fig. 4.30. When the temperature of module#2 rises from 35 °C to 145 °C (i_{DS}= 19 A), R_{ON} increases by 84% as shown in Fig. 4.31. As reported in Fig. 4.32 and Fig. 4.33, the variation

of R_{ON} with respect to i_{DS} is modest for both modules. The temperature can be estimated correctly for both modules, despite module#2 has a lower R_{ON} variation with respect to the temperature.

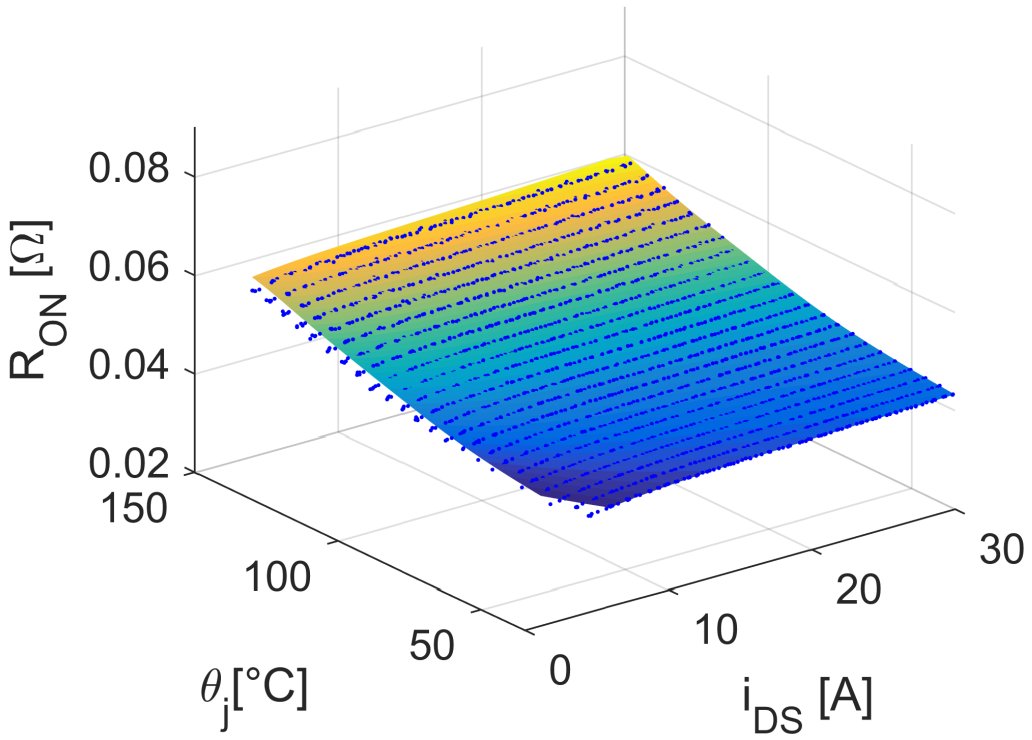


Fig. 4.28: Measured R_{ON} as a function of junction temperature and current for module#1.

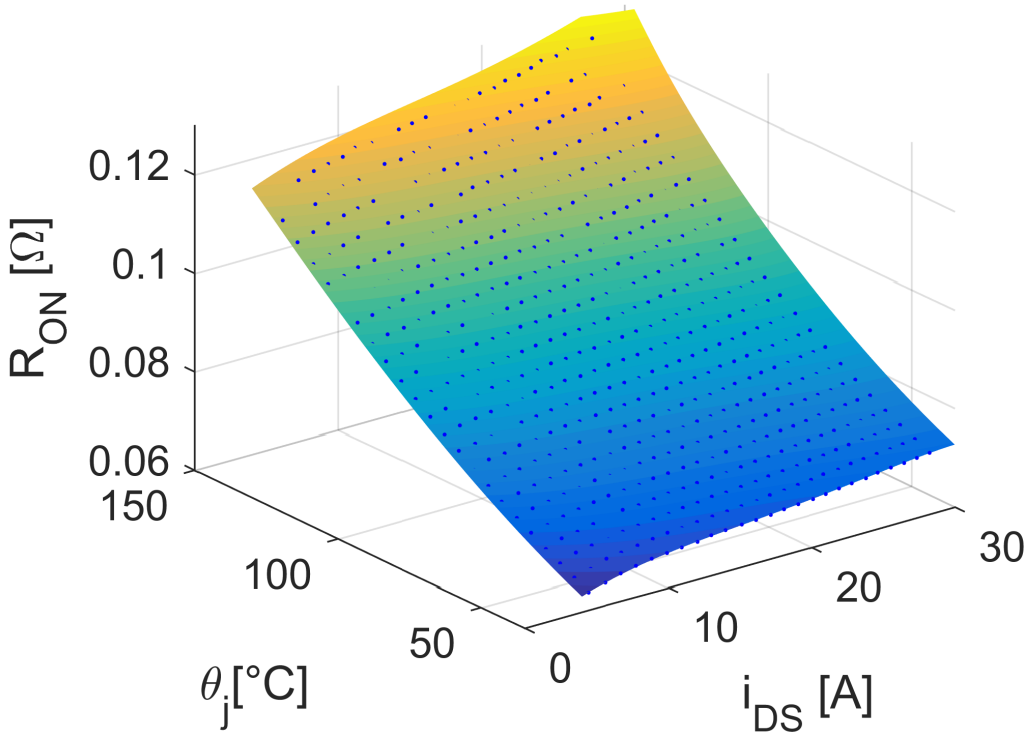


Fig. 4.29: Measured RON as a function of junction temperature and current for module#2.

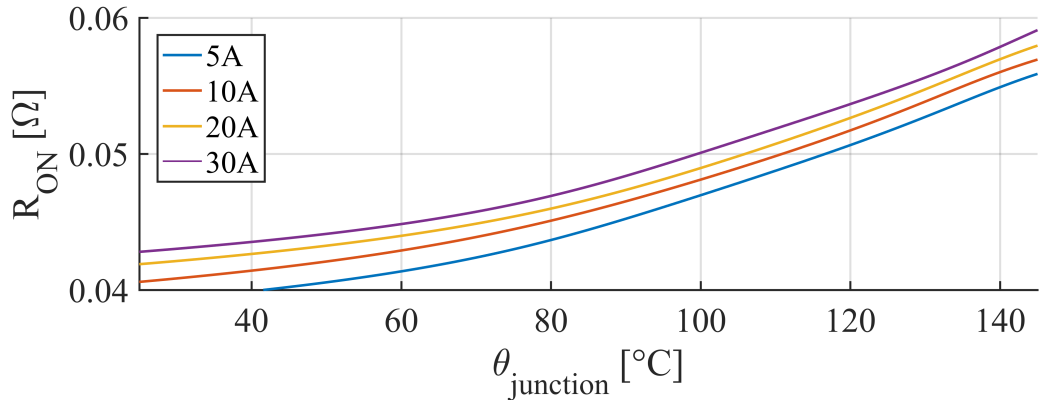


Fig. 4.30: Measured values of R_{ON} as a function of θ_J for module#1.

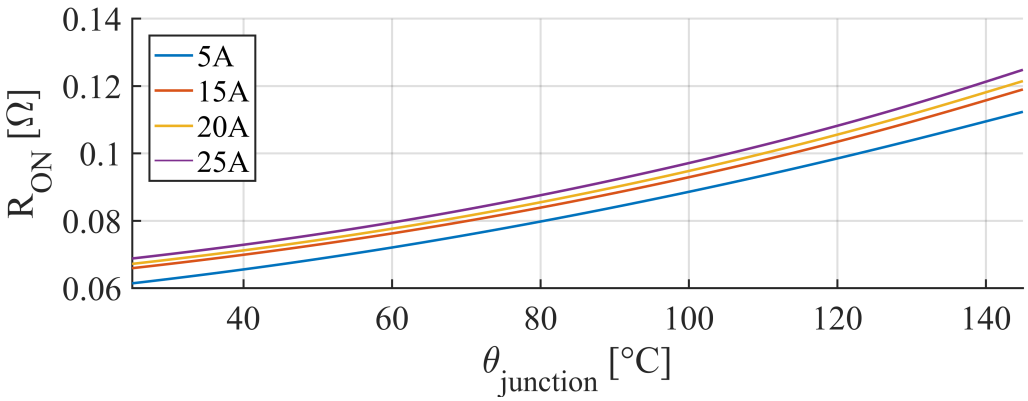


Fig. 4.31: Measured values of R_{ON} as a function of θ_J for module#2.

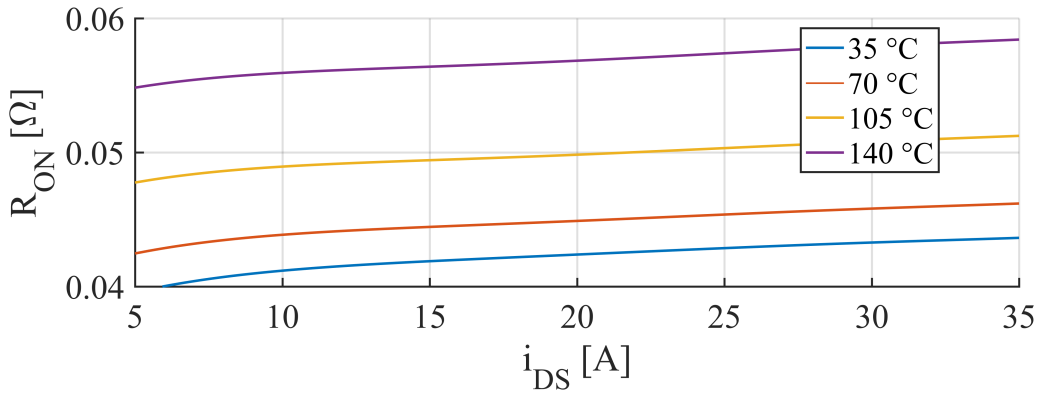


Fig. 4.32: Measured values of R_{ON} as a function of i_{DS} for module#1.

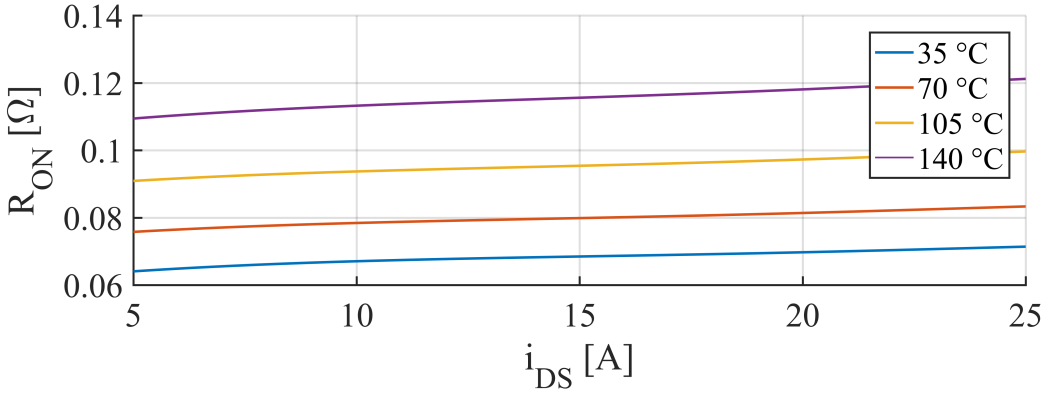


Fig. 4.33: Measured values of R_{ON} as a function of i_{DS} for module#2.

4.6 Conclusion

4.6.1 Limitations of the Proposed Test Rig

The main limitations of the proposed test rig are:

- The switching frequency for having a valid temperature estimation is currently limited to 80 kHz when the duty cycle is 50%, thus corresponding to a minimum settling time of 3 µs circa. Another critical situation is when the duty cycle of the switch under test is low. E.g. the switch is closed only for 1% of the period, so that the settling time for measuring V_{ON} is not sufficient. This case is usually not critical in terms of junction temperature.
- Only the switch SW1L is fully monitored for reasons of simplicity. The other switches inside the power module can be monitored in a similar manner.
- The temperature is estimated only for positive drain current, because the V_{ON} measurement system is not able to sample negative voltages. This choice was done to maintain high the level of accuracy for this measurement. However after the tests it is clear that a 12 bit A/D would be sufficient to cover the entire range.
- The temperature estimation is inaccurate when the drain current is low. Regarding this set-up $\theta_{J,est}$ becomes inaccurate when the current in the device is less than 1/3 of the nominal current. This is a weakness of the adopted TSEP. However for low values of currents θ_J is not usually critical.
- For commissioning, it is necessary to heat the heatsink to the maximum junction temperature that the user want to estimate. This can be a problem in many applications, especially if the commissioning test is performed by the final user and not at the end of the line by the manufacturer. Alternatively the commissioning test can be performed at a lower temperature (E.g. up to 70 °C) and then to extrapolate the component map at higher temperatures. This aspect is currently under investigation. Despite the encouraging results, more tests need to be done. Performing the commissioning test at low temperature could allow to heat up the heatsink using the losses of the power module instead of external resistors.

4.6.2 Other Considerations

As shown in Fig. 3.5 three currents are measured: i_{SW1L}, i_{SW2L} and i_{LOAD}. i_{SW2L} measurement is not strictly necessary, it has been added as a redundancy check on the current measurement. The current in the switch under test can be measured using the shunt sensor(i_{SW1L}) or the closed-loop hall sensor (i_{LOAD}).

Theoretically when SW1L is ON both sensors measure the same value of current, however the closed loop hall sensor has a lower bandwidth with respect to the shunt resistor. To obtain a precise temperature estimation i_{DS} and V_{ON} have to be sampled synchronously. If the current signal coming from the sensor is delayed, V_{ON} and i_{DS} cannot be correlated correctly. The required bandwidth of the current sensor depends on the application. E.g. if the current ripple due to the modulation is high, so a high bandwidth current sensor is required.

It is well known that V_{ON} is affected by V_{GS} (Fig. 4.34), consequently a measurement system for monitoring the voltage between gate and source has been included as shown in Fig. 3.5. The V_{GS} measure is not strictly necessary, it was added for checking that the gate driver was working properly. In a commercial application this measurement would be unnecessary.

The V_{ON} measurement system has been calibrated to produce precise identification curves for the module under test. However in a commercial application, it is not necessary to run any calibration to correctly estimate the junction temperature. Instead of using the real V_{ON} when building the look-up table of the component, it is sufficient to use the value output by the ADC. Said differently it is not necessary that the V_{ON} pickup is extremely precise or finely calibrated, it is important that the measurement scale is consistent and repeatable throughout the life of the converter.

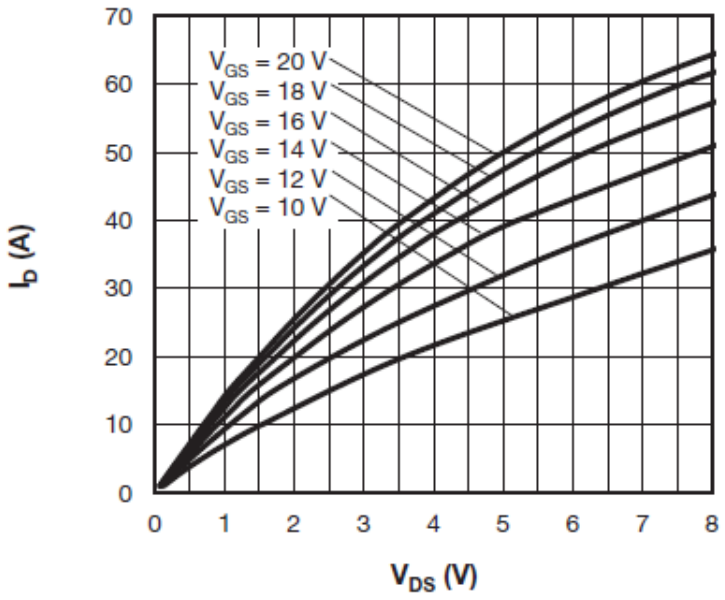


Fig. 4.34: Typical drain to source current output characteristics at $\theta_J = 25\,°C$ for module#2.

Chapter 5

Prognostics

5.1 Review of Power Devices Prognostics

Fig. 5.1 shows that according to a survey based on over 200 power electronic products [55], semiconductors are among the weakest parts. Power converters have reached high levels of efficiency and compactness, however a lot of work is still to be done concerning their reliability [56]. High levels of reliability must be guaranteed in safety critical applications like aviation, automotive and medical, or applications where the downtime is costly. The junction temperature plays a key role in the lifetime expectancy of a semiconductor. The knowledge of $\theta_{J,est}$ permits to increase the reliability of the devices inside a power module. The lifetime of a semiconductor is not only influenced by its absolute working temperature, but also by the temperature swings [57]. Many efforts have been made to improve power modules reliability, by enhancing the heat dissipation and the thermal cycling capability [57]. Different failure mechanisms are possible: bond wire lift-off, corrosion, chip cracking, delamination and solder fatigue [58].

Online or offline diagnostic tests help reducing the need for regular maintenance and preventive replacement of component. Even more, prognostics techniques can alert about the aging of power semiconductors and avoid or mitigate the consequences.

To maintain a high reliability, the power semiconductors can be systematically replaced after a certain running time. However, this solution is costly and it does not permit to protect the system in case of premature aging of the components. An alternative solution is to run a prognostics test to evaluate the current health state of the device. In literature, different health monitoring techniques have been proposed [59], [60] :

- **Model based.** This family of techniques requires a detailed knowledge of the internal structure of the power device. To identify the parameters of the model a series of complex tests need to be conducted using dedicated laboratory

equipments. An electrothermal model and a thermomechanical model are needed. The first mode compute the losses and, in turn the temperature variation of the device [61]. The second model estimate the mechanical stress across the device due to the temperature variations [62]. The device model can then be used to simulate the long term degradation due to different ambient and load conditions [63].

- **Dedicated sensor.** With the aging of the component, the thermal resistance between the different layers increases due to the degradation effects. The thermal resistance variation can be computed from the difference of temperature between the top and the bottom of the solder layer provided that the switch losses are known. Usually, the losses are calculated using a model of the component while the temperature can be measured using a local temperature sensor. The use of sensors can be costly, can compromise the normal operations of the converter and can decrease the reliability of the system [64].

- **Electrical parameters.** Electrical parameters can be used as an indirect indicator of the device health state. R_{ON} [65], [66] and the gate threshold voltage are among the most common parameters to estimate the health state of a power device [67]. However, other less conventional parameters can be used for prognostics, like parasitic capacitances variation, gate voltage waveforms, switching waveforms, body diode voltage drop and thermal impedance variation. This family of techniques is normally used in a laboratory environment where testing conditions can be controlled. E.g. The aging of a component can be evaluated by measuring the R_{ON} increase at a **fixed** current and junction temperature.

As aforementioned, the R_{ON} increase before the failure of the component can be used for prognostics. In [66] a Si power MOSFET is aged by cycling its junction temperature. It is observed that the R_{ON} increases by 10%-17% before the component fails. If R_{ON} is used as an indicator of the health state of the converter the main problem is its dependency from both temperature and current. When the tests are conducted in a controlled environment, currents and temperatures can be regulated, thus measuring R_{ON} variations. In [66] the device current is regulated using an external power supply and R_{ON} is sampled when the junction temperature measured using a PTC sensor attached to the device reaches a "trigger" value.

In this chapter, a methodology based on the R_{ON} inspection for assessing the health state of SiC power MOSFET modules is presented. Differently from other methodologies proposed in the literature, the evaluation of the health state of the device can be performed directly on the final converter without the need to control the environmental conditions and without the need of dedicated equipment. The commissioning test illustrated in Section 4.1.1 has been improved so to obtain a second look-up table used for estimating the health state of the switch under test.

Thanks to the obtained look-up table the health state of the device can be evaluated at any moment by imposing a DC current to the load. To prove the effectiveness of the proposed technique the power module under test has been aged and its health state has been evaluated. Part of this work was presented in [68].

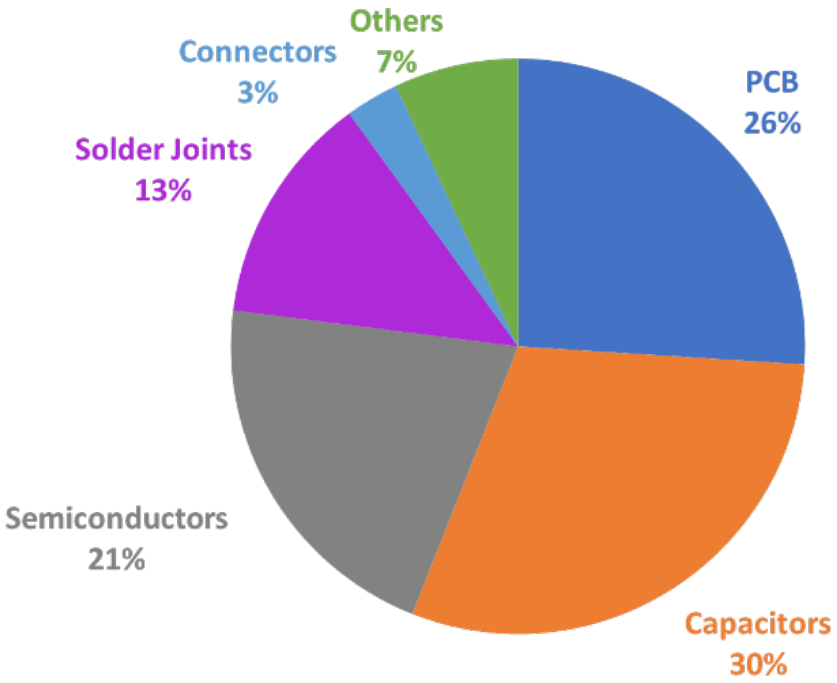


Fig. 5.1: Failure distribution among major components [55].

5.2 Modified Commissioning Test

The commissioning test procedure illustrated in Section 4.1.1 has been improved, so to obtain a second look-up table that can be used to estimate the aging of the component. The advanced commissioning test includes an additional R_{ON} capture per each DBC temperature level, besides the current pulse sequence described in the previous chapters. The modified procedure can be schematized as follows:

1. The heatsink is heated using the external resistors. When the temperature measured by NTC1 thermistor reaches 145°C the resistors are turned-OFF and the heatsink starts cooling naturally.

2. As before, a set of current pulses (Fig. 4.1) from 1 A to the maximum target current is imposed to the switch under test SW1L.

3. Moreover, a 15 A DC current of 10 s duration is commanded to the load. The V_{ON} is sampled after 10 s and memorized.

4. When the temperature measured with the NTC1 drops by 5°C the control algorithm automatically execute a new set of current pulses, including the final 10 s one.

5. As before, the test stops when the heatsink reaches the room temperature.

The advanced commissioning test flowchart is reported in Fig. 5.2. Fig. 5.3a shows the samples obtained from the commissioning test when the DBC temperature is greater than 85 °C (no 15 A-10 s commissioning), while Fig. 5.3b shows the samples obtained from the commissioning test when the temperature of the DBC is less or equal to 85 °C(with 15 A-10 s commissioning). The blue dots in Fig. 5.3b represent the last sixteen samples of the 15 A test (sampling time is 100 µs). Due to the 10 s duration the junction temperature differs from the temperature measured by NTC1. Different from the rest of the commissioning, this test refers to fixed current and fixed DBC temperature conditions. The average of the blue samples (Fig. 5.3b) populates a 2-D look-up table where R_{ON} is expressed as a function of the DBC temperature measured by NTC1 at a constant current of 15 A. The obtained $R_{ON}(\theta_{DBC}, i_{DS}{=}15\,\text{A})$ curve can then be used to estimate the health state of the switch SW1L.

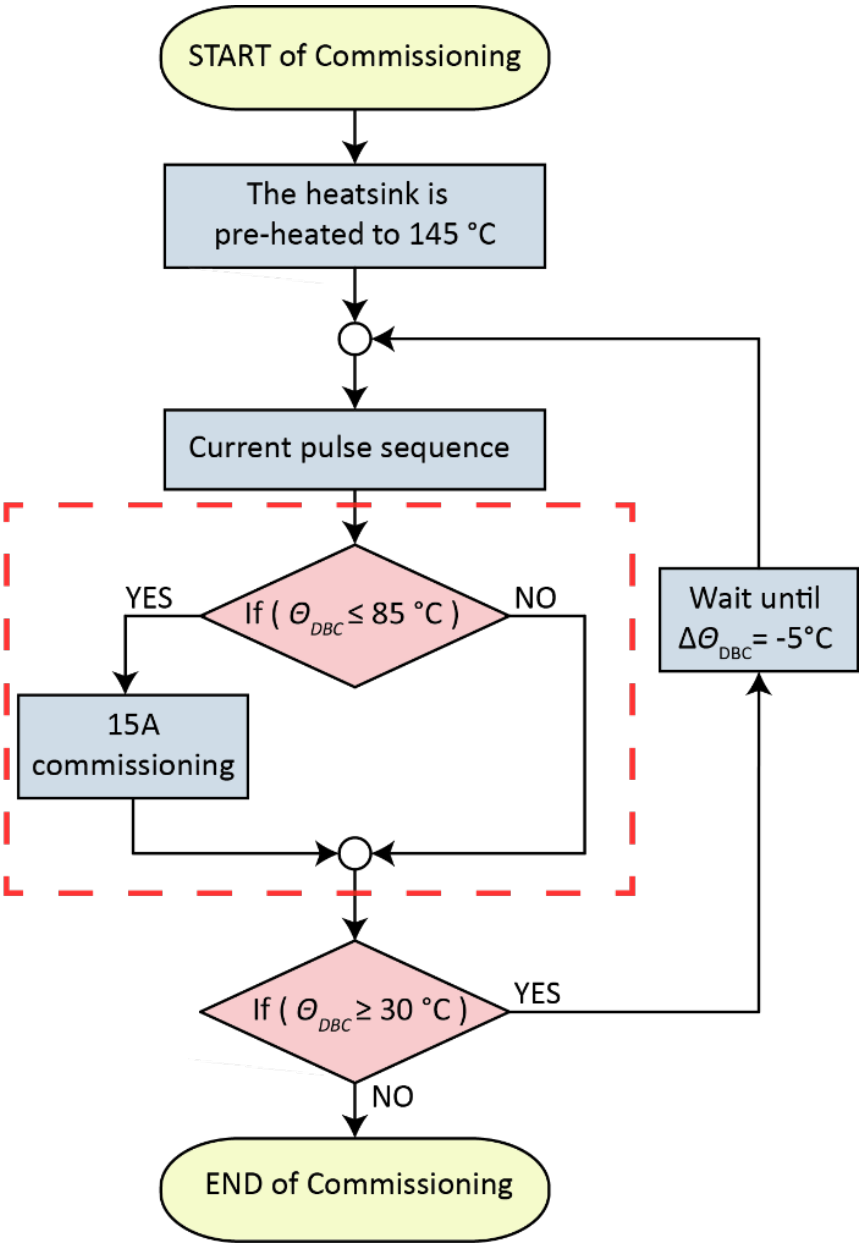
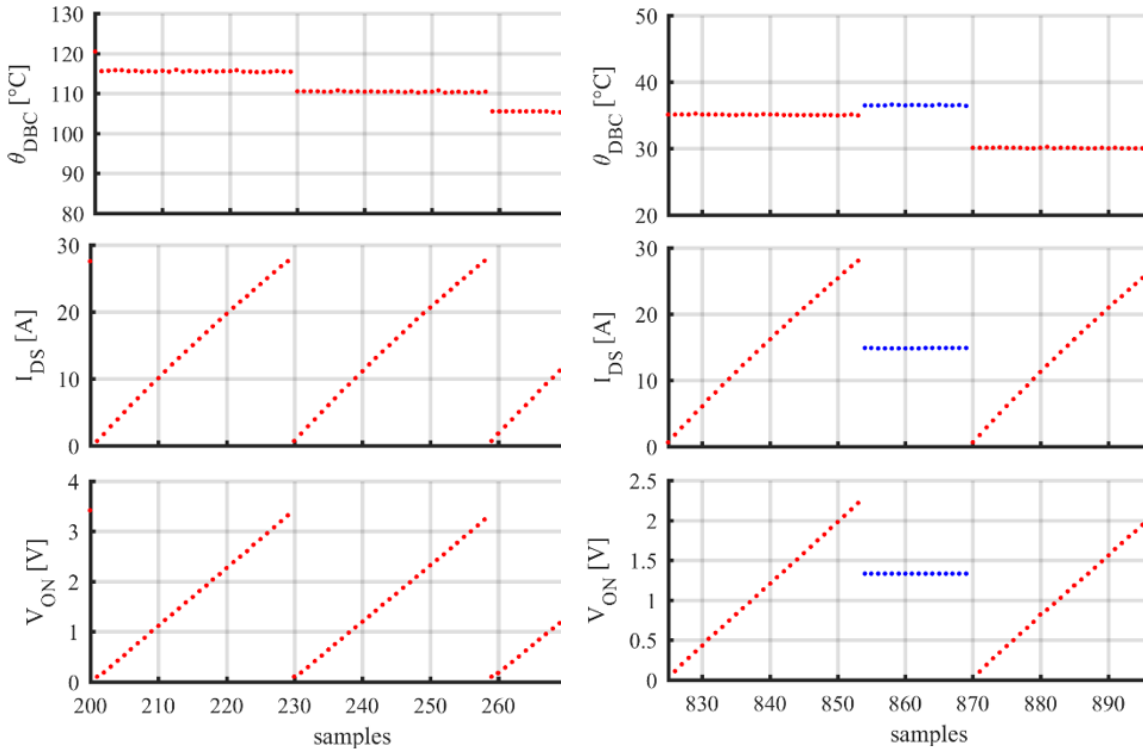


Fig. 5.2: Commissioning test flowchart.The dashed red box indicates the additional task dedicated to life state assessment for prognostics.



(a) θ_{DBC}>85 °C. (b) $\theta_{DBC}\leq$85 °C.

Fig. 5.3: Advanced commissioning test, with additional test (blue dots).

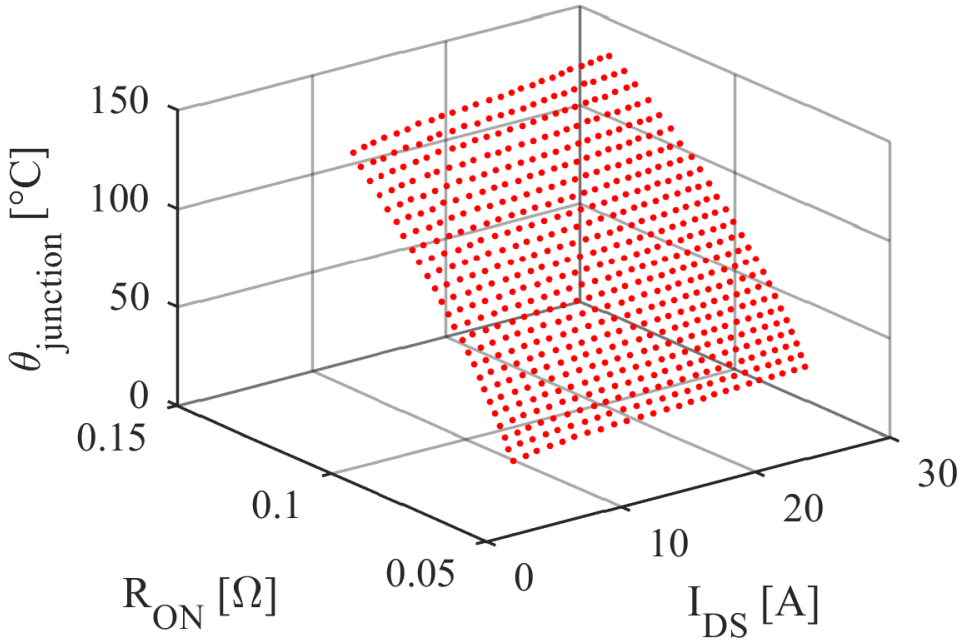


Fig. 5.4: Pulse current test results $\theta_J(R_{ON}, i_{DS})$.

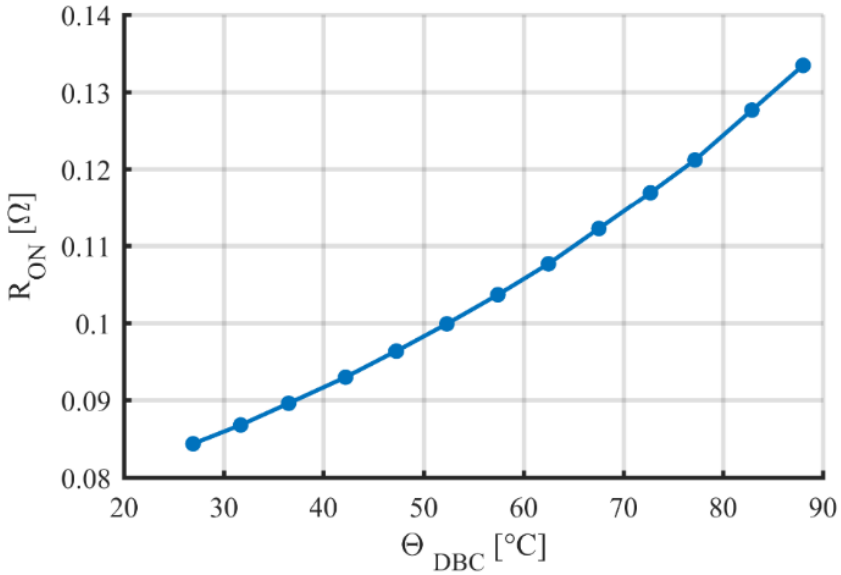


Fig. 5.5: $R_{ON}(\theta_{DBC}, i_{DS}$=15 A) from 15A-test commisioning, representative of the healthy module.

5.3 Accelerated Aging of the Compoent

To validate the proposed methodology, the switch SW1L is artificially aged through thermal cycling. Several techniques can be adopted to accelerate the aging process of a semiconductor. Depending on the aging technique, different typologies of failures can occur. In power devices, failures are often related to the packing and thermal cycling is recognized as one of the best aging methodology regarding the package related failure [69], [70]. The device under test is usually cycled between temperatures larger than those seen in normal operating conditions. The device can be heated passively by using an external heat source or actively by using the device own losses. **Passive thermal cycling** allows to control the temperature swings of the device with precision . **Active thermal cycling** does not allow a precise control of the thermal swings, but determines a more realistic temperature distribution.

In this thesis, the switch under test of module#2 has been aged by active power cycling. The reference duty cycle of LEG1 has been set to 0% (SW1L always close) with the load current controlled by LEG2 between 0 A to 21.5 A with a duty cycle of 50% and period of 4 s . After 15,000 thermal cycles (17 hours circa) the module has been characterized again. Two new look-up tables $\theta_J(R_{ON}, i_{DS})$ and $R_{ON}(\theta_{DBC}, i_{DS}{=}15\,\text{A})$ have been obtained. Fig. 5.6 shows the R_{ON} as a function of the **junction temperate** at i_{DS}=15 A, measured before and after the aging. The R_{ON} increase after 15,000 thermal cycles is around 1.6 mΩ, circa constant independently from the junction temperate. Fig. 5.7 shows R_{ON} as a function of the **DBC temperate** at i_{DS}=15 A, measured before and after the aging. In this case the increase of the R_{ON} after the aging is more pronounced and it is not constant respect to the DBC temperature. After the aging, the R_{ON} increase is around 10 mΩ when θ_{DBC} is 80 °C and around 4 mΩ when θ_{DBC} is 25 °C. For a certain DBC temperature, if the R_{ON} increases, it causes an increase of the conduction losses that in turn will further increase the junction temperature. In conclusion, the identification at 15 A and known DBC temperature is giving useful evidence of the aging of the component, and can be used for this specific purpose.

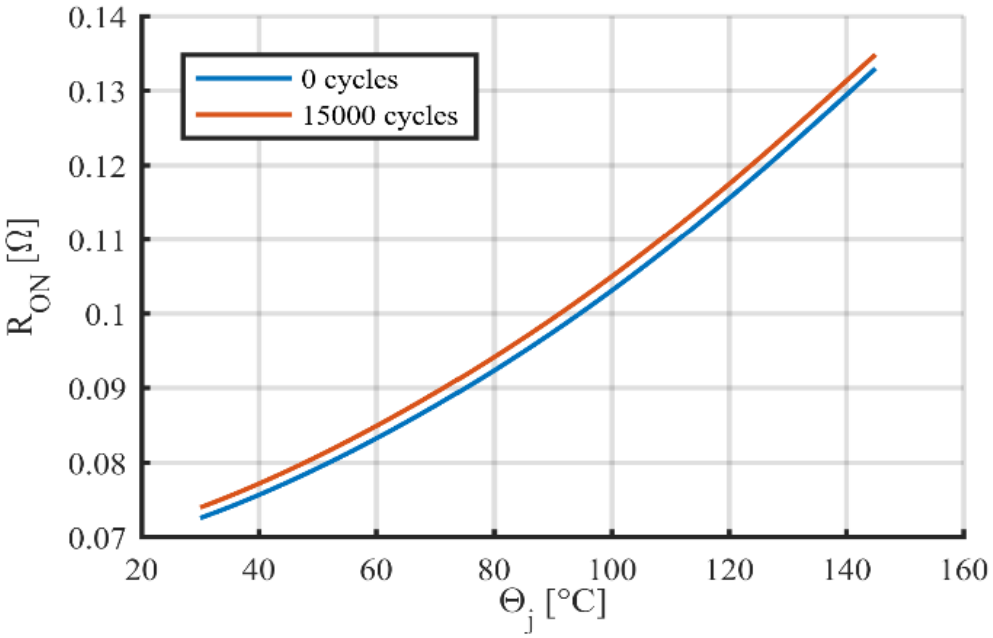


Fig. 5.6: $R_{ON}(\theta_J, i_{DS}$=15 A) before and after 15,000 cycles aging.

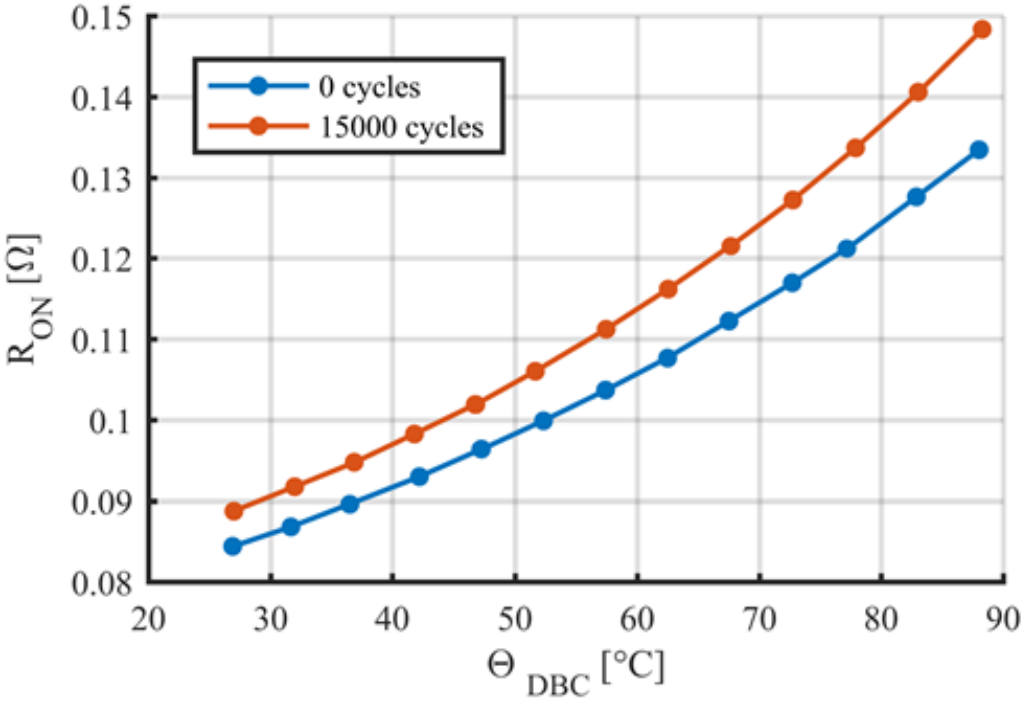


Fig. 5.7: 15A-test commisioning results $R_{ON}(\theta_{DBC}, i_{DS}$=15 A).

5.4 Effect of Aging on Temperature Estimation After 15,000 Cycles Aging

After the 15,000 thermal cycles the temperature is over-estimated by the "original" junction temperature look-up table. In Fig. 5.8 the aged power module is tested with a square wave load current ranging between 15 A to 20 A. The yellow line represents the temperature estimated using the "original" look-up table while the purple line represents the junction temperature estimated using an updated look-up table, i.e. by repeating the commissioning after the thermal cycles.

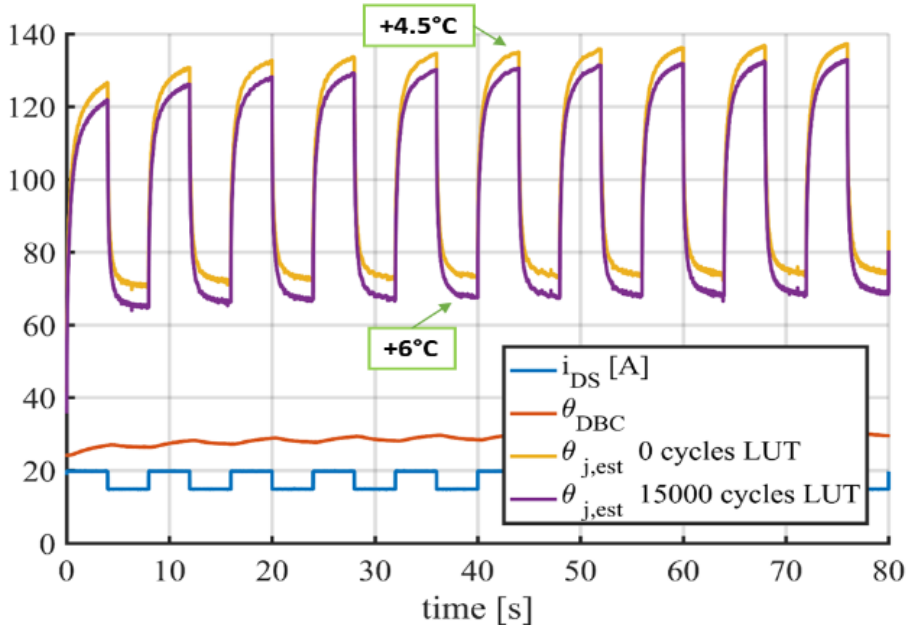


Fig. 5.8: Junction temperature estimation after 15,000 cycles aging. The orange line is the estimation of the junction temperature using the original LUT measured at the beginning of the life of the module. The purple line is the estimation of the junction temperature using the new LUT measured after the aging of the module.

In this example, the temperature overestimate is between 4.5 °C (high current) to 6 °C (low current). These results are consistent with the behaviour of the $R_{ON}(\theta_J)$ curve of Fig. 4.9, which slope increases with $\theta_{J,est}$. The temperature estimate becomes more imprecise at lower temperature respect to higher ones. Altogether, the effect of aging makes the temperature monitoring cautelative (+4.5°C around 120°C). Therefore, the temperature monitor becomes more and more conservative as the aging proceeds, progressively suggesting that the load current capability of the converter is no longer acceptable. The temperature monitor itself is already an indirect precursor or failure, thanks to the mentioned trend of overestimating the junction temperature. After another 2,000 thermal cycles, the switch

SW1L failed. This means that the analysed case is near to the worst case condition and also when the module is near to the failure the temperate over estimation is modest.

5.5 Direct Prognostics

The table $R_{ON}(\theta_{DBC}, i_{DS}{=}15\,\text{A})$ retrieved during the advanced commissioning test can be used to evaluate the aging of the switch SW1L. A simple test called the **15A-test** is proposed in this section. After the 15,000 cycle aging, during the idle time of the converter the same 15 A DC current used during the advanced commissioning test has been commanded to the load. After 10 s, i_{DS}, θ_{DBC} and V_{ON} have been measured. Fig. 5.9 shows the 15A-test time-wise, where the red cross indicates the sampling time (R_{ON} is shown instead of V_{ON}). The sampled R_{ON} at a DBC temperature of around 58 °C is then compared with the reference $R_{ON}(\theta_{DBC}, i_{DS}{=}15\,\text{A})$ curve as shown in Fig. 5.10. Compared to the original curve, the measured resistance for a DBC temperature of 58 °C increased by 5 mΩ. This deviation from the original curve is an evident precursor of failure for the switch under test. The 15 A-test can be performed at any time during the idle state of the converter.

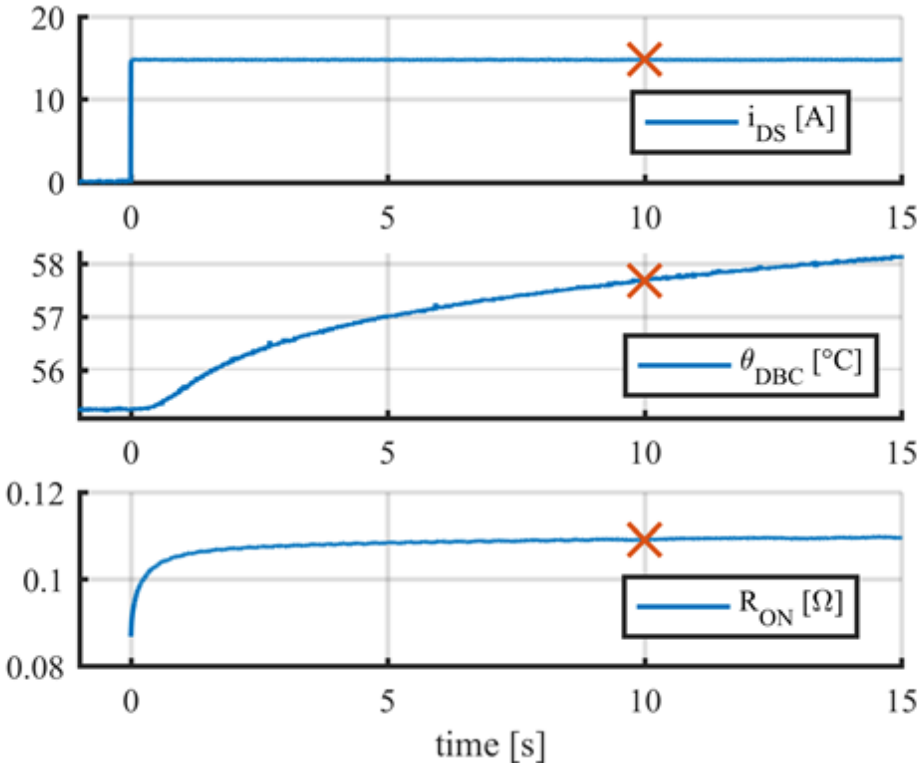


Fig. 5.9: 15A-test after 15,000 thermal cycles.

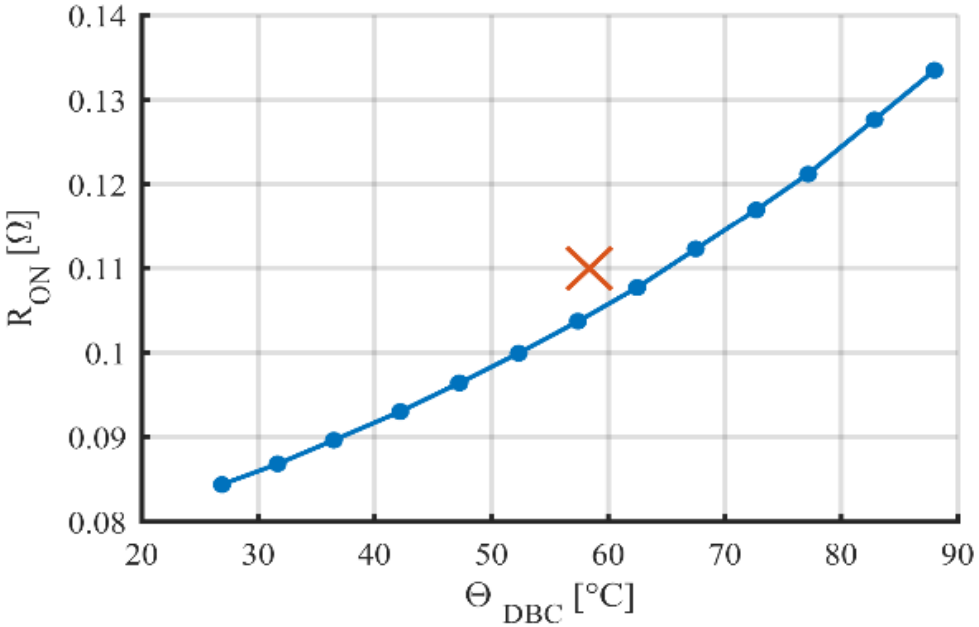


Fig. 5.10: $R_{ON}(\theta_{DBC}, i_{DS}$=15 A) after 0 thermal cycles vs 15 A-test after 15,000 thermal cycles.

5.6 Considerations About the Proposed Methodology

- Fig. 5.9 shows the θ_{DBC} waveform during the 15 A-test. The temperature evolution is dominated by more than one time constants, however two main dynamic stages are clearly visible in Fig. 5.9. Initially, a "fast" thermal transient with a time constant of around 1 s. A "slow" thermal transient due to the heatsink thermal inertia, with a time constant in the order of minutes. After the first 5 s the fast thermal transient is over, thus the temperature difference between the junction and the DBC can be considered constant **in the first approximation**. The 15 A current has been chosen so to guarantee a sufficient level of accuracy in the measurement. As stated many times before, the temperature estimation becomes imprecise for low values of drain current. On the other hand, if the current used for the test is too high, the device can be damaged during the commissioning at high DBC temperatures. For a device current of 20 A, the junction overtemperature respect to the DBC is more than 100 °C, as shown in Fig. 5.8. In turn, the device can be damaged if the commissioning is performed at 20 A. In this case, a possible solution can be to reduce the maximum DBC temperature used for the 15 A commissioning.

- According to Fig. 3.3, where the internal layout of the power module is shown, the embedded thermistor NTC1 is placed in the left lower corner of the power module. Unlike the short current pulses test, during the 15 A commissioning test the temperature gradient across the DBC is not negligible. To be able to compare the $R_{ON}(\theta_{DBC}, i_{DS}$=15 A) curve with the 15 A-test, in both cases, it is mandatory to have the same temperature distribution across the DBC. The losses between the four MOSFETs inside the power module during the 15 A commissioning have to be distributed likewise the losses in the 15 A-test. E.g. If during the 15 A commissioning the duty cycle of LEG0 is set to 0% and the duty of LEG2 is set to 5%, so also during the 15 A-test the two legs have to work with analogous duty cycle. Unlike the method used for the temperature estimation, the method used for the aging evaluation is sensitive to the thermal path. In fact, the thermal connection with the heatsink can influence the thermal distribution across the DBC. Upon noticing a significant mismatch between the measured R_{ON} using the 15 A test and the original $R_{ON}(\theta_{DBC}, i_{DS}$=15 A), the user can decide to replace the power module or to run a new commissioning test so to update the junction temperature map.

- According to different studies when the R_{ON} starts to increase the module is near the end of his life. In [71] where the same power module has been tested a substantial increase in the R_{ON} value has been measured before the component failure. The proposed method does not give any information about the failure mechanism. The R_{ON} increase depends on the failure mechanism that, in turn depends on the adopted aging technique and on the manufacturing process of the device. E.g If the bonding wires are damaged the R_{ON} increase is modest, because their resistance accounts only for a small part of the total R_{ON} resistance [69].

In conclusion thanks to the V_{ON} measurement, the health state and the junction temperature of the semiconductor can be estimated. The presented health monitoring solution needs to be further developed, so far it can't give precise informations about the residual lifetime of the semiconductor. The aim of this research was to demonstrate the feasibility of the solution in a commercial converter. A lot of work has still to be done and an exhaustive series of tests have to be conducted before implementing the proposed solution in a real case scenario.

Chapter 6

3-PH SiC Inverter for Student Formula Electric

Following the good results obtained with the POC test rig, the developed technology was applied to a real-world custom designed converter. A new SiC MOSFET inverter with on-line temperature estimation has been designed for the "Squadra Corse" of the Politecnico di Torino [72]. Squadra Corse is a student racing team that competes in formula SAE, an international student formula competition organized by SAE international [73].

The first edition of Formula SAE was held in 1981 in USA with six student teams attending. Arrived in Europe in the early 2000s, Italy saw its first edition in 2005. Today formula SAE has grown in importance with hundreds of teams from all over the world and with different branches from autonomous driving to aero design. The Squadra Corse competes in the Formula SAE electric, that is reserved to full electric vehicles. In order to participate to the formula SAE electric the car has to satisfy a series of technical and safety requirements, as explained in the next sections. Fig. 6.1 shows the prototype car for season 2018, while the car for the new season is currently under design.

Fig. 6.1: Previous version of the Squadra Corse prototype race car.

6.1 Description of the Race Vehicle

The car has four motorised wheels and four respective inverters. Fig. 6.2 shows one wheel with the electric motor. Between the wheel and the motor there is a planetary.

6.1.1 AMK Motor Drive Package

The AMK supply a "racing kit" for the formula SAE consisting of four AMK motors and one quad inverter. The current version of the race car of the Squadra Corse is equipped with the inverter provided with the racing kit. This is the "off the shelf solution" adopted by most of the teams that compete in formula SAE electric.

The adopted PM synchronous motor model **DD5-14-10-POW** is by AMK, the main specifications are reported in Table 6.1. It weighs 3.55 kg and its dimensions are reported in Fig. 6.3. With reference to the datasheet, the maximum RMS current is equal to 105 A, corresponding to a peak value of 148.5 A. The maximum mechanical speed is 20000 rpm, thus corresponding to a maximum electric frequency of 1667 Hz (5 pole pairs). It is a permanent magnet synchronous motor with high power density. However, in the flux weakening speed range (i.e. high speed) a substantial part of the current is spent for flux weakening. Fig. 6.4 shows the maximum torque versus speed and maximum power versus speed profiles of

the AMK motor drive under different maximum voltage limits, corresponding to different state of charges of the battery pack. The battery voltage range is from 350 V (full discharge) to 600 V (full charge). The torque profiles show that flux weakening begins at 16000 rpm when the DC-link (i.e. the battery) is 600 V and 13000 rpm at 500 V. The peak power, with 600 V, is 36 kW at 600 V and 30 kW at 500 V.

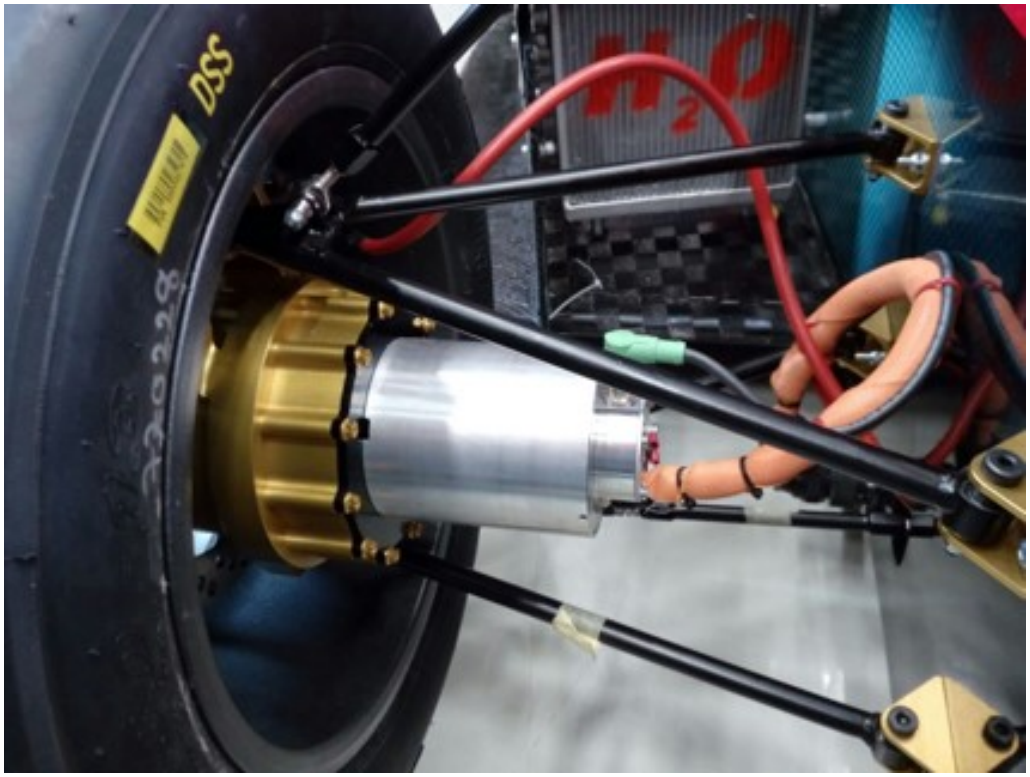


Fig. 6.2: One of the motorized wheels.

Table 6.1: IPM motor model: DD5-14-10-POW.

Rated Torque	9.8 Nm
Stall Torque	13.8 Nm
Maximum Torque	21 Nm
Rated Speed	12000 rpm
Maximum Speed	20000 rpm
Rated Power	12.3 kW
Rated Phase Voltage, pk	350 V
Rated RMS Current	41 A
Stall RMS Current	53.1 A
Maximum RMS Current	105 A
Number of Poles	10
Terminal Resistance	0.135 Ω
L_q	0.12 mH
L_d	0.24 mH
Cooling Type	"Liquid"
Motor Mass	3.55 kg

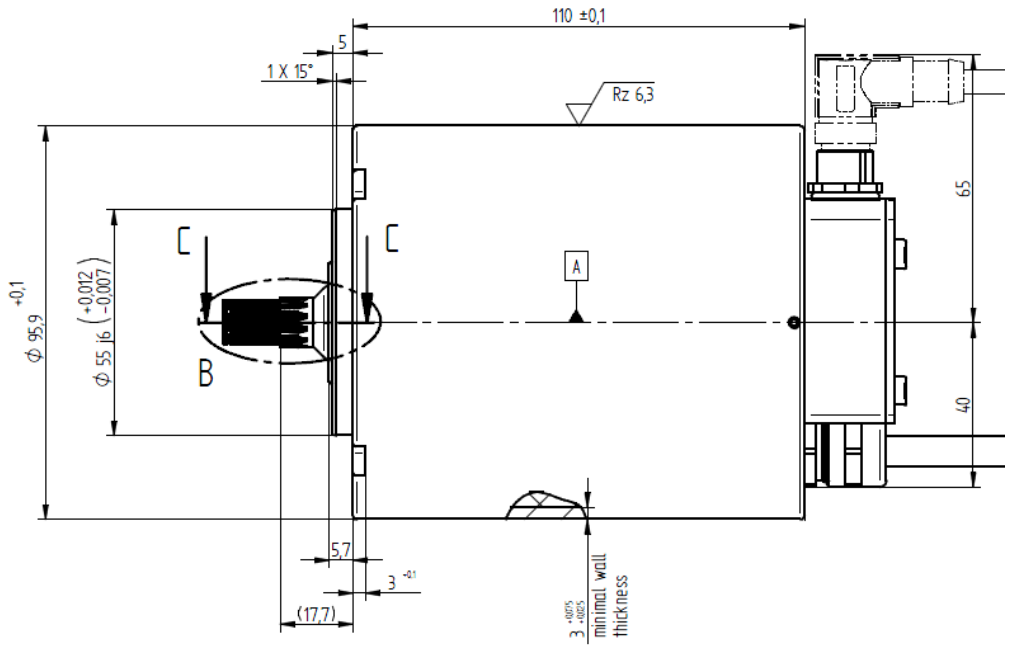


Fig. 6.3: Mechanical drawing of AMK motor model: DD5-14-10-POW.

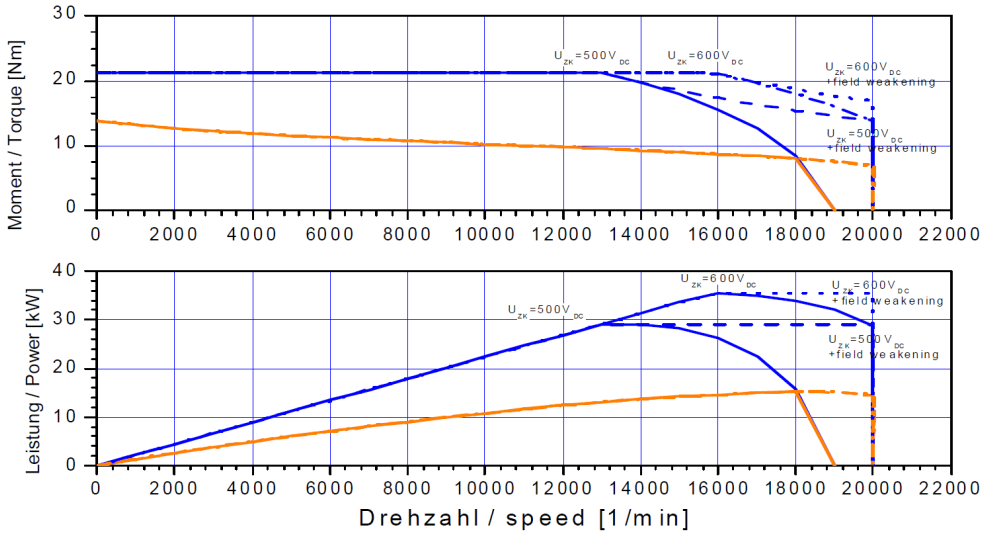


Fig. 6.4: Maximum Torque (top) and power (bottom) versus speed characteristics at maximum current and different DC-link voltage values.

The AMK inverter is shown in Fig. 6.5, it consists of a quad inverter with integrated drive controllers enclosed in one box. The central metal plate is the liquid cooled heatsink, on top of that there are two inverters and under that, the other two inverters. The inverter package is designed to be placed in the rear part of the car.

Each inverter uses a three-phase IGBT power module, model FS200R12PT4 from Infineon. The rated current for this module is 200 A (T_c=95 °C) and the breakdown voltage is 1200 V.

The AMK off the shelf solution is easy to implement but it has a series of drawbacks:

- All four inverters are enclosed in one package, whereas four separate modules would permit to distribute masses and volumes with more flexibility .
- The firmware is proprietary and the team can modify just a restricted number of parameters.
- The switching frequency of 8 kHz is rather low respect to the motor fundamental frequency.
- The schematic of the inverter is not released.
- The debugging tools are not sufficient.
- All such turns into reliability problems. It is not unusual that one module fails, and it is not always clear why.

Having all the four inverters in one package permits to use one heatsink for all the modules. However, this solution does not allow a good weight distribution, as said in this configuration the quad inverter has a weight of approx 11 kg. The four-inverter package is placed in the rear part of the car, where most of the weight is due to the presence of the battery pack, and distant from the four wheels, in particular from the two in the front. The dimensions of the four pack inverter are around 241 x 339 x 183 mm. Having the inverter away from the motors worsens the EMI emissions and the use of long cables can lead to over voltages problems.

The second bullet point is about the impossibility to modify the firmware for the motor control. A custom motor control firmware can be a major advantage in terms of performance and efficiency especially if associated to the OFF-line characterization of the electric motors.

The switching frequency for this inverter it is 8 kHz and the electric motor has a maximum fundamental frequency of 1666 Hz. It is a good rule of thumb to run the control with a frequency **at least** 10-20 times higher than fundamental one. Probably the AMK control uses "double sampling, double refresh" therefore a sampling frequency of 16 kHz. This is barely enough to maintain the control of the electric machine at maximum fundamental frequency.

The schematics of the inverter are unknown and the debugging tools made available by the inverter manufacturer are basic: this makes it hard to find the problem when a fault occur. Also, fixing the inverter without the schematics can be difficult and sometimes impossible. For this reason it is necessary to keep a good number of spare inverters.

The last problem is related to the low reliability, due to the fact that the inverter works in an extremely harsh environment. In order to maintain the weight of the vehicle as low as possible the cooling system is down to the bare bones. On top of that the inverter has to work in overload conditions during the acceleration and deceleration phases. Unexpected failures have often occurred, and sometimes the cause of the failure remained unknown. In some cases catastrophic failures of the IGBT modules occurred, forcing the replacement of one or more inverters.

Table 6.2: AMK inverter power ratings.

Input voltage range	$250 - 720\ V_{DC}$
Supply voltage for logic supply	$24\ V$
Efficiency	$\approx 98\ \%$
Switching frequency	$8\ kHz$
Rated output current I_N	$43\ A$
Peak output current I_{max}	$105\ A$
Max. duration of peak output current I_{max}	$10\ s$
Max. cold plate and ambient temperature	$40°C$

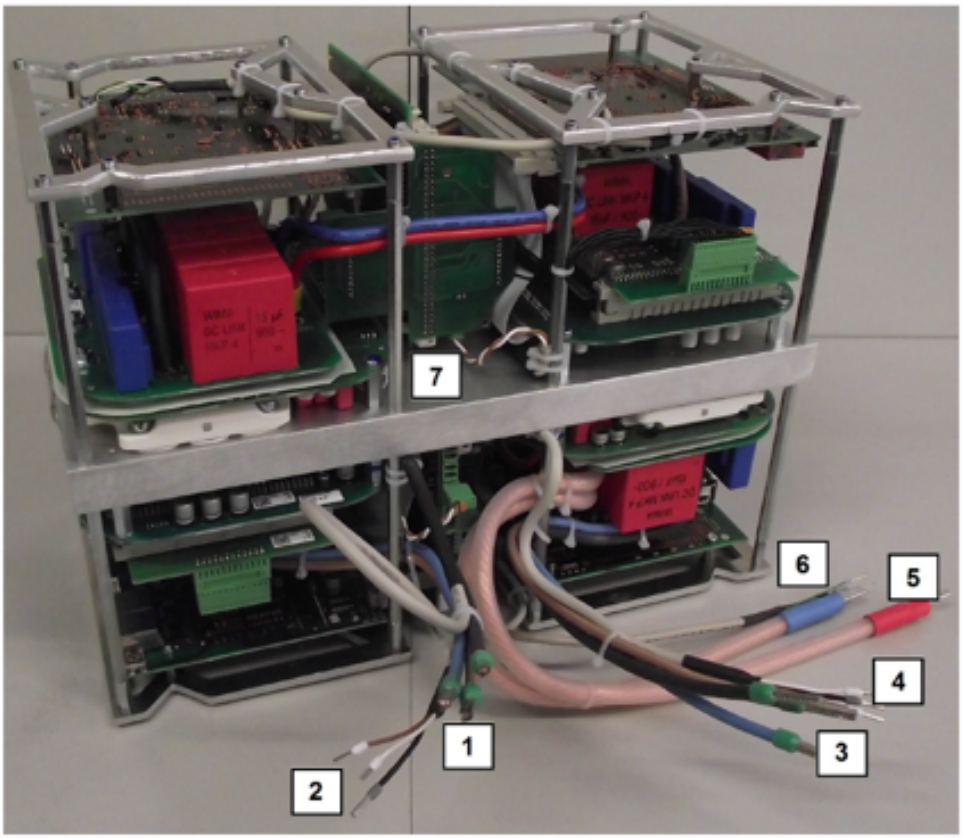


Fig. 6.5: Commercial inverter produced by AMK.

6.1.2 Key Regulations of Formula SAE Competitions

To compete in formula SAE, the vehicle has to satisfy a series of technical requirements [74]. The regulation refers mainly to vehicle safety. Concerning the electrical part the main constraints are:

- "A firewall must separate the driver compartment from all tractive system components, including any high voltage wiring."
- "The maximum allowable power that can be drained from the batteries is 80 kW."
- "The maximum permitted voltage that may occur between any two points must not exceed 600 V DC."

The car dynamic performance (dynamic events) and the design (static events) are evaluated. The main **dynamic events** are [75]:

- **Acceleration.** The vehicle has to speed up to the maximum acceleration for 75 m. The score depends on the time.
- **Skid Pad.** The vehicle has to run on a track that looks like an "8". The ability to turn of the car is evaluated and the lateral speed up is measured.
- **Autocross.** The vehicle has to complete two laps of a track in the shortest time possible. The average speed is between 30 km/h to 40 km/h. The score is given by the best lap time.
- **Endurance.** The vehicle has to drive 22 km on a circuit similar to the one used for the Autocross event. The score depends on the total time.

The main **static events** are [76]:

- **Design Event.** The project of the vehicle is evaluated. The main categories of evaluation are: suspension, chassis and engine.
- **Business Event.** A simulation where the car is presented in front of potential sponsors. The score depends on the ability of the team to develop a business plan.
- **Cost Event.** The bill of materials of the vehicle is analysed and the total cost is computed. The total cost and the sustainability of the project are evaluated.

6.2 New SiC MOSFET Inverter for Formula SAE

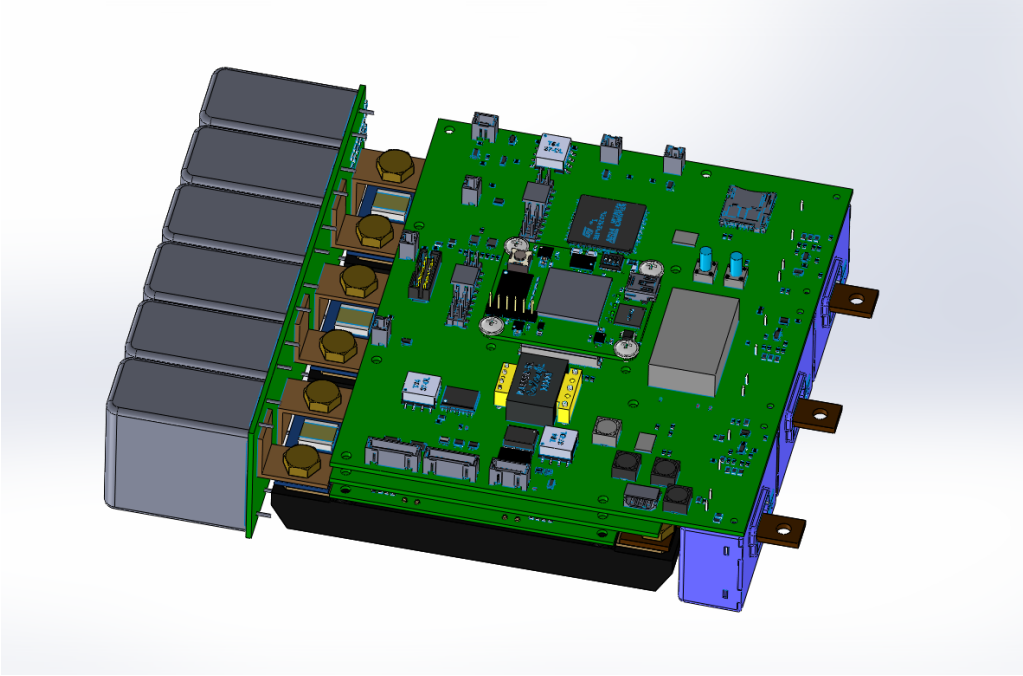


Fig. 6.6: Assembly of the power converter.

This chapter describe the design of the new high power density SiC power MOSFET inverter for the new racing car prototype of the Squadra Corse. The inverter is equipped with an improved version of the V_{ON} measurement system, that is used for the junction temperature estimation of the MOSFETs inside the power modules. All six MOSFETs of the inverter are identified and real-time monitored. Fig. 6.7 reports the schematics of the power stage of the inverter, with indication of the currents and Drain-Source voltages of the six power devices, that are measured.

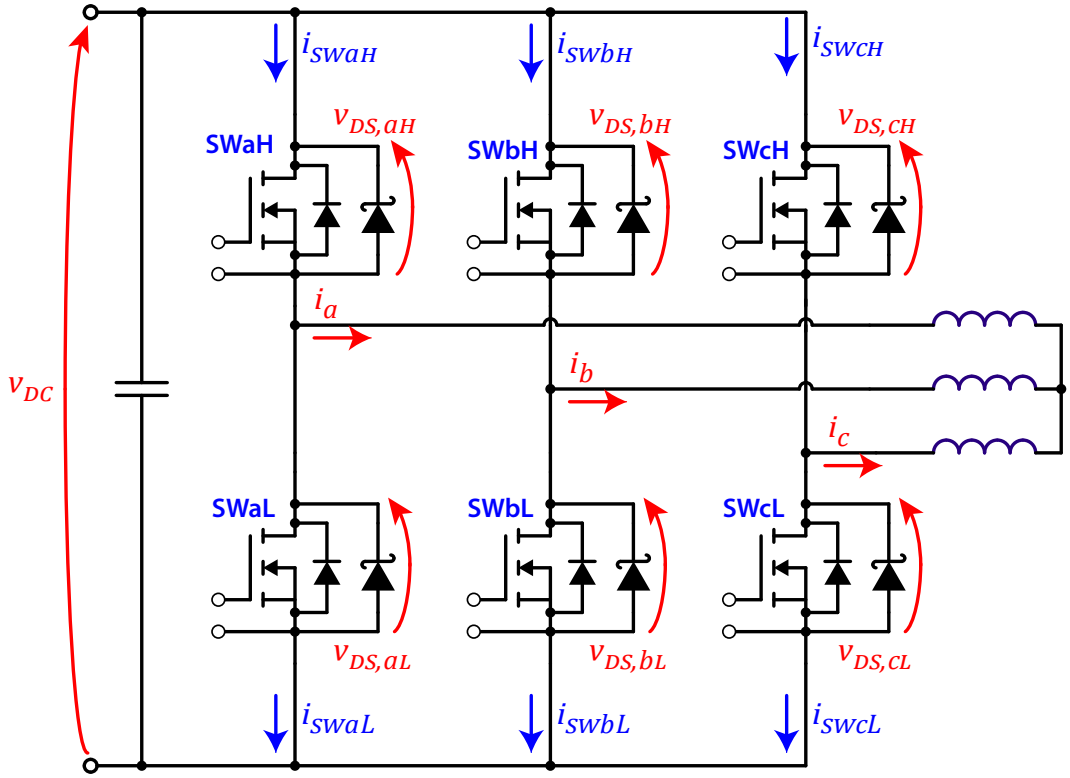


Fig. 6.7: Inverter schematic. Red quantities are measured online.

6.2.1 Mechanical Layout

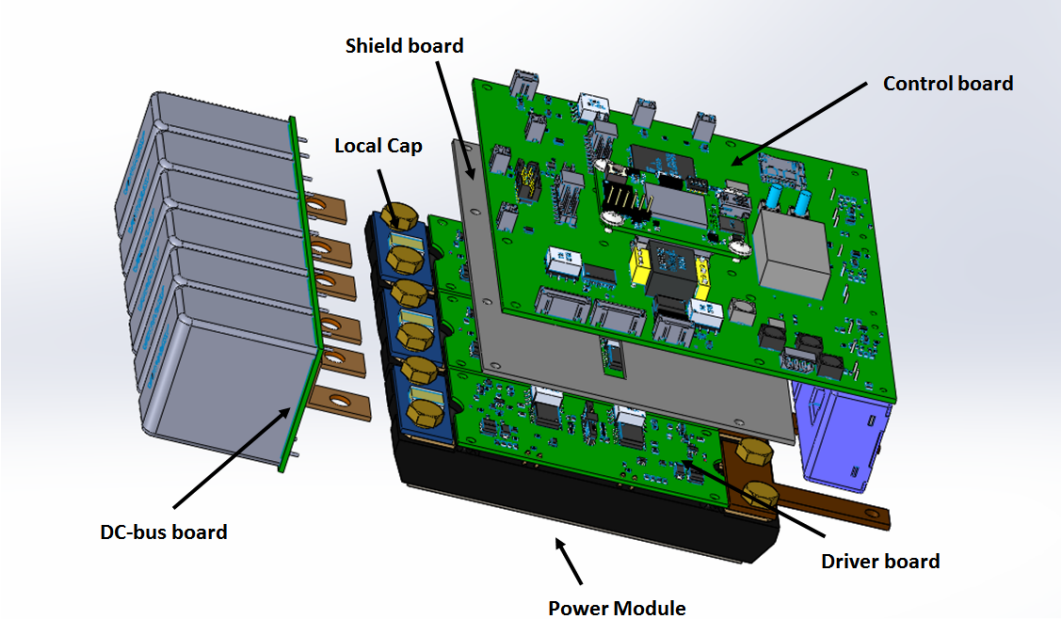


Fig. 6.8: Exploded view of the power converter.

The mechanical design has been carried out using Solidworks and Altium Designer. Fig. 6.8 shows the exploded view of the power converter, where it is possible to identify the main components:

- DC-bus Capacitors Board.
- Power Modules.
- Driver Board.
- Shield Board.
- Local Capacitors Boards.
- Control Board.

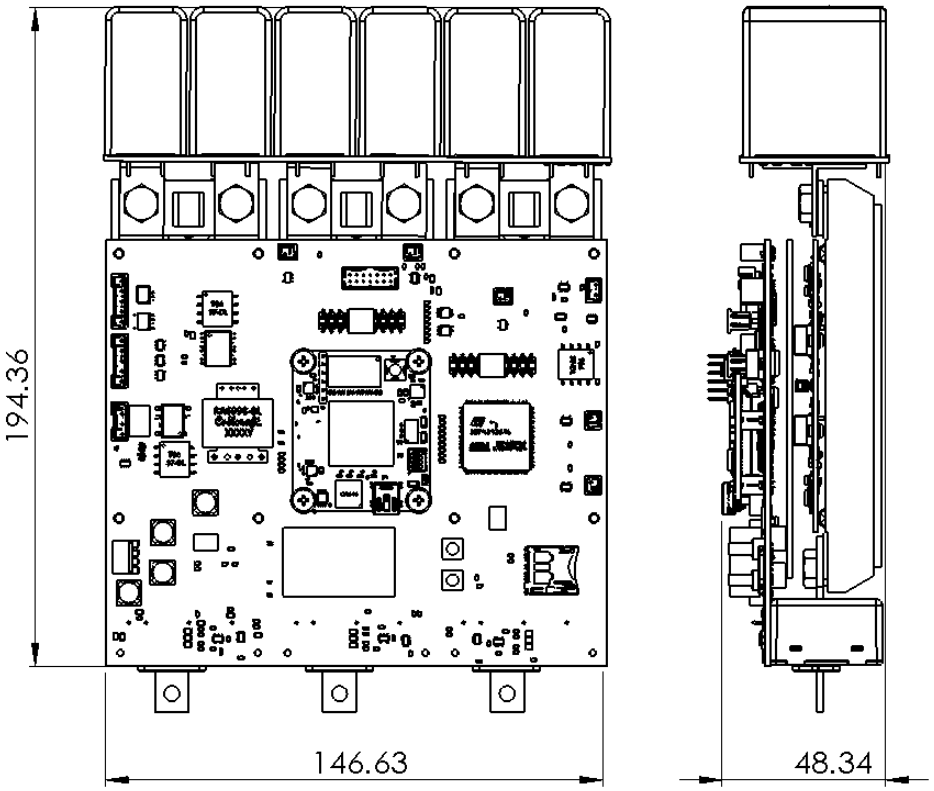


Fig. 6.9: Mechanical drawing of the inverter (dimensions in mm).

6.2.2 3-Phase Power Modules

The market offers a range of SiC Power MOSFET modules, however only a few models are currently available for high currents. To achieve a high level of power density the first choice was the power module model: APTMC120TAM12CTPAG produced by Microsemi, consisting of a three-phase SiC MOSFET bridge. This module is extremely compact (108 x 62 x 11.5 mm), permitting an extremely high power density. This solution presented, however, a couple of drawbacks:

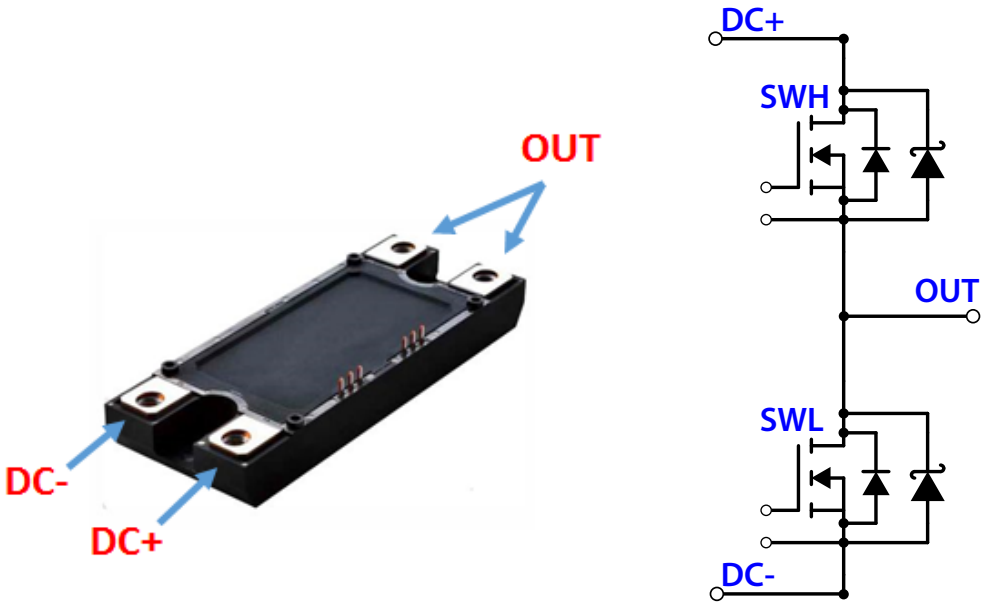
- Due to the small size of the module, the space for the gate drive circuitry and for the V_{ON} measurement system is not sufficient unless multiple overlapped boards are used. This solution would cause an increase on the vertical dimension of the inverter and it would require additional connectors between the boards.
- The heat exchange surface is small if compared to a single leg module, this results in a higher thermal resistance between case and heatsink. This can

be critical because the car cooling system is undersized to keep the vehicle as light as possible.

For this reason a solution with single-leg modules has been preferred. The main semiconductors manufacturers offers similar products in terms of performance and dimensions. The power module model BSM180D12P3C007 produced by ROHM semiconductors was chosen, mainly because of the favourable pinout. The ROHM power module is shown Fig. 6.10a. It is possible to observe that the DC bus pins are on one side of the module while the output pins are on the other side of the module. The power module ratings are shown in Tab. 6.3 .

Table 6.3: Power Module BSM180D12P3C007.

Breakdown Voltage	1200 V
$\mathbf{I_D}$ **($\mathbf{T_c}$= 60°C)**	180 A
$\mathbf{I_{D,pulse}}$ **($\mathbf{T_c}$= 60°C, 1ms)**	360 A
$\mathbf{T_{j,max}}$	175°C
$\mathbf{T_{j,operative}}$	150°C
$\mathbf{R_{DS,ON}}$ **($\mathbf{T_j}$=25°C, $\mathbf{I_D}$= 180 A)**	10 $m\Omega$
$\mathbf{R_{DS,ON}}$ **($\mathbf{T_j}$=150°C, $\mathbf{I_D}$= 180 A)**	17 $m\Omega$
Size	45.6 x 122 x 17 mm



(a) Package. (b) Circuit diagram.

Fig. 6.10: SiC power module model:**BSM180D12P3C007**.

Fig. 6.10b shows the schematic of the power module. It is possible to notice the presence of SiC diodes in anti parallel to the power MOSFET. The diodes improve the commutation dynamics: the same power module without the anti parallel diodes is available on the market (model: BSM180d12p2c101). Fig. 6.11 shows the internal layout of the power module. Each MOSFET and each diode is made up of six dies connected in parallel.

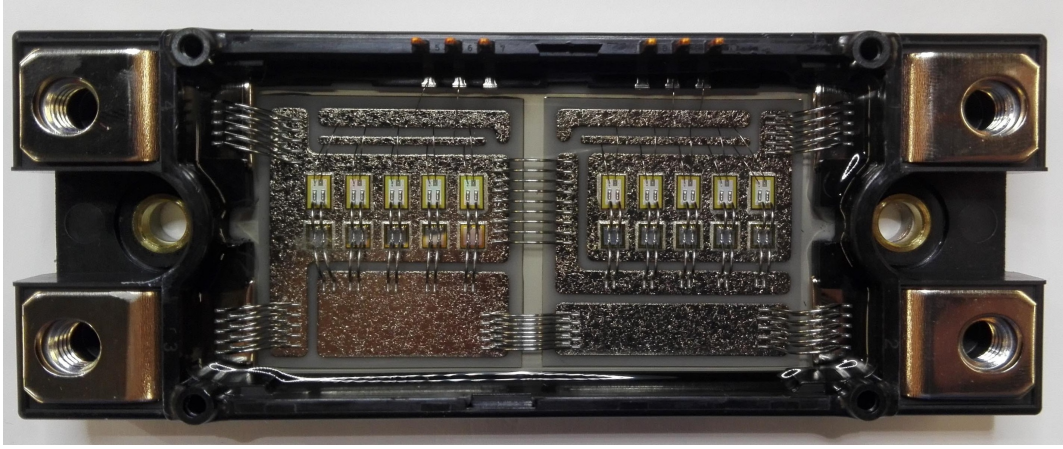


Fig. 6.11: Internal layout of the power module.

6.2.3 Driver Board Design

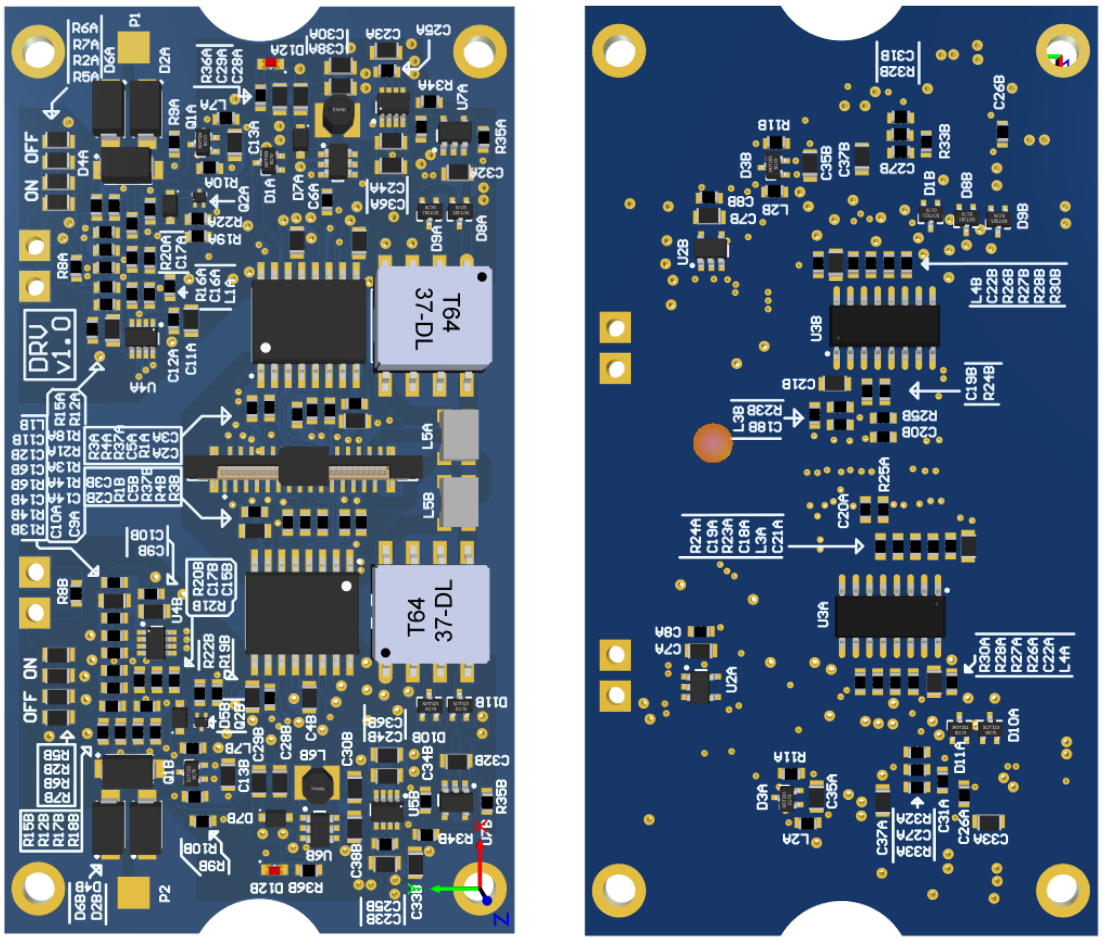
Custom gate driver boards have been designed, capable of measuring the V_{ON} voltages of the SiC MOSFETs.

The driver boards match the power modules layout as shown in Fig. 6.13: each board commands one inverter leg. The V_{ON} measurement system is illustrated in Section **??** while the power supply system is illustrated in Section 6.2.6.

The gate drive system uses the isolated driver ADuM4135 by Analog Devices. This commercial solution integrates the desaturation protection and permits to command on the gate of the MOSFET positive and negative voltages with a maximum current of 4 A. The ADuM4135 provides galvanic insulation with a common mode transient immunity of 100 kV/µs, which is very important when wide-bandgap devices are used. The gate voltage commanding the ON-state is +18 V. The OFF-state is commanded with -2 V. These two values are the ones suggested in the datasheet. The datasheet recommends to use different gate resistances for the turn-ON and for the turn-OFF, the minimum value suggested from the datasheet have been used: $R_{G,ON}$=8 Ω and $R_{G,OFF}$=5 Ω.

Ideally the commutations should be as fast as possible, however problems such as EMI emission, turn-OFF overvoltages, turn-ON overcurrents (due to the reverse recovery of the diode) and partial discharges between the windings of the electric

machine can occur. The gate resistances can be easily modified during the validation test phase of the inverter. To maintain the size of the driver board as small as possible a six-layer PCB has been designed, with the components placed on both sides as shown in Fig. 6.12. The driver boards are connected to the control board using a 30-pin flat cable. This solution permits to interconnect the two boards without tight manufacturing tolerance requirements. A commonly used solution for this kind of inverters would be using board-to-board connectors, but this would require very tight manufacturing tolerances, as said.



(a) Top view. (b) Bottom view.

Fig. 6.12: Driver board, both sides.

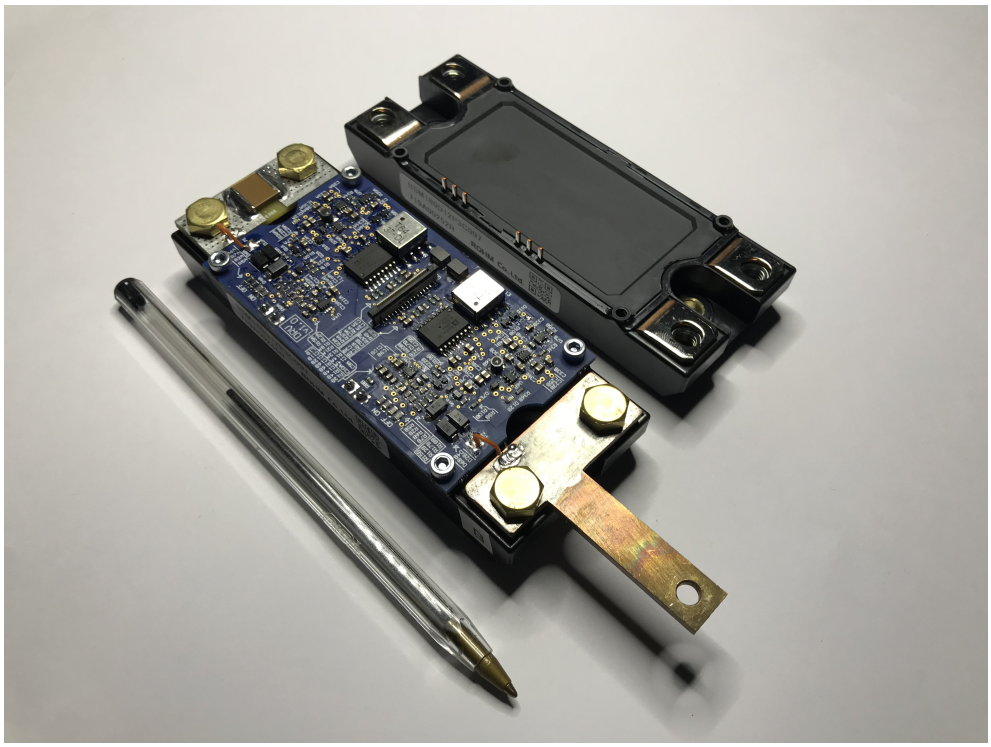


Fig. 6.13: Power modules, driver board, local capacitor board and output busbar.

6.2.4 Control Board Design

The control board shown in Fig. 6.14 is mounted on top of the converter. For having maximum flexibility on the control and plenty computational power, an hybrid architecture microcontroller-FPGA has been adopted. The microcontroller handles the motor control task, whereas the PWM modulation, the measurement and the hardware protections are carried out by the FPGA. The FPGA and the MCU communicate using four full duplex SPI lines and two GPIO pins, used for interrupt requests. The control board functional diagram is shown in Fig. 6.15.

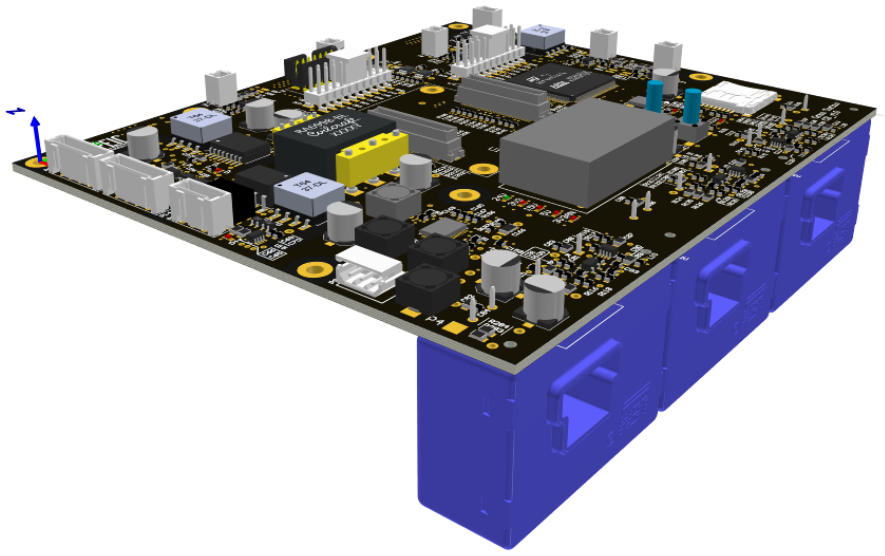


Fig. 6.14: Control board with current transducers.

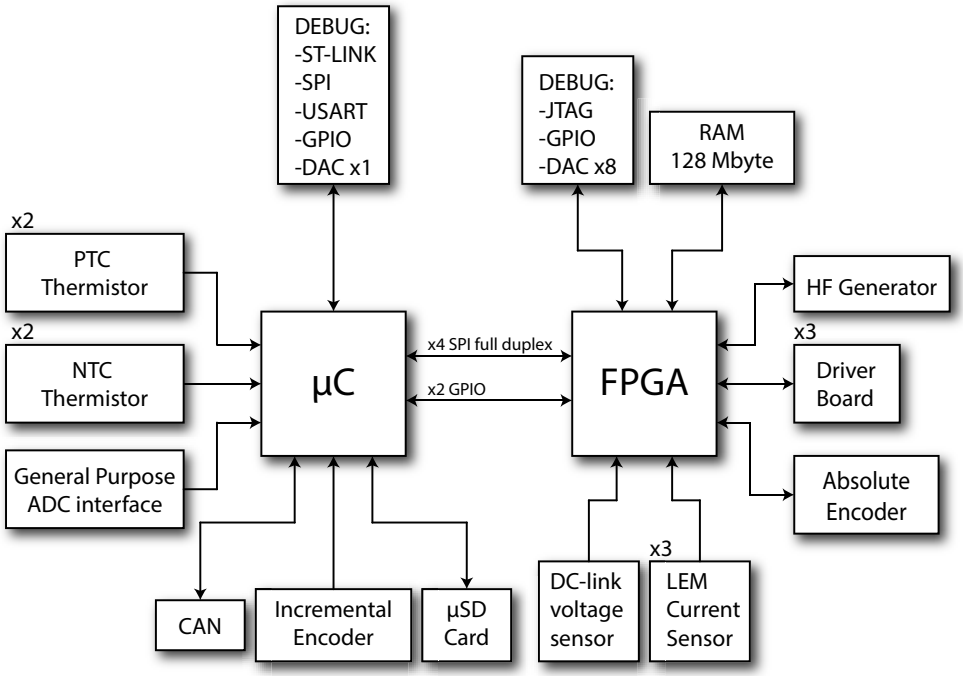


Fig. 6.15: Control board functional diagram.

The **STM32H743ZI** MCU by STMicroelectronics employs a CortexM7 core

with a clock frequency up to 400 MHz and FPU (Floating Point Unit) . The MCU was selected for ease development, although it is not automotive grade. A wide range of embedded pheripherals are embedded on the microcontroller, such as:

- DMA (Direct Memory Access)
- SPI (#6)
- USART (#8)
- Timers and Counters (#14)
- FMC (Flexible Memory Controller)
- Quad SPI (#1)
- 16 bit ADC (#3)
- DAC (#1)
- Watchdog Timer
- Analog Watchdog
- CAN (#2)

Instead of soldering the FPGA directly on the control board the FPGA module model **TE0630-01IBF** by Trenz Electronic has been used. This FPGA module embedded a **XC6SLX75-2CSG484I Spartan 6 FPGA** by Xilinx, plus a 128 $Mbyte$ RAM memory, a 16 $Mbyte$ flash memory, a USB transceiver and all the necessary voltage regulators. The Trenz module is extremely compact and avoids routing the 484 pins of the FPGA.

Moreover, the control board embeds different sensors and additional circuitry:

- Three LEM current transducers with current output, the analog signal conditioning circuitry and the local 14-bit ADC. In Fig. 6.14 are visible the three LEM current transducers (three blue boxes) .
- A DC-link voltage sensor consisting of an operational amplifier in differential configuration and a 14-bit local ADC with galvanic insulation.
- Incremental encoder interface compatible with the standard EnDat 2.2 used for HEIDENHAIN encoders. This interface permits bidirectional communications between the encoder and the control board, it uses a differential clock line and a differential data line. Two galvanic insulated RS-485 transceivers are present on the control board. This peripheral is connected directly to the FPGA because the microcontroller does not handle EnDat communication.

- A insulated CAN interface that meets the specifications of the ISO11898-2 standard. This interface is connected to the microcontroller embedded CAN unit.
- An incremental encoder interface, that can be configured to accept differential or single-ended signals from the encoder.
- Two PTC thermistor interfaces, consisting of the analog conditioning circuitry used for measuring the **PTFM101T1A0** thermistor, placed on the heatsink. The analog output from this interface is connected to the internal ADC of the microcontroller.
- Two NTC thermistor interfaces, consisting of the analog conditioning circuitry used for measuring the **NTCALUG01A103F800** thermistor, placed on the heatsink. The analog output from this interface is connected to the internal ADC of the microcontroller.
- A general ADC interface consisting of the analog conditioning circuitry whose output is connected to the internal ADC of the microcontroller. This interface can be used for future developments of the inverter and can work in different configurations.
- A µSD card slot that can be used to store data on an external flash memory. This permits to record data in operation can be used as a "black box" for off-line investigation.
- The microcontroller debug interface consisting of of one SPI, one USART, one DAC, one ST-link interface and four GPIOs.
- A HF power supply for on-board auxiliaries, illustrated in detail in Section 6.2.6.
- The FPGA debug interface consisting of one JTAG, seven GPIOs and eight DACs.
- The gate driver interface consisting of all the needed signal for communicating with the driver boards. Fig. 6.17 shows the bottom part of the control board, where the three flat connectors J1, J2 and J3, used for connecting the three drivers boards are visible.

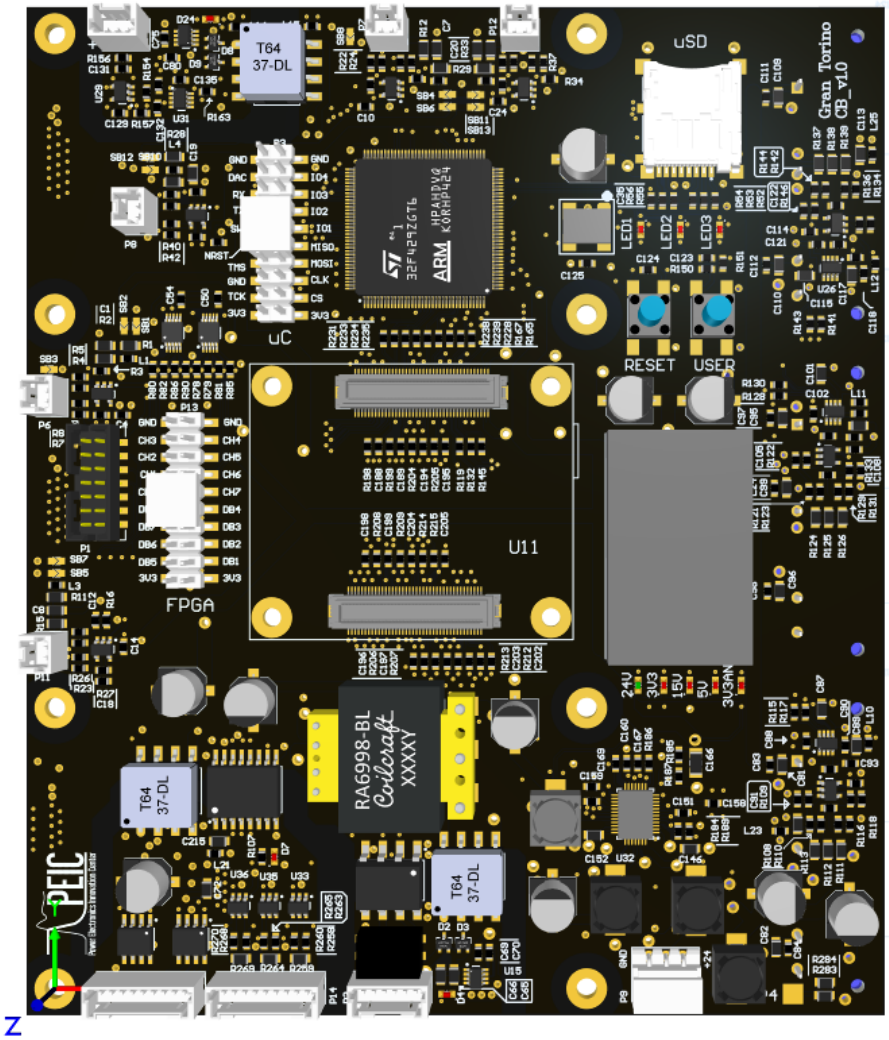


Fig. 6.16: Control board top side.

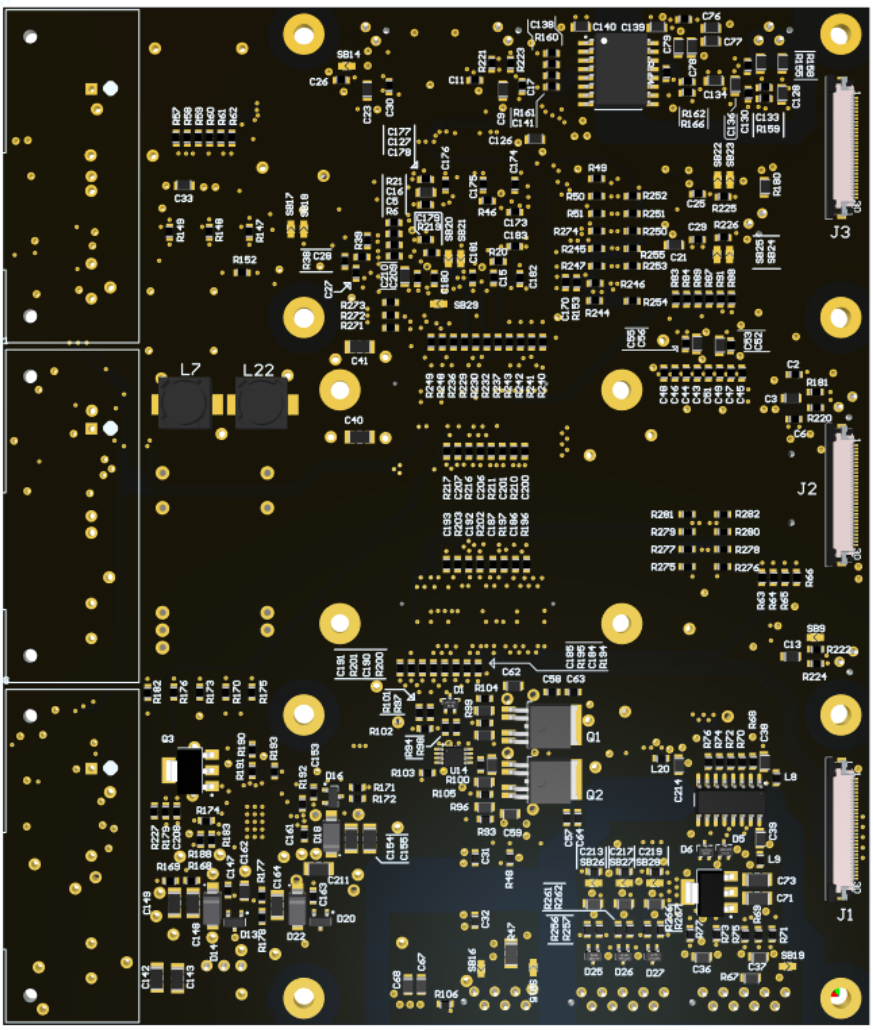


Fig. 6.17: Control board bottom side.

6.2.5 Capacitor Boards Design

The DC-link capacitors board assembly is shown in Fig. 6.18. It is placed in proximity of the DC connectors of the power modules as shown in Fig. 6.8. The board contains six polypropylene film capacitor model **MKP1848C62090JP4** by Vishay. The main characteristics of the capacitors are reported in Tab. 6.4. The total DC-link capacitance is 120 μF and the maximum RMS current is 84 A. A second board denominated "local capacitor board", houses a ceramic capacitor model 3640AC224KAT3A as shown in Fig. 6.19. This board is placed as close as possible to the DC pins of the power module as shown in Fig. 6.20. A total of three local capacitor boards are present, one for each power module. The ceramic capacitor has a nominal capacitance of 220 nF and a resonance frequency of 20 MHz (Table 6.5). The ceramic capacitors permit to minimize the stray inductance of the commutation loop, thus avoiding over voltages and ringing effects.

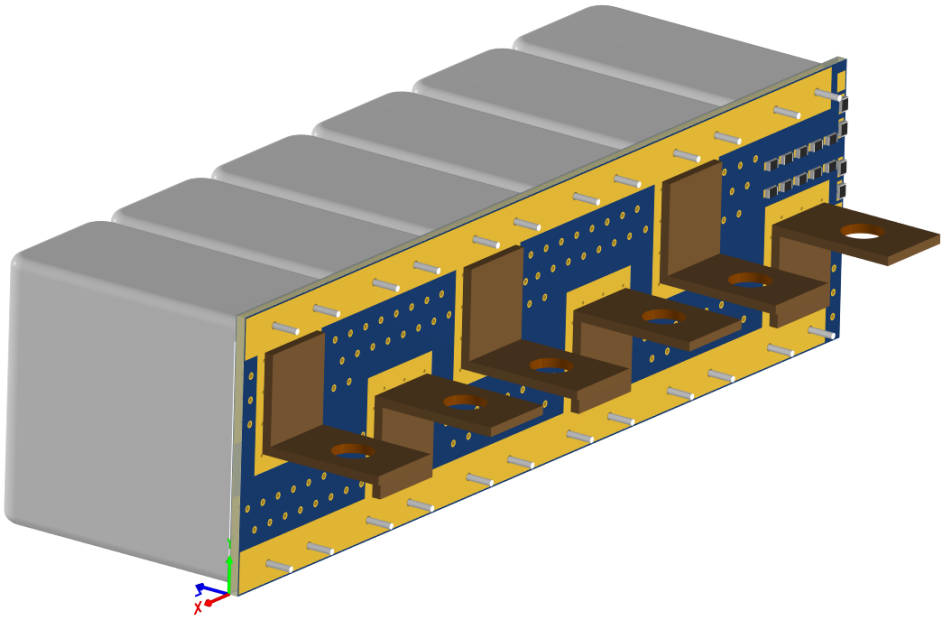


Fig. 6.18: DC-link capacitors board.

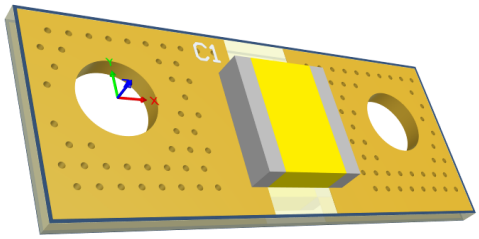


Fig. 6.19: Local capacitor board.

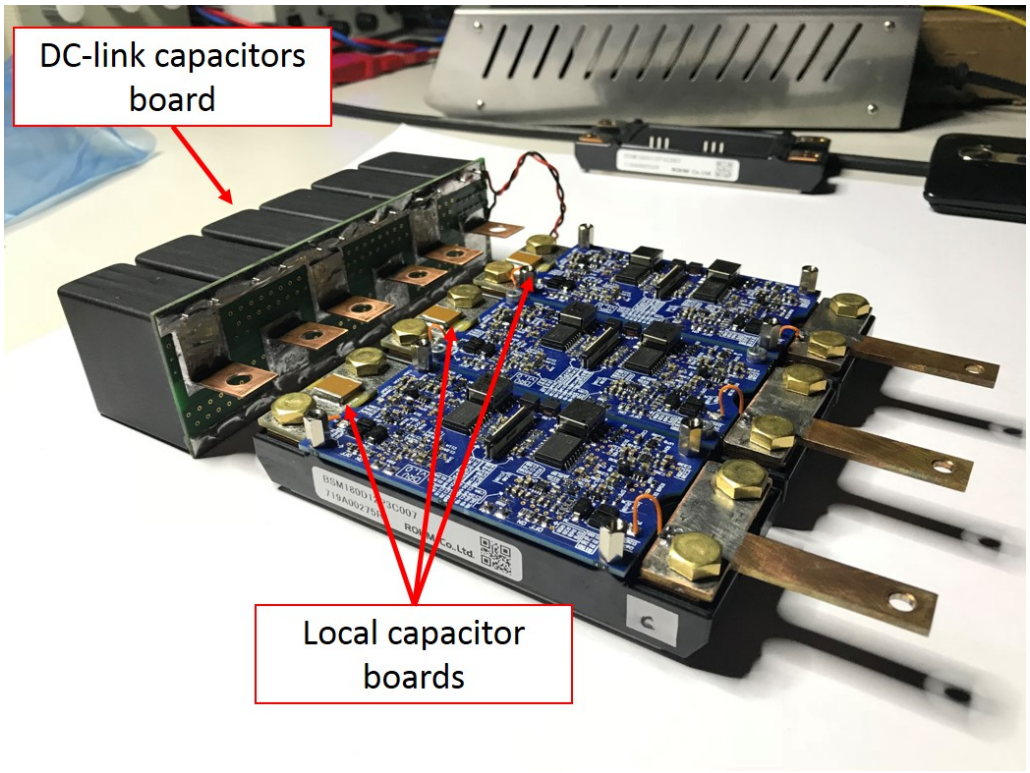


Fig. 6.20: Power module, driver boards, local capacitor boards, output busbar and capacitor board.

Table 6.4: Capacitor: MKP1848C62090JP4.

$\mathbf{C_{rated}}$	20 µF
$\mathbf{U_{NDC}}$ **(T$_A$=85 °C)**	900 V
$\mathbf{I_{RMS}}$ **(T$_A$= 85 °C)**	14 A
$\mathbf{I_{peak}}$	700 A
ESR	5 $m\Omega$
dv/dt	35 $V\mu s$
$\mathbf{f_{resonance}}$	$\approx$ 300 kHz
Dielectric	Polypropylene
Size	24 x 44 x 42 mm

Table 6.5: Capacitor: 3640AC224KAT3A.

$\mathbf{C_{rated}}$	220 nF
$\mathbf{U_{NDC}}$	1000 V
$\mathbf{f_{resonance}}$	$\approx$ 20 MHz
Dielectric	$X7R$
Package (inch)	3640

The DC-link capacitors are one of the bulkiest components of the inverter. To save space the designer would like to keep the DC-link capacitance as small as possible. The main constraints in this respect are:

- The maximum RMS current size of the capacitors.
- The maximum voltage ripple.
- Resonance frequencies.

The RMS current that the capacitors absorbs varies with the motor operating point and the battery voltage. The RMS current in the capacitor can be computed by numerical simulation. The hypotheses behind this analysis are:

- Sinusoidal PWM with third harmonic injection (or SVM).
- Sinusoidal phase currents, peak value of 180 A and balance load.
- Constant DC-link voltage.
- The whole AC component of the inverter input current is absorbed by the capacitors, whereas the DC component is provided by an external power source.

The inverter input current has three components: a DC component given by the average input current, a low frequency component due to the realized output current waveform and a high frequency component due to the modulation. In case of a balanced load the low frequency component is zero. With reference to Fig. 6.7, the inverter leg state is represented using a binary codification as shown in 6.1.

$$S_x = \begin{cases} 1 \rightarrow SWxH \ \ is \ \ ON, \ \ SWxL \ \ is \ \ OFF \\ \\ 0 \rightarrow SWxH \ \ is \ \ OFF, \ \ SWxL \ \ is \ \ ON \end{cases} \qquad x = a, b, c \tag{6.1}$$

The instantaneous input current is the sum of the individual leg currents (6.2).

$$i_{DC-link} = S_a \cdot i_a + S_a \cdot i_b + S_a \cdot i_c \tag{6.2}$$

$I_{DC-link,avg}$ is defined in (6.3), where T_e is the fundamental period of the output current.

$$I_{DC-link,avg} = \frac{1}{T_e} \int_0^{T_e} i_{DC-link} \, dt \tag{6.3}$$

$I_{DC-link,RMS}$ is defined in (6.4).

$$I_{DC-link,RMS} = \sqrt{\frac{1}{T_e} \int_0^{T_e} (i_{DC-link} - I_{DC-link,avg})^2 \, dt} \tag{6.4}$$

The computation process can be automatized. Fig. 6.21 shows the results obtained when $V_{phase,ref} = 1 \ pu$ and $cos(\theta) = 1$. Fig. 6.22 is the magnification of Fig. 6.21. The upper plot shows the reference duty cycle for the three phases and the triangular carrier. The lower plot show the average and instantaneous input currents. The RMS current in the capacitors has been computed for different output reference voltages and for different power factor angles, the results are shown in Fig. 6.23. The RMS current is plotted as function of the output reference voltage. The worst case condition occurs when $V_{phase,ref} \approx 0.6 \ pu$ and $cos(\theta) = 1$. In the worst case condition the RMS current in the capacitors can be 83 A.

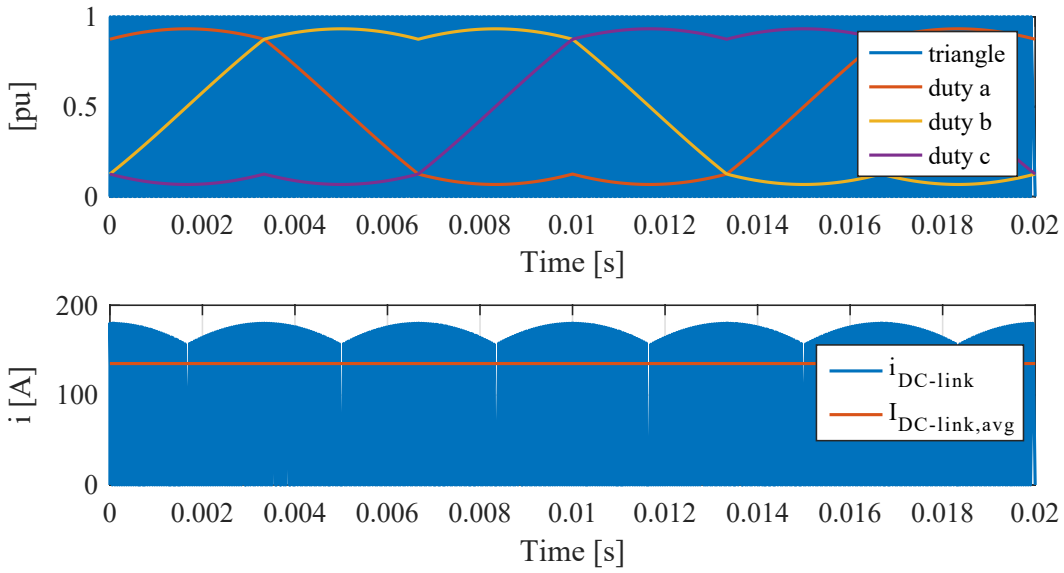


Fig. 6.21: I_{rms} DC-link capacitors. ($i_{phase,pk}$=180 A, cos(θ)=1, $V_{phase,ref,pu}$=1).

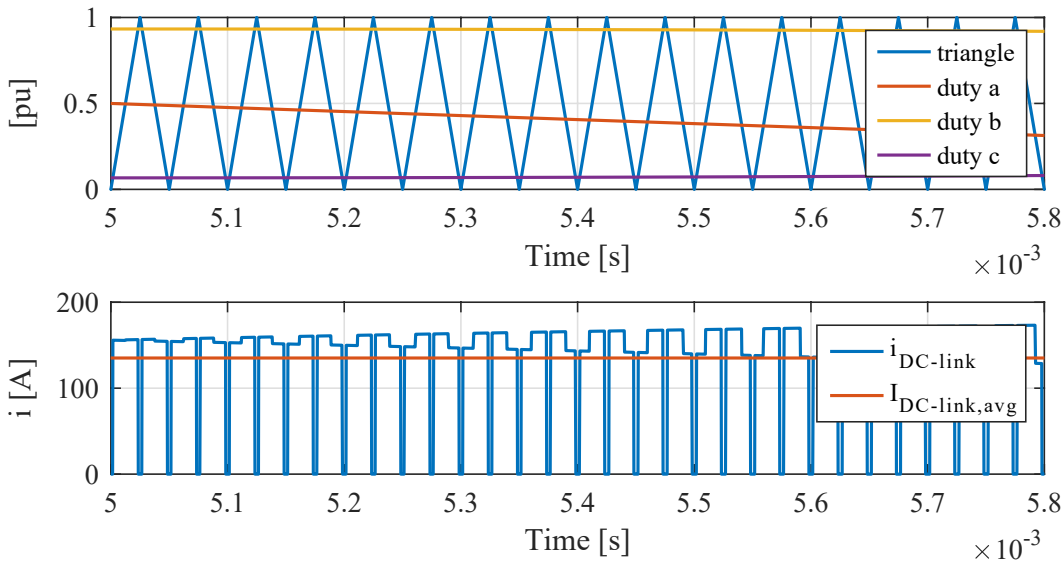


Fig. 6.22: Detail of Fig. 6.21.

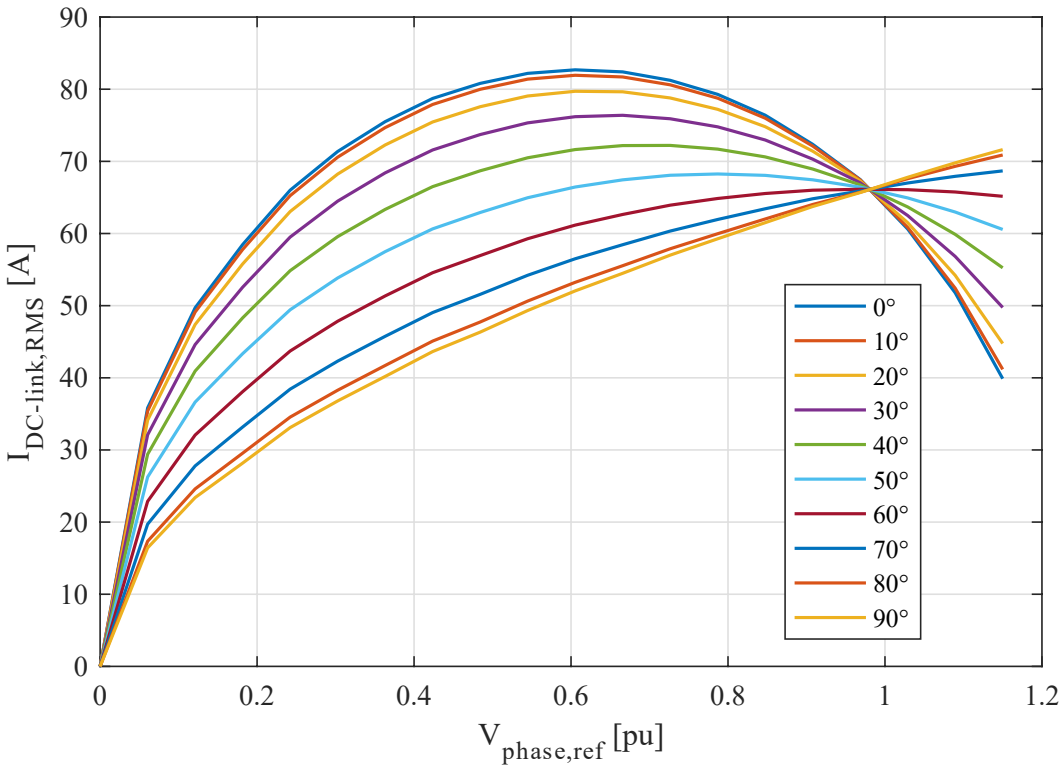


Fig. 6.23: I_{RMS} in the DC-link capacitors at different value of $\cos(\theta)$ and $V_{phase,ref}$.

The second constrain concerns the maximum voltage ripple. Supposing a switching frequency of 20 kHz in the worst case condition the ripple can be analytically computed [77].

$$\Delta v_{pk-pk} \approx \frac{I_0}{4 \cdot f_{sw} \cdot C} = \frac{180}{4 \cdot 20000 \cdot 120 \cdot 10(^{-}6)} = 18.75\ V \tag{6.5}$$

The last constrain concerns the resonance frequency. The resonance frequency of the film capacitors is 300 kHz, it is more than 10 times the switching frequency (20 kHz).

Some considerations can be made about the results. First of all the SAE regulation limits the power absorbed from the battery to 80 kW. However, during accelerations most of the torque is delivered by rear wheels, while during braking most of the torque is delivered from the front wheels. Therefore, the peak power of each inverter unit is >20 kW. Furthermore, the flux weakening of the electric motor requires to provide high amount of reactive power. The current needed during the flux weakening of the motor can become high especially when the battery it is near to the complete discharge and the voltage of the DC-link can go down to 350 V. According to Tab. 6.3 the maximum RMS current of the motor is 105 A, equivalent to 148.5 A peak sinusoidal current.

This inverter has been design taking into consideration the future developments of the car. The next step will be to replace the AMK motor with a custom design motor. In turn, the capacitors have been designed to match the maximum power modules current (180 A). The maximum current of the power modules strongly depends on the working conditions, this aspect will be investigated experimentally.

6.2.6 Auxiliary Power Supplies

Special care has to be paid to the auxiliary power supplies. Different voltage levels need to be provided and some of them require galvanic insulation. The vehicle carries a 24 V battery for on-board auxiliary systems. The additional battery permits to avoid to use the DC-link battery to supply the auxiliary systems: this permits to increase the system efficiency and the immunity to the EMI interferences. Fig. 6.24 shows the functional diagram of the auxiliary power supplies: it is possible to notice in green the 24 V from the battery. Three buck regulators produced 3.3 V and 5 V outputs used for supplying the digital parts of the control board (eg. MCU, FPGA ...). The analog devices of the control board (eg. operational amplifiers) are supplied using another 3.3 V, obtained from the 5 V through a linear regulator. This permits to obtain a regulation with minimum noise and to keep the power supply of the digital part separate from the power supply of the analog part.

The 15 V obtained from the buck converter is used to supply the HF generator. The HF generator consists of a resonant H-bridge converter with zero voltage commutations. The output of the HF generator is a 15 V AC voltage at 200 kHz, used to provide insulated supply via high frequency transformers.

For example, the encoder is supplied using the high frequency transformer , the voltage is first rectified and then adjusted using a linear regulator. Theoretically the encoder could be supplied using just the 5 V coming from the buck regulator without any galvanic insulation. However, this is a bad practice because the encoder is installed on the motor that is supplied in PWM, thus causing common mode noise. The encoder cable thought the parasitic capacities works as a preferential path for the common mode current. The common mode noise coming from the encoder can compromise the whole control board. For this reason it is a good practise to keep the encoder insulated when working with wide bandgap devices. The same applies to the CAN communication and to the DC-link voltage sensor.

The LEM current transducers are supplied using a separate DC/DC converter that outputs +15 V and -15 V.

The drivers boards are also supplied by the high frequency bus. In this case a common mode filter has been added before the transformer. This improves the common-mode rejection rate especially for the drivers that are the most affected parts. +18 V and -2 V lines are needed for driving the gates of the power MOSFETs. The +18 V is obtained with a boost converter because the adopted high frequency transformer can provide just 7.5 V. Obviously on the market there are

transformers with a different turn ratio but this solution permits to obtain all the four needed voltages with just one transformer. The 3.3 V is used for supplying the V_{ON} measurement system is provided via a linear regulator. The ≈ 7.5 V line is direct from the rectified voltage of the hight frequency transformer. This non particularly stable voltage is used to supply a current generator that does not need a precise voltage input. More details can be found in Section 6.2.7.

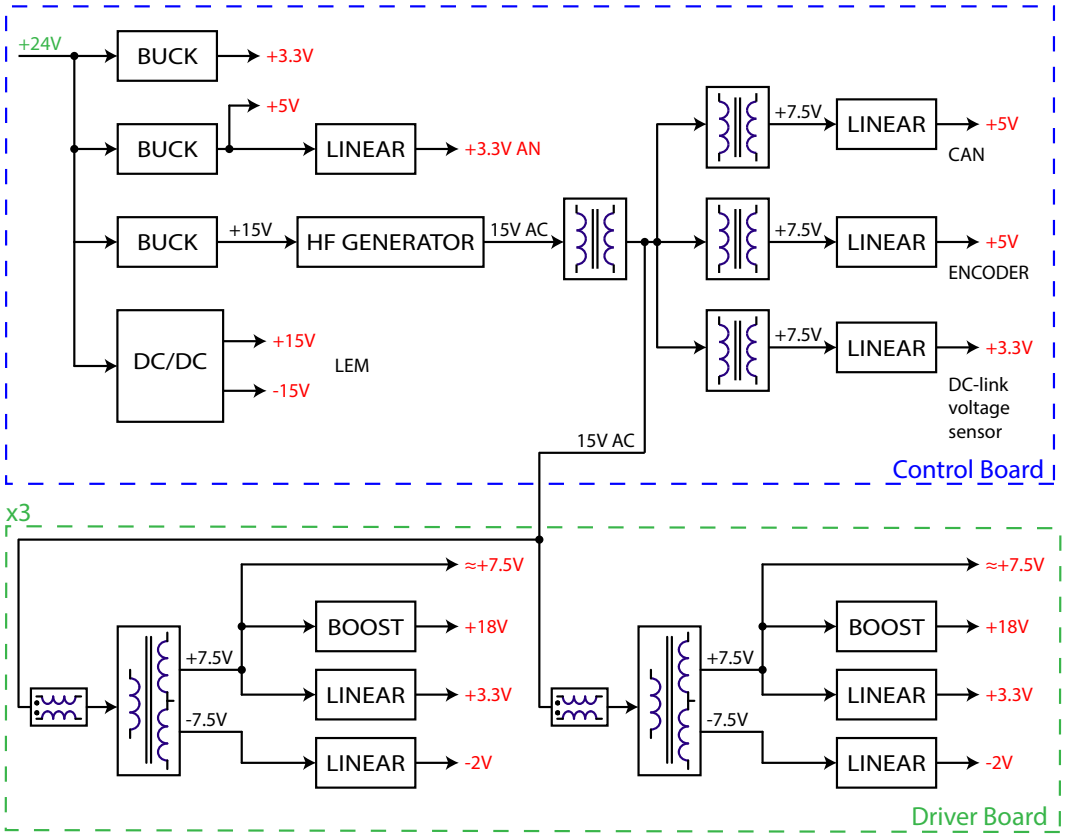


Fig. 6.24: Auxiliary power supplies functional diagram.

6.2.7 V_{ON} Measurement System

Special care has to be paid to the system for measuring the voltage drop of the MOSFET during his conduction state. Compared to the POC test rig the new solution offers increased bandwidth and precision. The schematic of the proposed solution is depicted in Fig. 6.25.

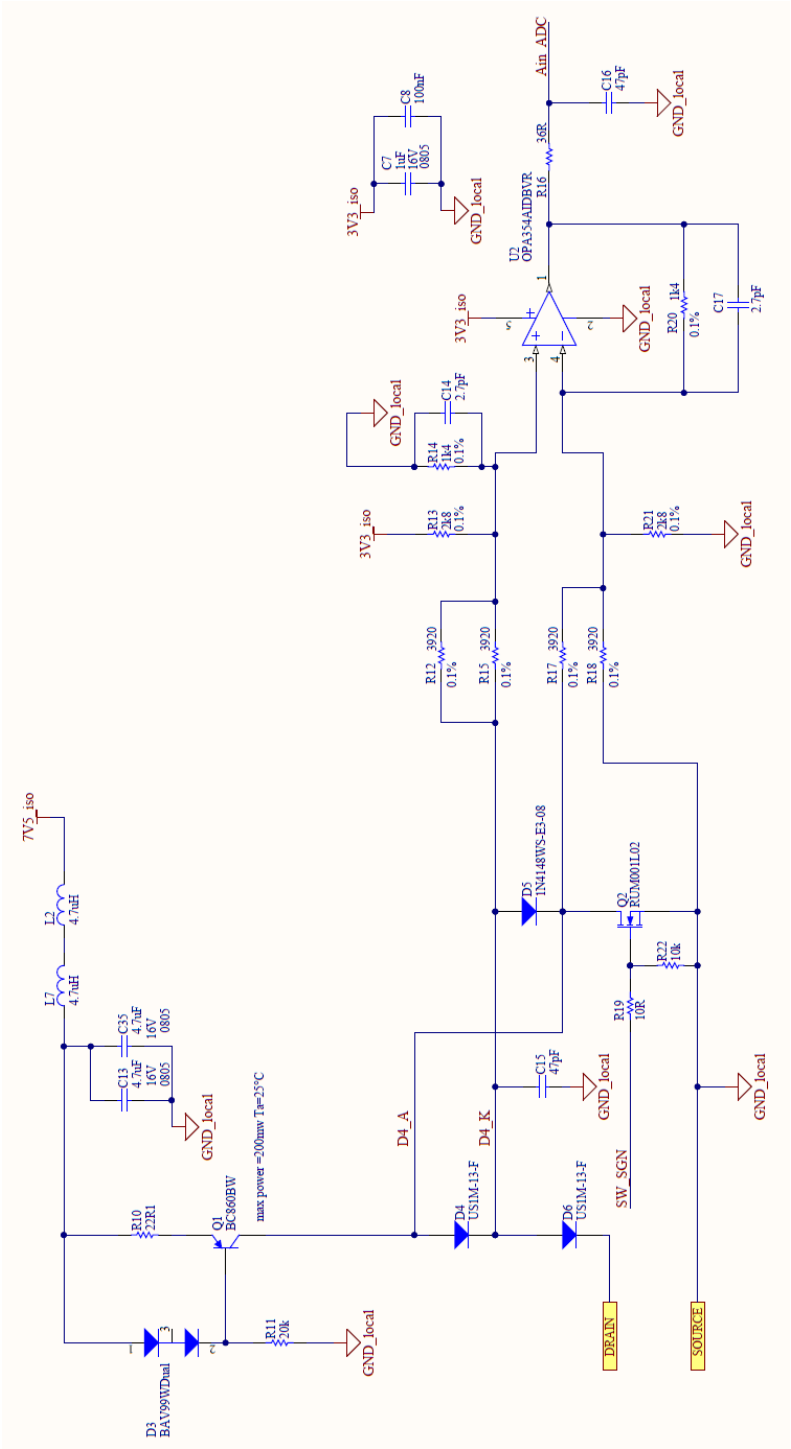


Fig. 6.25: Schematic V_{ON} measurement system.

Since the Drain-Source voltage of the MOSFET can rise up to the DC-link voltage after the turn-OFF, it is necessary to protect the measurement system by

adding a diode (diode D6 in Fig. 6.25). The diode is forward biased with a current generator when the MOSFET is in conduction state and the voltage between drain and source drops to a few volts. The conditioning system measures the voltage between the drain and the source plus the voltage drop on D6. For this reason a second diode(diode D4 in Fig. 6.25) in series to the first diode has been added. The two diodes are polarized in first approximation with the same current so that the two voltage drops compensate each other. To avoid the saturation of the measurement circuit, the MOSFET labelled as Q2 in Fig. 6.25 has been added. Q2 can be closed when v_{DS} go up to the DC-link voltage, so to avoid the saturation of the operational amplifier. The analog signal conditioning system consists of an operational amplifier in differential configuration. The gain of the system can be analytically computed. The proposed measurement system during normal operating conditions works in linearity, where the superposition principle applies. The system can be considered as the combination of three differential operational amplifiers with three different gains. The first system is measuring the forward voltage of the diode $D4$. The gain is computed in ((6.6)).

$$G_{D4} = \frac{V_{Ain\ ADC}}{V_{D4\ A} - V_{D4\ K}} = -\frac{R_{20}}{R_{17}} = -\frac{1400}{3920} = -0.3571 \tag{6.6}$$

The second system is measuring the voltage between drain and source plus the voltage drop on diode $D6$. The gain is computed in ((6.7)).

$$G_{DS+D6} = \frac{V_{Ain\ ADC}}{V_{D4\ K} - V_{SOURCE}} = \frac{R20}{R18} = \frac{1400}{3920} = 0.3571 \tag{6.7}$$

The third system is used to introduce a voltage offset on the output of the operational amplifier.

$$G_{offset} = \frac{V_{Ain\ ADC}}{3.3V} = \frac{R_{20}}{R_{13}} = \frac{1400}{2800} = 0.5 \tag{6.8}$$

The output voltage of the measurement system:

$$V_{Ain\ ADC} = (V_{D4\ K} - V_{SOURCE}) \cdot G_{DS+D6} + (V_{D4\ A} - V_{D4\ K}) \cdot G_{D4} + 3.3 \cdot G_{offset} \tag{6.9}$$

The bandwidth of the proposed system has to be sufficient to measure the voltage between the Drain and the Source of the component also when the conduction time is short. The operational amplifier is the OPA354 by the Texas Instruments, with a unity-gain bandwidth of $250MHz$. The resulting bandwidth of the measurement system is further reduced by the insertion of two feedback capacitors and by the insertion of an "RC" output filter. The two feedback capacitors work as a first order filter with a cut-off frequency of:

$$f_{cut-off,fbk} = \frac{1}{2\pi R_{20} C_{17}} = \frac{1}{2\pi R_{14} C_{14}} = \frac{1}{2\pi \cdot 1400 \cdot 2.7e-12} = 42.1\ MHz \quad (6.10)$$

The output RC filter has a cut-off frequency of:

$$f_{cut-off,out} = \frac{1}{2\pi R_{16} C_{16}} = \frac{1}{2\pi \cdot 36 \cdot 47e-12} = 94.1\ MHz \quad (6.11)$$

The the resistors used with the operational amplifier have a 0.1 % tolerance.

The proposed design has been validated with a SPICE simulator. Fig. 6.26 shows the SPICE simulated response of the circuit of Fig. 6.25 to a voltage square wave (shown in blue) applied between the Drain and the Source pins.

The input square wave is ranging between +3.5 V and -3.5 V with a frequency of 200 kHz. The output voltage, in red, represents the input of the ADC converter.

The V_{ON} voltage is tracked with high dynamics. Fig. 6.27 shows one detail of Fig. 6.26: it is possible to notice that the settling time is around 0.05 µs. The results obtained from the small signal AC analysis are shown in Fig. 6.28 . The plot on the top shows the gain of the system when frequency changes. For low frequencies the gain is equal to the one analytically computed in (6.7). In Fig. 6.29 v_{DS} is step-varied from 600 V to -3.5 V. V_{ADC} varies from a saturation state to a linear state. The settling time computed in simulation is around 0.07 µs. However, the real settling time is larger, because of the noise due to the commutation effects and to the effects of the parasitics of the circuit.

Fig. 6.30 shows the variation of the voltage drop on diode D4 and D6 when v_{DS} varies from 3.5 V to -3.5 V. The voltage drop variation is due to the variation of the current in the diodes. The transistor Q1 works as a current generator, however it is not ideal. When v_{DS} varies the current generator is not able to keep the current perfectly constant. Furthermore, the two diodes despite being in series are not conducting the same current, because of the differential measurement system that is absorbing part of the current. In turn, the voltage drop on the two diodes is not equal. This difference introduce a small nonlinearity in the measurement system, however this will not affect the measurement temperature estimation. As explained in the previous chapter, the same measurement system is used to generate the look-up table and to measure the voltage drop during the normal operations of the converter.

The threshold of a diode depends on its junction temperature. The nominal current of D4 and D6 is 1 A, in turn a few mA current will not cause any significant temperature increase. However, the ambient temperature can varies and this can affect the voltage threshold of the two diodes. The two diodes are placed in close proximity as shown in Fig. 6.31 so that they can be considered always at the same temperature. In turn, any variation in the forward voltage will cancel each other.

A source of error is the temperature variation of the transistor Q1, that affects the current injected in the diodes. On the market there are IC devices that can work

as a constant current generator. An IC solution permits a more accurate adjustment of the current with a lower sensitivity to temperature variations. However, due to the higher number of components they have a lower current bandwidth. In this application, having a current generator with a high bandwidth is indispensable, in turn a pnp transistor with a transition frequency of 100 MHz has been used.

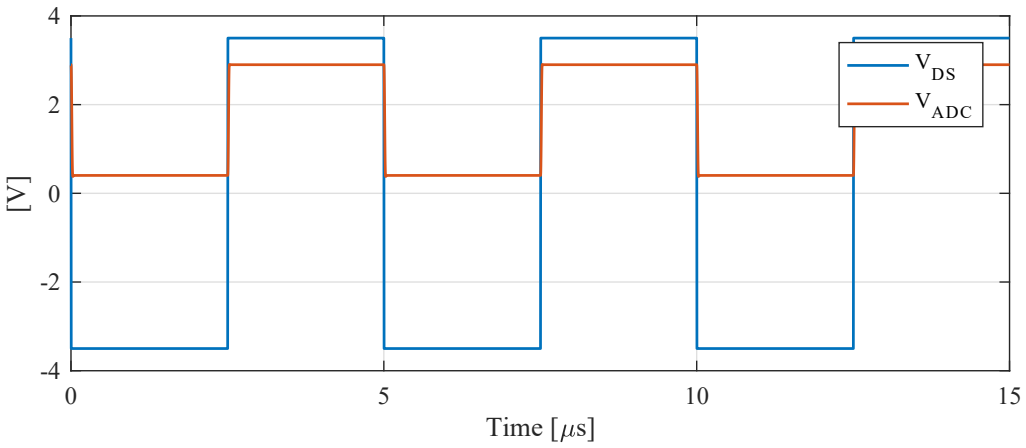


Fig. 6.26: Spice simulation of the V_{ON} measurement system response at 100 kHz switching frequency.

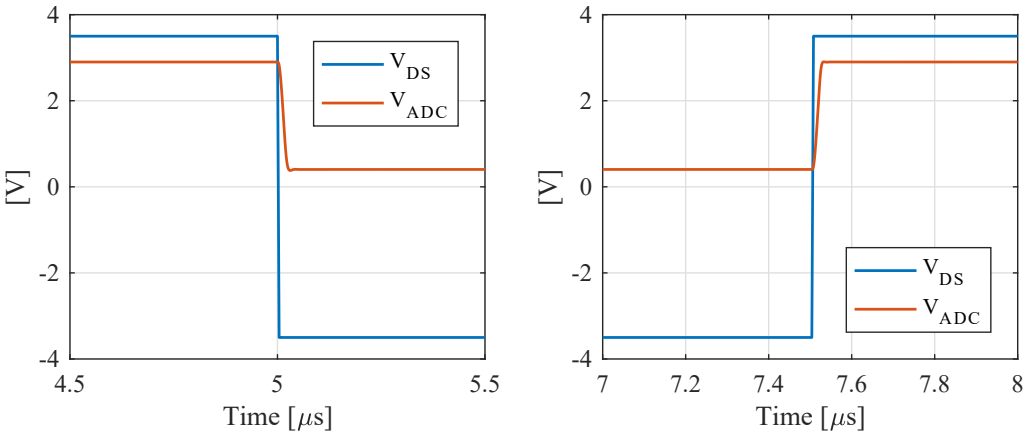


Fig. 6.27: Detail of Fig. 6.26. (Left) down-front. (Right) up-front.

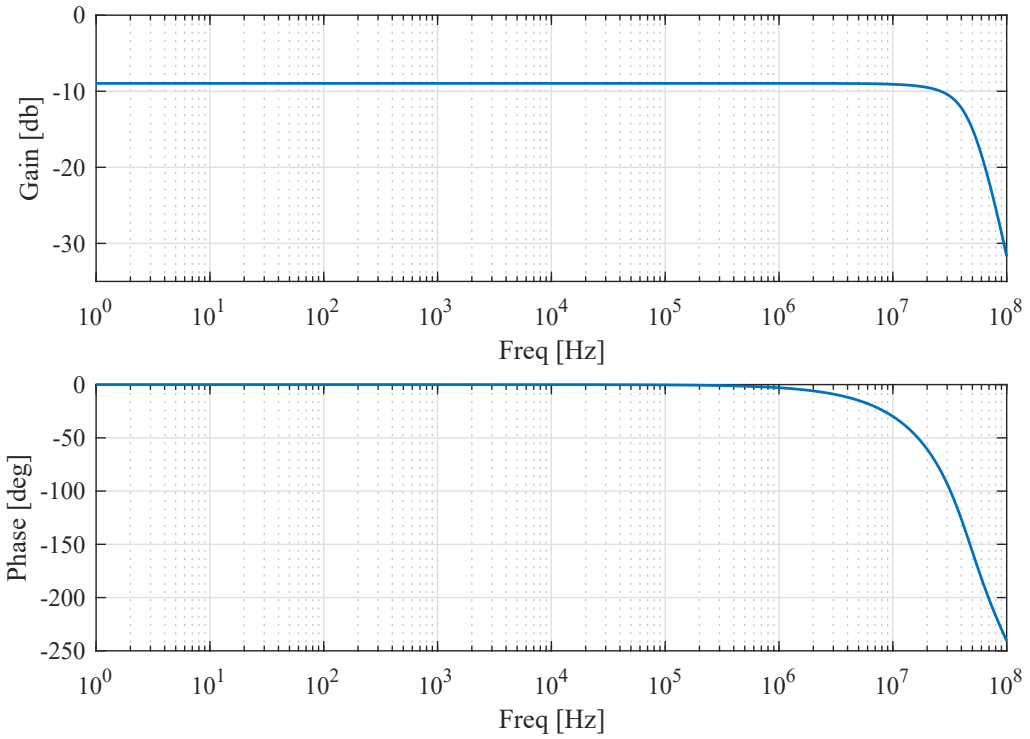


Fig. 6.28: Bode diagram of the $V_{Ain\ ADC}/V_{DS}$ response.

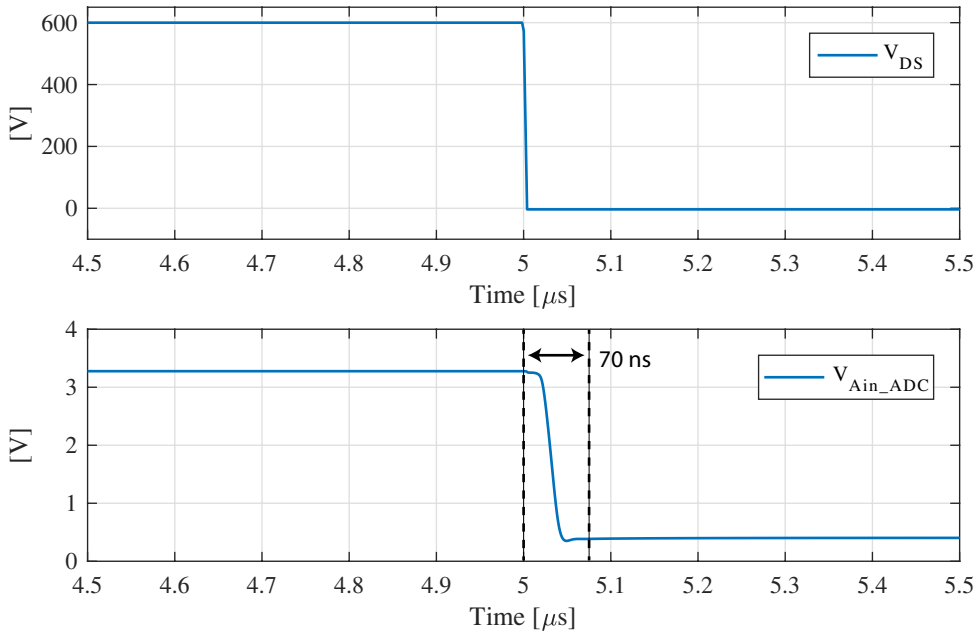


Fig. 6.29: v_{DS} step changed from 600 V to -3.5 V.

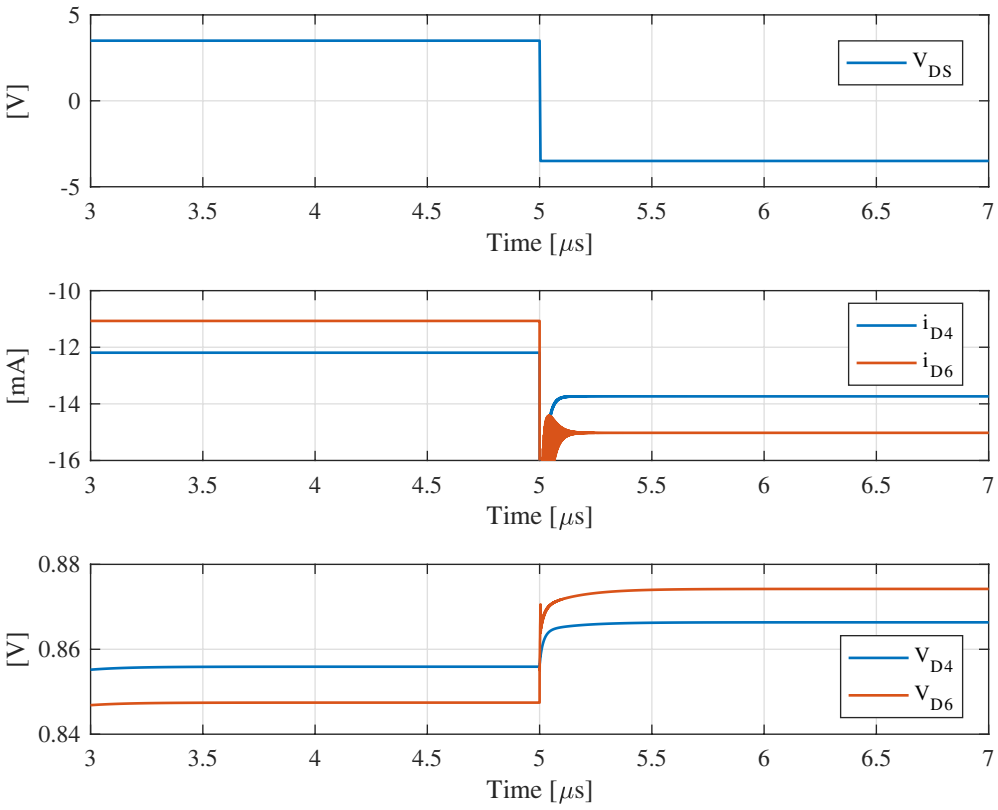


Fig. 6.30: Currents in D4 and D6 before and after a step variation of v_{DS}.

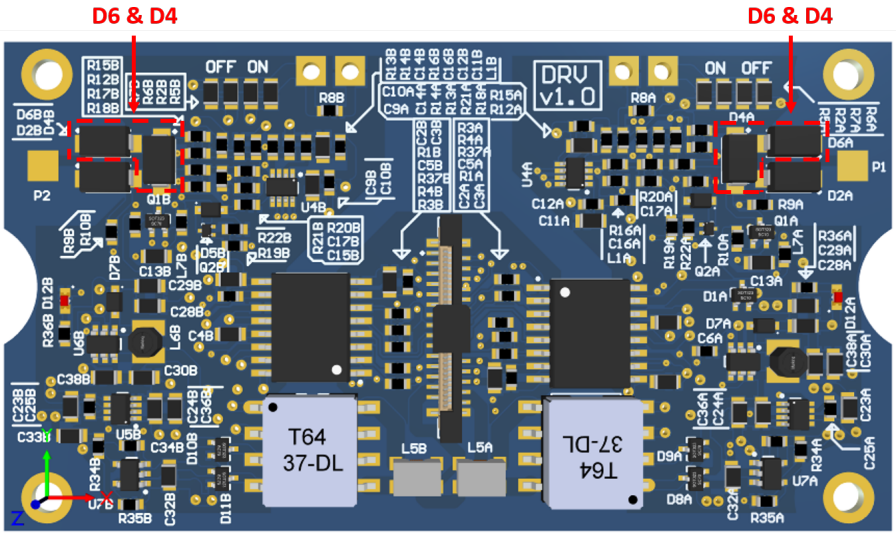


Fig. 6.31: Diodes D4 and D6 in close proximity.

6.3 Firmware Description

As mentioned in Section 6.2.4 the inverter is based on a hybrid with architecture MCU and FPGA. The two chips communicate via four full duplex SPI lines and two digital IO. It is not the purpose of this thesis to focus on the code implementation: this section provides an overview of the code structure.

6.3.1 FPGA Code

The FPGA code has been implemented in VHDL and can be divided in the functional blocks described above.

- System time manager.
- PWM modulator.
- Sampling manager.
- Fault manager.
- SPI Communication.
- Interrupt Generator.
- µC overrun.
- DAC.
- Data buffer
- Encoder EnDat

The **system time manager** generates the interrupts for all the units and contains all the PLL (phase-locked loop) needed to generate the system clocks. During the PLL start-up the system time manager resets all the FPGA units. The interrupts generated by this block are phase locked with the PWM triangular carrier. E.g. two interrupts (one on the positive triangle vertex and one on the negative triangle vertex) are sent to the sampling manager for measuring the V_{ON}.

The **PWM modulator** is one of the most important parts of the inverter. The three reference duty cycles received from the MCU are turned into gate driver commands for each MOSFETs. To avoid the DC-link short circuit, dead time are introduced between the commands of top and bottom switches of each inverter leg. The output duty cycle can be updated one or two times per period depending on the user settings.

The **sampling manager** handles the ADC measurements. Each external ADC communicates with the FPGA through an half duplex SPI interface that is operated

by the sampling manager. The sampling manager can also do some manipulation on the acquired data, like the offset removal or samples average if oversampling is used.

The **fault manager** handles all the protections. If a fault condition is detected the protection manager will generate an hard fault or a warning. In case of an hard fault all the switches are commanded to open immediately, the modulation stops and the FPGA goes into error state. In case of warning the FPGA continues to work and the warning is communicated to the microcontroller.

The **SPI communication** block manages the four full duplex SPI communication between the microcontroller and the FPGA. The FPGA works as slave while the microcontroller works as master. Data can flow in both directions.

The **interrupt generator** generates the PWM-synchronized microcontroller interrupt using one of the two GPIOs lines. The interrupt is generated shortly after the vertex of the PWM triangle when all the ADC acquisitions are complete. After the interrupt the microcontroller starts to communicate with the FPGA using the SPI line. Depending on the modulation strategy one or two interrupts per PWM period can be generated.

The **µC overrun** block is used to control the correct synchronization between the microcontroller and the FPGA. If the microcontroller stops or the motor control algorithm can't be executed in time this block generates an error that is transmitted to the protection manager, which generates a hard fault.

The **DAC** block is used to command the two external four-channel DACs. The external DACs are used mainly for debug purposes.

The **Data buffer** is a buffer used to store the data from the sampling manager before they are sent to the microcontroller.

The **Encoder EnDat** block manges the Endat communication with the encoder. More details about this encoder communiation protocol can be found in [78].

6.3.2 Microcontroller Code

The Microcontroller firmware structure is summarized in Fig. 6.32. At each PWM period the FPGA triggers the microcontroller through the GPIO line. When the microcontroller receives the FPGA trigger, the main interrupt routine is executed. For purpose of simplicity the main interrupt routine has been schematized as follows:

1. The microcontrolloer acts as a master and reads the FPGA data through the four SPI lines. The external ADCs measurements, the absolute encoder position and some informations about the FPGA state are acquired by the microcontroller. During this phase also the data coming from the peripherals

of the microcontroller are acquired (e.g. the ADCs measurements and the position of the incremental encoder).

2. Data is received through the debug interface. A detailed explanation is given in Section 6.3.3.

3. Different types of faults can be generated by the microcontroller or by the FPGA. A hard fault or a warning can be generated depending on the type and on the duration of the error. If a hard fault is generated all the MOSFET are commanded open and the inverter goes in error state. It has to be said that most of the protections (e.g. the overcurrent protection) are implemented directly in the FPGA that can decide to open the MOSFETs immediatly, and then to communicate the error state to the microcontroller. Other kind of protection are "hardware" like the desaturation protections embedded in the gate driver, in this case the error state is just communicate to the microcontroller.

4. The junction temperature of all the six MOSFETs is estimated. If the control on the maximum junction temperature is active, the reference current is limited accordingly.

5. The main controller communicate via CAN the reference torque to the main control unit of the car. If the maximum current level is being limited because the junction temperature limit has been reached, then also the maximum achievable torque is limited accordingly (the maximum achievable torque is sent to the main controller via CAN). The motor control code is executed and the reference duty cycle are computed.

6. Data is sent to the debug interface. A detailed explanation is given in Section 6.3.3.

7. Data are sent through the SPI back to the FPGA.

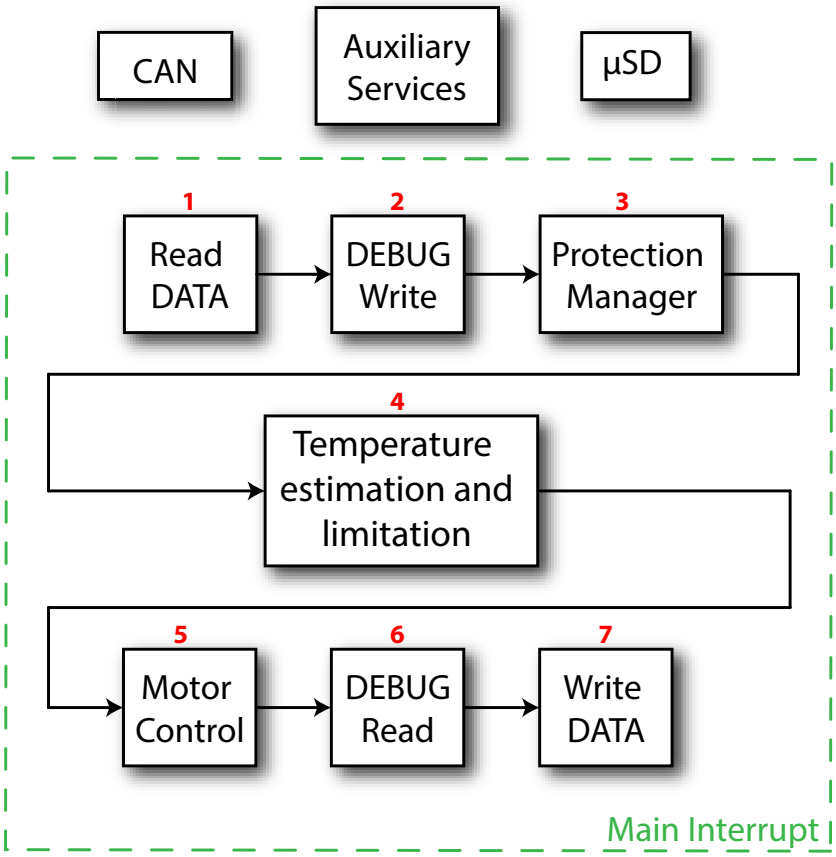


Fig. 6.32: Flowchart description of the control task executed by the MCU. The control task executed at each interrupt is enclosed in a green dashed line.

6.3.3 Debug and Acquisition Tool

Although the subject of the thesis is the temperature estimation, a considerable amount of time has been dedicated to develop the debug and acquisition interface. Ideally, the user would like to visualize the variables inside the microcontroller at each PWM period. The standard solution is to use the DAC converter inside the microcontroller and to visualize the value of the internal variables on an oscilloscope. The limitations of this solution are the oscilloscope channels, that have a vertical resolution of 8 bit. Moreover, the STM32H743ZI has just one DAC on board. Alternatively, it is possible to use the GPIO port of the microcontroller to generate signal that can be read by an oscilloscope but this ports can provide just a "binary" information.

The microcontroller manufacturer provides a programming and debugging interface called **ST-LINK/V2**, that can communicate directly with the ARM core inside the microcontroller using a dedicated SWD (Serial Wire Debug) protocol. The

ST-LINK/V2 debugger permits to read and modify the control variables while the process is running without affecting the execution of the code. The ST-LINK/V2 interface can be easily managed with commercial IDEs (Integrated Development Environments) like Keil µvision. However, there are some limitations regarding the maximum bitrate. Moreover, ST-LINK/V2 interface does not allow to write and read variables at a precise time interval. For these reasons additional debugging interfaces are required.

A functional diagram of the debug interfaces is shown in Fig. 6.33.

A more sophisticate solution was developed purposely for this converter, to export MCU data frames into Matlab, in floating point format and without downsampling. It uses a USART interface, a half duplex SPI interface and a Trigger signal (GPIO port). The USART interface provides a low speed (around 1 Mbit/s, depending on the load state of the PC) bidirectional communication between the micrcontroller and the PC. The SPI provides a high speed (up to 40 Mbit/s) unidirectional communication from the microcontroller to the PC.

Two functions have been added to the main interrupt routine, one at the beginning and one at the end of execution. In turn:

1. At the start of the main interrupt routine, the function **DEBUG_write( )** communicates via USART with the PC. A galvanic isolated USART to USB adapter has been interposed between the microcontroller and the PC. The adapter emulates a virtual COM port on the PC, that can be controlled with MATLAB.

   The DEBUG_write( ) function permits to :

   - Set control variables and parameters at the beginning of the interrupt.
   - Set the dimension of data buffer used to store the data during the commissioning test of the inverter.
   - Set which control variables are visualized.
   - Receive informations about the microcontroller state.

2. The second function **DEBUG_read( )** is called at the end of the main interrupt. This function is used to stream the data from MCU to PC through the SPI interface. The SPI interface is in half duplex configuration where the MCU act as a master and it connected to an external logic analyzer. In addition to the SPI interface there is a GPIO line used to generate a trigger signal, at every PWM interrupt. The logic analyzer is connected to the PC through an optocoupled USB communication. The logic analyzer can be interfaced directly with Matlab thanks to the API provided by the manufacturer. The bitrate of the SPI communication is 25 Mbit /s, limited by the adopted logic analyzer. Considering a switching frequency of 20 kHz

and 32 bit output variables, at each interrupt thirty-five variables can be sent to the PC (theoretically the maximum number of variables is thirty-nine, but an idle time between one variable and another has to be added). It is also possible to work in downsampled mode and increase the number of variables to stream.

The possibility to manage the debug and acquisition system directly with Matlab permits a high level of flexibility. It is possible to quickly develop a GUI interface like the one shown in Fig. 6.34. More important thanks to the Matlab environment it is possible to easily manipulate and visualize the acquired control variables.

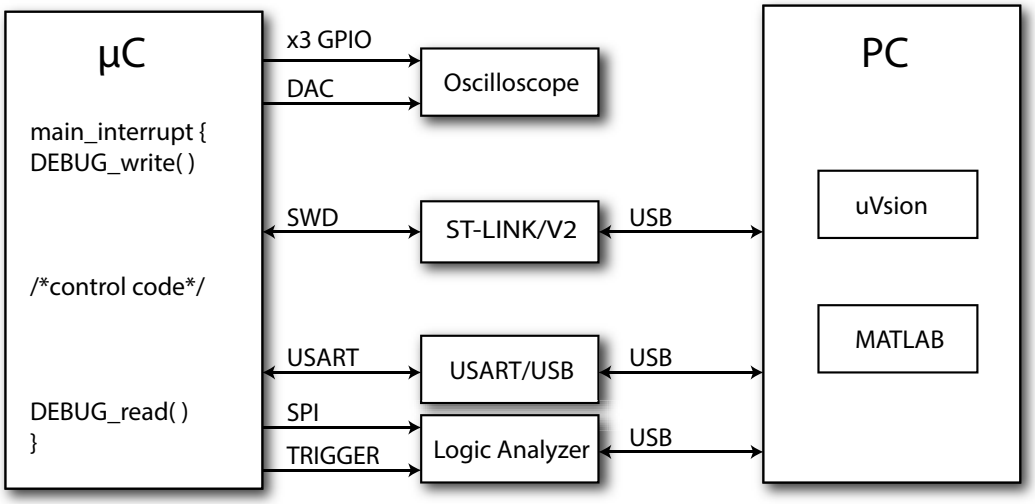


Fig. 6.33: DEBUG interface functional diagram.

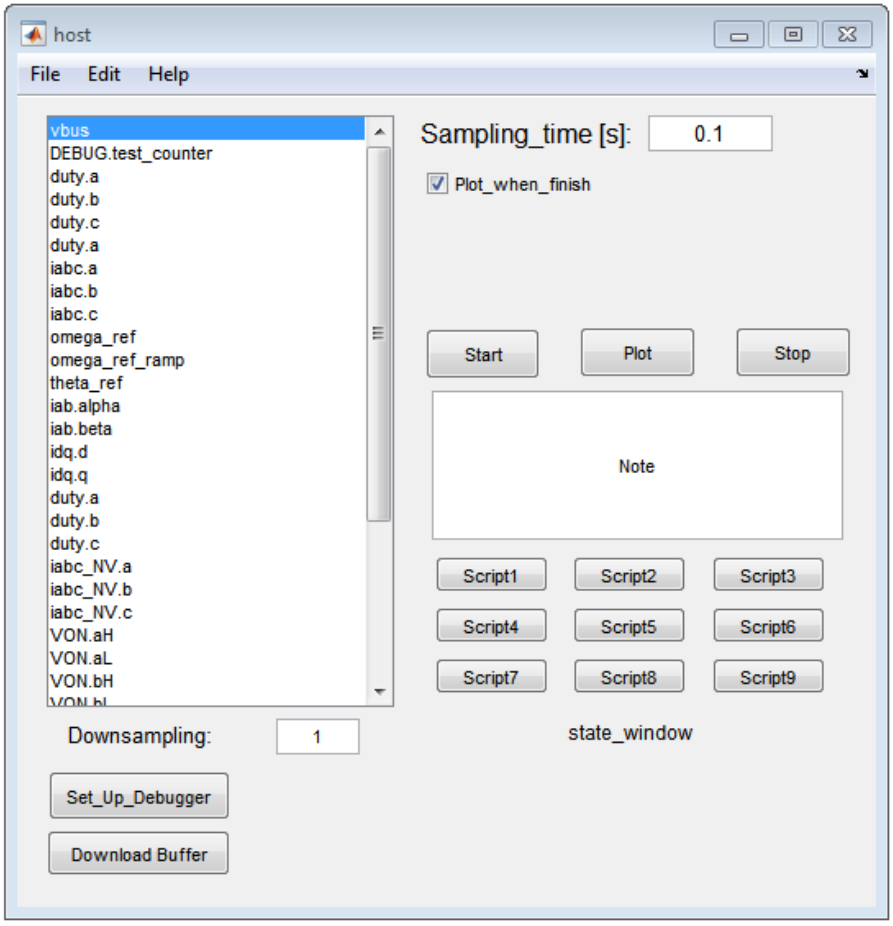


Fig. 6.34: DEBUG GUI MATLAB.

Chapter 7

Results for the 3-phase Inverter Prototype

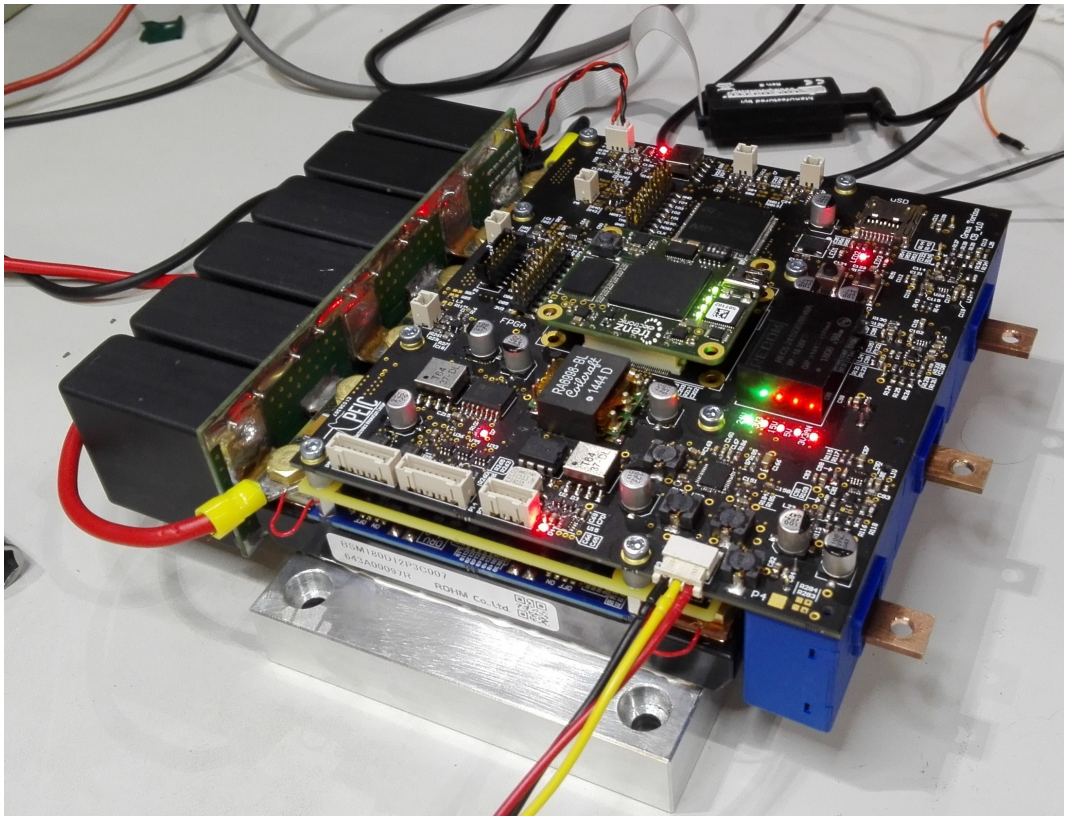


Fig. 7.1: Power converter overview. The provisional heatsink is a block of aluminium.

7.1 Commissiongin Test

The R_{ON} maps of all six power switches of the inverter are identified, to be later used for real-time estimation of the respective junction temperatures. To do so, a three-phase inductor is connected to the converter's output (Fig. 6.7). Respect to the first proof of concept (Chapter 4), the three-phase nature of the system and the fact that both devices of each leg are identified must be taken into account.

7.1.1 Commissioning Test Description

The commissioning test procedure is similar to the one presented in Section 4.1.1. The water-cooled heatsink is here preliminary replaced by a temporary aluminium plate. The power converter with the aluminium plate is visible in Fig. 7.1. Two PTC thermistors measure the temperature of the aluminium plate. The commissioning steps are:

1. The aluminium plate is heated using a temperature controlled hot plate. When the temperature measured by the two thermistors reaches 150 °C, the heater is turned-OFF. The aluminium plate starts cooling naturally.

2. At this temperature, short current pulses from 1 A to 180 A are commanded for each of the six inverter axes as showed in Fig. 7.3. This permits to map all the six switches both for positive and negative currents.

3. When the temperature measured with the the two PTC thermistors drops by 5 °C a new set of current pulses is commanded to the load.

4. The test stops when the aluminium plate reaches the room temperature.

7.1.2 Pulse Sequence on Axis "a" Positive

The state of the inverter leg is "1" when the upper switch is ON and "0" when the lower switch is ON. E.g. "100" indicates that phase "a" is connected to the positive terminal of the DC-link and phases "b" and "c" to the negative terminal. This is called "phase a positive" state, represented in Fig. 7.2. The first pulse sequence is controlled on this axis, modulating between the active state "100" and the two zero voltage states "000" and "111", as represented in Fig. 7.2. The controlled current flows through phase "a" and returns via phases "b" and "c", half per phase. The "phase a positive" test permits to sample the V_{ON} of SWaH at positive current and the V_{ON} of SWbL, SWcL at negative (half) currents as show in Fig. 7.4.

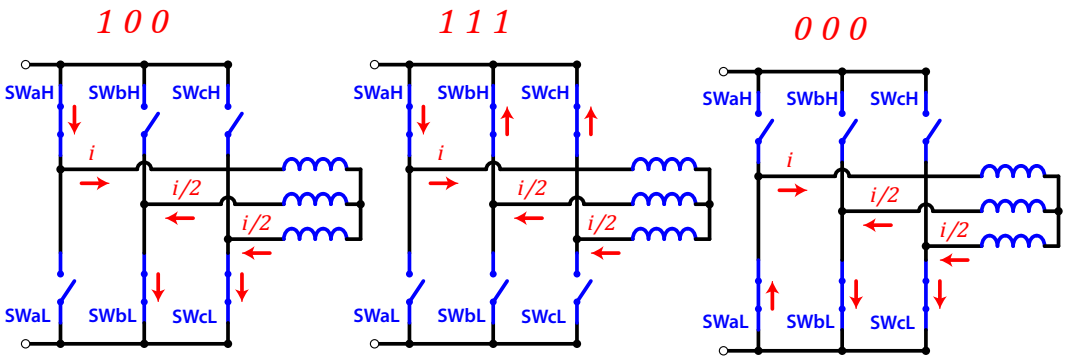


Fig. 7.2: First hexagon: switches state.

7.1.3 Phase Hexagon

The center and the vertices of the limit hexagon represents all the allowable configurations of the inverter switches. The axes of the hexagon labelled as "a", "b" and "c" represent the three output phases of the inverter. Fig. **??** shows the i_a variation during the current step along the "a" axis. At the top of the figure, the inverter switching states are indicated in red, while the sampling times are indicated by two blue arrows labelled as SP1 and SP2. When the current pulse test is conducted along the "a positive" axis, SWaH is mapped for positive currents while SWaL is mapped for negative currents. The currents in the switches and the sampling time (SP1 or SP2) for the first hexagon are reported in Tab. 7.1. A similar approach can be used for the other five axes of the hexagon. This enable to map all the switches for positive and negative currents.

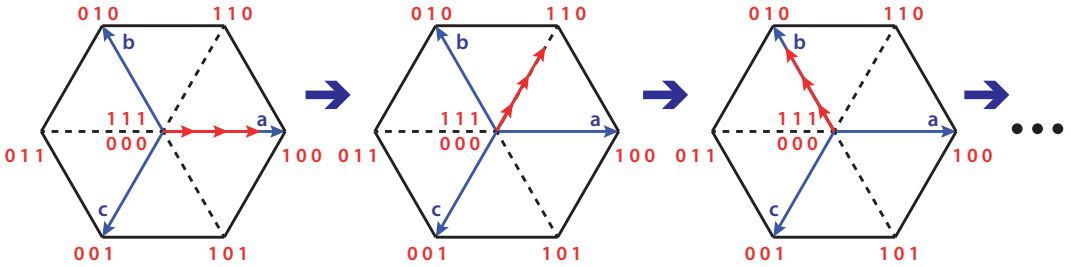


Fig. 7.3: Current pulses of growing amplitude on each of the six axis of the phase hexagon.

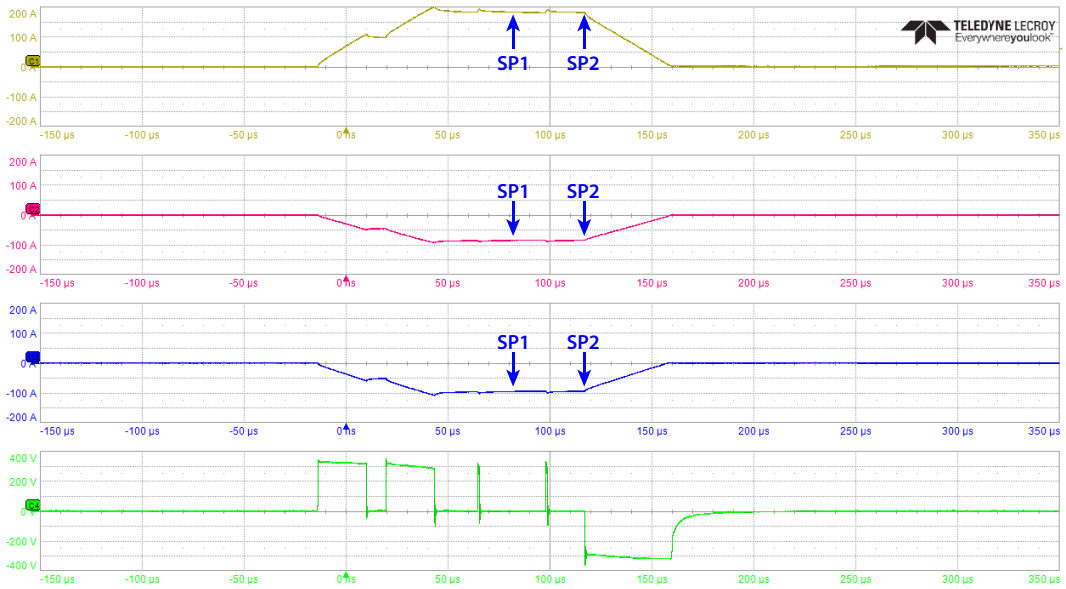


Fig. 7.4: Commissioning test. Starting from the top: i_a (50 A/div), i_b (50 A/div),i_c (50 A/div) and V_{ab} (100 V/div). (t=50µs/div).

Table 7.1: Test "a positive": sampling instances.

SWaH (SP1)	i_a
SWaL (SP2)	$-i_a$
SWbH (SP1)	$-i_a/2$
SWbL (SP2)	$i_a/2$
SWcH (SP1)	$-i_a/2$
SWcL (SP2)	$i_a/2$

7.1.4 Deviation of θ_J Respect to Hot Plate Temperature

As for the POC demonstrator, the key assumption underpinning the validity of the proposed commissioning technique is that the junction temperature and the measured hot plate temperature are the same when V_{ON} and i_{DS} are sampled. The short duration of the current pulses ensures that during the current pulse test the temperature measured using the PTC thermistor equals the junction temperature of the power devices. The aim of this section is to demonstrate that the junction temperature variation caused by the highest current pulse is modest and can be neglected.

Reference is made to the worst case condition, where the controlled current pulse is 180 A on the "phase a positive" and the temperature is 150 °C. The phase

"a" current waveform is reported in Fig. 7.5. The pulse test has been conducted with the same modulation technique used during the normal operation of the inverter. The triangular carrier reported at the bottom of Fig. 7.5 has a frequency of 15 kHz corresponding to a period of 66.7 µs. The duty cycle of phase "a" is reported in red.

According to datasheet curve reported in Fig. 7.7, V_{ON} is 3.2 V when i_{DS} is 180 A, and θ_J is 150 °C. The current pulse test has been divided into seven sectors. The switch SWaH is conducting only in sectors 1,3,5, coloured in red. Some assumptions can be made:

- The commutation losses are in first approximation negligible, because the test is conducted at reduced DC-link voltage of 320 V.
- The duration of sector 2 is negligible. In turn, the current ramps from 0 A to 180 A in 66.7 µs.
- The R_{ON} is supposed to be constant during the test, thus V_{ON} is proportional to i_{DS}.

The conduction losses in the switch SWaH related to sectors 1 + 3 are computed in (7.1).

$$E_{loss,1} \leq \frac{I_{pk}}{\sqrt{3}} \cdot \frac{V_{ON,180A}}{\sqrt{3}} \cdot T = \frac{180}{\sqrt{3}} \cdot \frac{3.2}{\sqrt{3}} \cdot 66.7 \cdot 10^{-6} = 0.0128\,J \tag{7.1}$$

V_{ON} of the switch SWaH is sampled in the middle of sector 5, labelled in blue in Fig. 7.5 as SP1. The conduction losses in the switch SWaH, relative to the first half of sector 5 are computed in (7.1).

$$E_{loss,2} = I_{pk} \cdot V_{ON,180A} \cdot \frac{T}{4} = 180 \cdot 3.2 \cdot \frac{66.7 \cdot 10^{-6}}{4} = 0.0096\,J \tag{7.2}$$

The total conduction losses in the switch SWaH are 0.0224 J and the total conduction time is 83.4 µs. The transient thermal impedance provided by the datasheet is reported in Fig. 7.6. In absence of data the transient thermal impedance for a pulse duration of less than 1 ms is extrapolated. The transient thermal impedance for a pulse duration of 83.4 µs is circa 0.00425 °C/W. The corresponding junction temperature increase of the switch SWaH is computed in (7.3).

$$\Delta\theta_{j,SWaH} = \frac{E_{loss,1} + E_{loss,2}}{T + T/4} \cdot Z_{th,83\mu s} = \frac{0.0128 + 0.0096}{83.38 \cdot 10^{-6}} \cdot 0.00425 = 1.14°C \tag{7.3}$$

The temperature rise is modest, and also considering few mJ due to the commutation losses, the temperature rise is below 2 °C.

The same approach is used for the switch SWaL, which is conducting in sectors 2,4,6 and that it is sampled at the end of sector 6 (labelled as SP2 in Fig. 7.5). In

sector 7 all the switches are commanded open (antiparallel diodes are in conduction) so to bring the current to zero as fast as possible.

Between the current pulses there is an idle time of 200 ms so to cancel any residual temperature perturbation. This ensures that θ_J returns to the heatsink value before the next current pulse occurs.

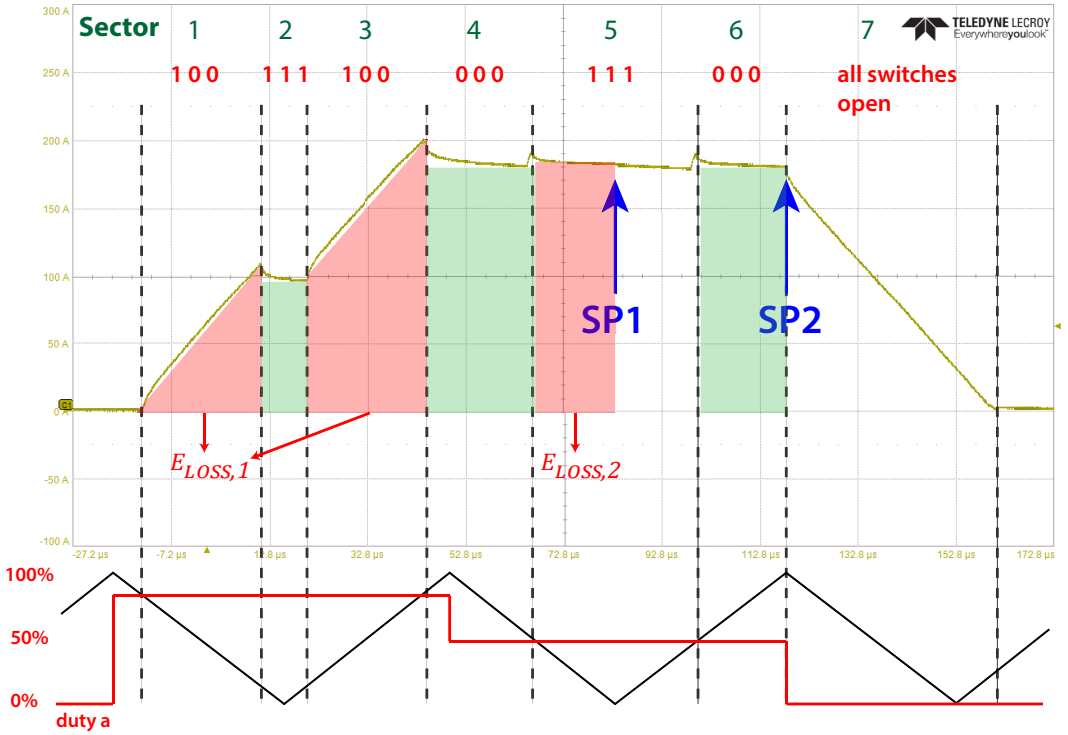


Fig. 7.5: Top: current pulse of phase "a" during the commissioning test (i_a=50 A/div; t=22 µs/div). Bottom: reference duty cycle phase "a" and triangular carrier.

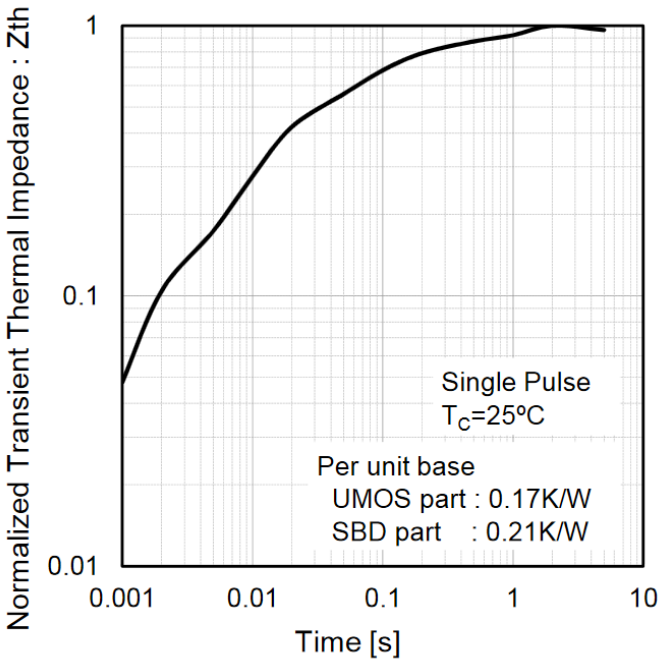


Fig. 7.6: Normalized transient thermal impedance (from the datasheet).

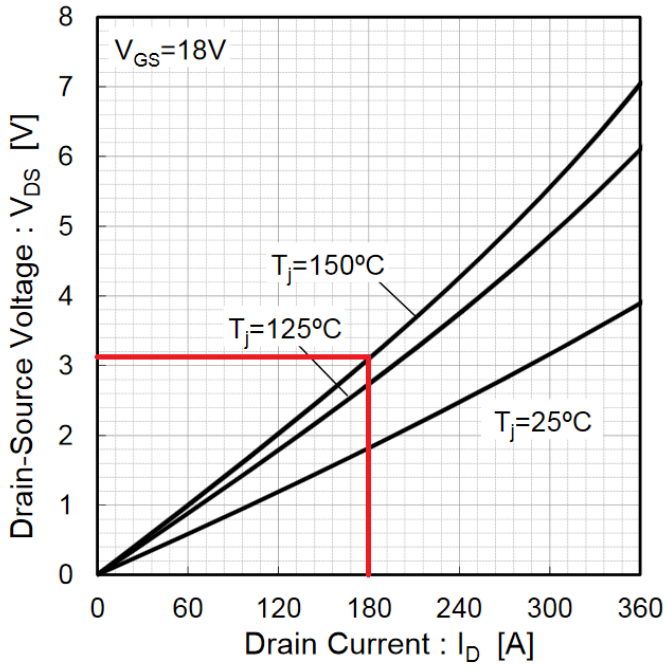


Fig. 7.7: Drain-Source voltage vs Drain Current (from the datasheet).

7.1.5 Effect of Antiparallel Diodes

All six power MOSFETs have been mapped for positive and negative current values. However, due to the presence of the antiparallel diodes the V_{ON} of the devices is not symmetrical for positive and negative current values.

Fig. 7.8 shows the SWaH look-up table for positive i_{SWaH}. This table is similar to the one obtained from the POC test rig. According to Fig. 7.9 R_{ON} increases only by 2 % when the current varies from 30 A to 180 A at a θ_J of 150 °C. Fig. 7.10 shows R_{ON} as a function of the junction temperature. R_{ON} increases by 64 % when θ_J rises from 30 °C to 150 °C at a current of 180 A.

Fig. 7.11 shows the SWaH look-up table for negative i_{SWaH}. When i_{SWaH} is negative the antiparallel diode conducts part of the current. Due to the nature of the current pulse test, the junction temperatures of MOSFET and antiparallel diode are identical. The effect due to the conduction of the diode is visible in Fig. 7.12, where R_{ON} is represented as a function of i_{SWaH} at different values of θ_J. For a θ_J of 50 °C, R_{ON} is constant with i_{SWaH} within -30 A to -100 A while it drops in the current range -110 A to -180 A. This second region is where the antiparallel diode takes over and conducts part of the current.

According to Fig. 7.12, the R_{ON} discontinuity starts earlier (for a lower current in absolute value) at higher temperature (e.g. -110 A @ 50 °C, -60 A @ 150 °C). This is consistent with the theory, in fact, the forward threshold voltage of a diode tends to became lower when the temperature increases. The R_{ON} of $SWaH$ as a function of θ_J for negative currents is shown in Fig. 7.13. When θ_J rises, the resistance of the device increase consequently, however the increase is less pronounced if compared to the case with the positive current. R_{ON} increases by 36 % when the temperature varies from 30 °C to 150 °C at a current of -180 A.

In conclusion, the negative current part of the R_{ON} maps will not be used for temperature estimate, because the test conditions during the commissioning and in operation are not the same when both the MOSFET and the diode are conducting. During the commissioning, the junction temperatures of both the MOSFET and diode are known and measured. However, during operation, the diode and MOSFET temperature conditions might be different. Fig. 6.11 shows that the MOSFET and the antiparallel diode have different dies, in turn they have different junction temperatures during the normal operations of the converter.

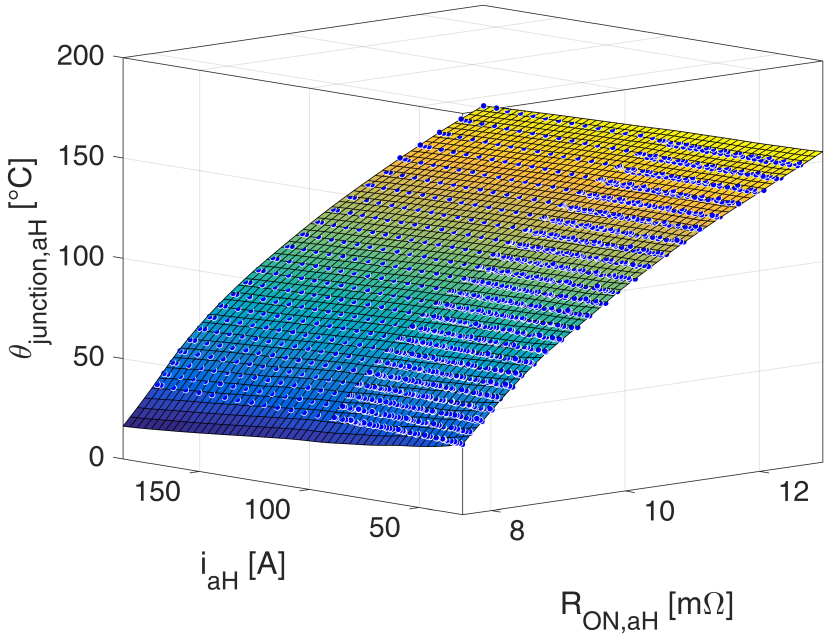


Fig. 7.8: Map of the switch SWaH for i_{SWaH}>30 A obtained from the current pulse test.

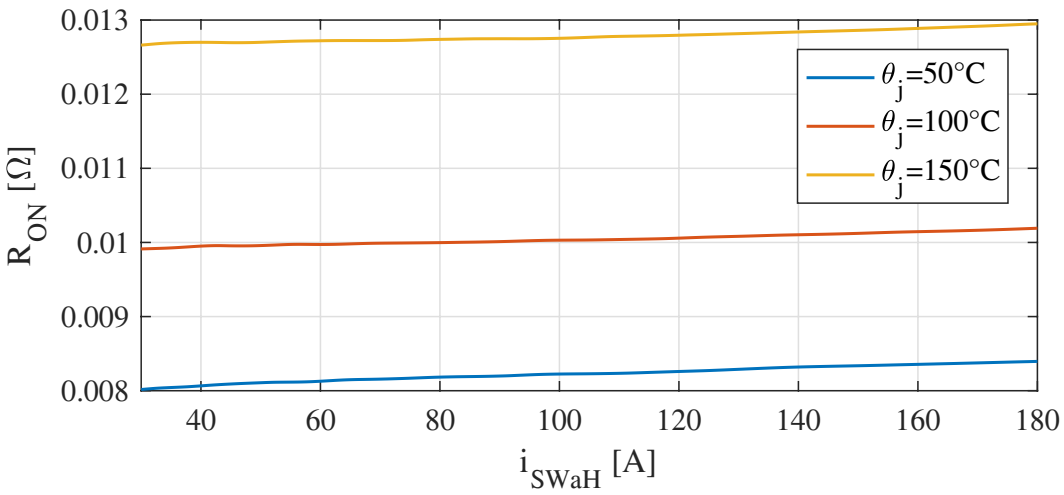


Fig. 7.9: R_{ON} as a function of current for i_{SWaH}>30 A.

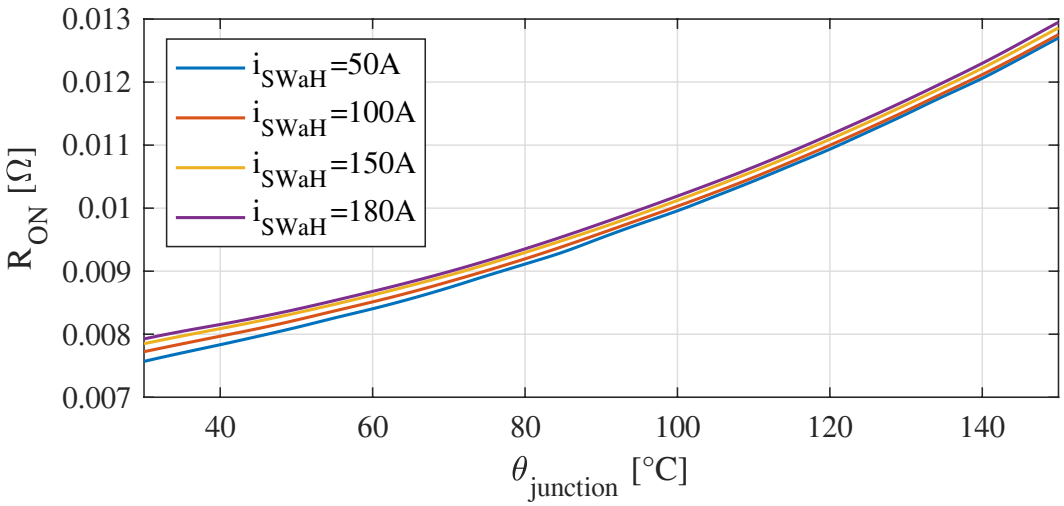


Fig. 7.10: R_{ON} as a function of θ_J for switch SWaH.

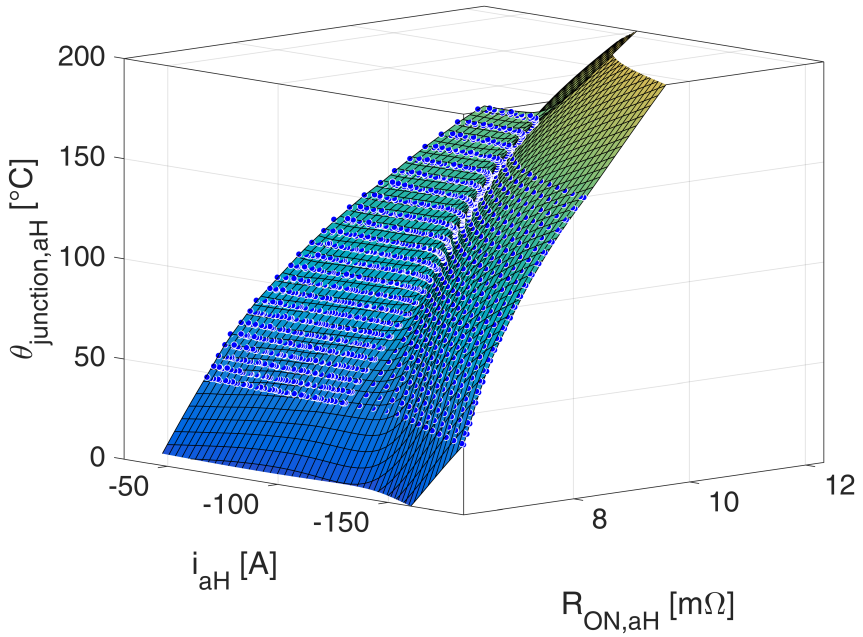


Fig. 7.11: Map of the switch SWaH for i_{SWaH}<-30 A obtained from the current pulse test.

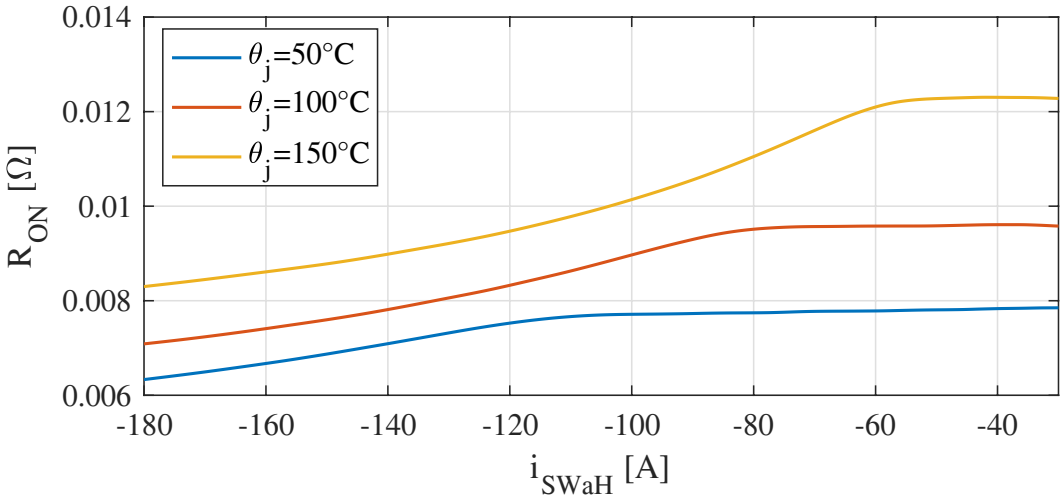


Fig. 7.12: R_{ON} as a function of current for i_{SWaH}<-30 A..

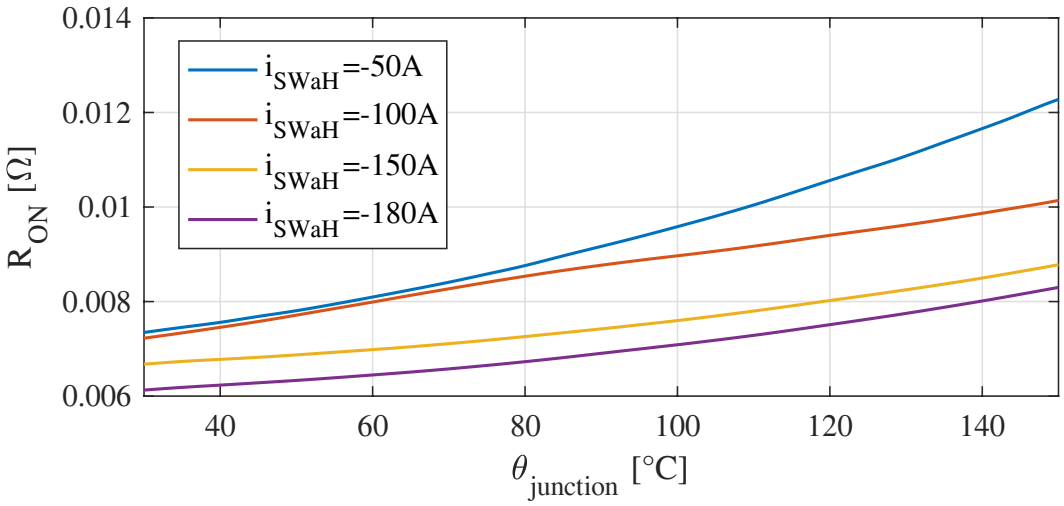


Fig. 7.13: R_{ON} as a function of θ_J for switch SWaH.

7.1.6 Parameters Dispersion

An important aspect that deserves to be investigated is the parametric dispersion. All six switches of the converter have been mapped. Fig. 7.14 shows R_{ON} as a function of the junction temperature for all the six switches inside the converter. The difference between the lower and the higher value is around 2-3 mΩ, depending on θ_J. This clearly shows that in order to have a correct estimation of the junction temperature each device has to be mapped.

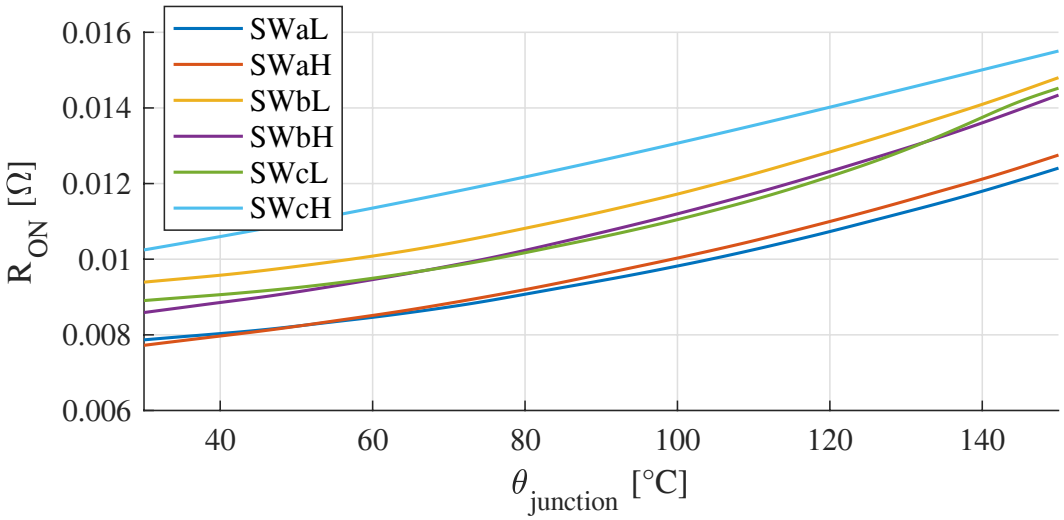


Fig. 7.14: R_{ON} as a function of θ_J. Comparison between all the switches, i_{DS}=180 A.

7.2 Online Temperature Estimation

The functional block diagram of the temperature estimator is shown in Fig. 7.15. The junction temperature of each of the six inverter MOSFETs is estimated only for positive values of i_{DS}.

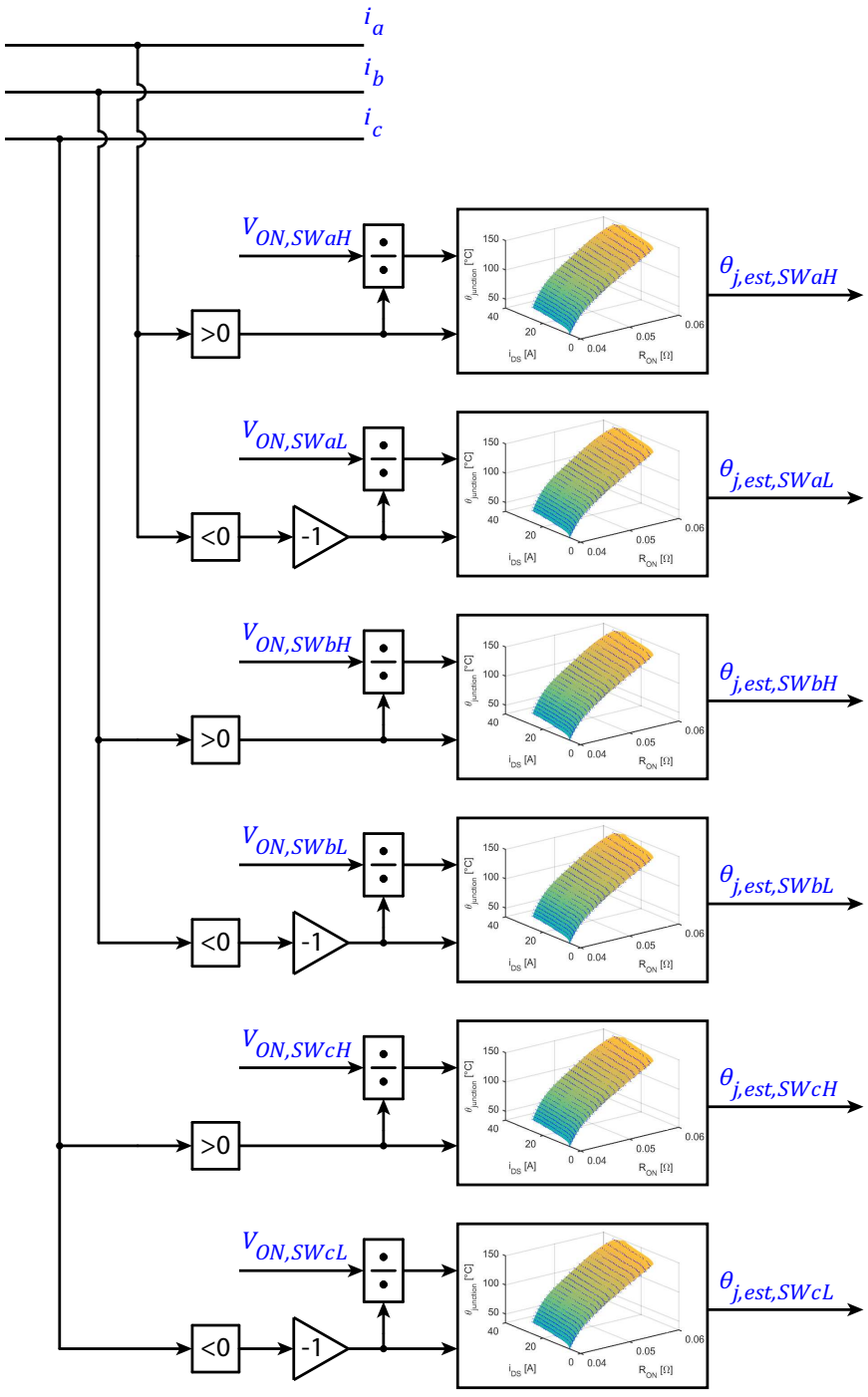


Fig. 7.15: Junction temperature estimator functional block using $\theta_J(R_{ON},i_{DS})$

7.2.1 Online Temperature Estimation Results

The inverter is supplying a purely inductive load. The 3-phase currents are vector controlled at constant amplitude of (120 A) and 0.5 Hz. The obtained results are shown in Fig. 7.16. The top plot shows the three output phase currents (sign convention of Fig. 6.7). The plot in the middle shows the measured heatsink temperature and the estimated temperature of the six MOSFETs. The heatsink temperature represented by a black dashed line is 58 °C and it remains constant during the test. As stated in the previous section it is not possible to estimate the junction temperature of the MOSFET for negative values of i_{DS}. θ_J of all the six MOSFETs is estimated only for i_{DS}>30 A. When it is not possible to estimate the temperature the estimator set $\theta_{J,est}$ to zero. The bottom plot shows V_{ON} of SW1aH and SW1aL. The voltage drop is not symmetrical, for negative currents the antiparallel diode conducts part of the MOSFET current. Tests at higher currents are not available at the moment due to problems with the debug interface. At high currents the EMI caused by the commutations disturb the communication between the control board and the debugger. Despite the converter can continue to operate, it is not possible to download the data. The author is confident to be able to present the data up to 180 A in the near future.

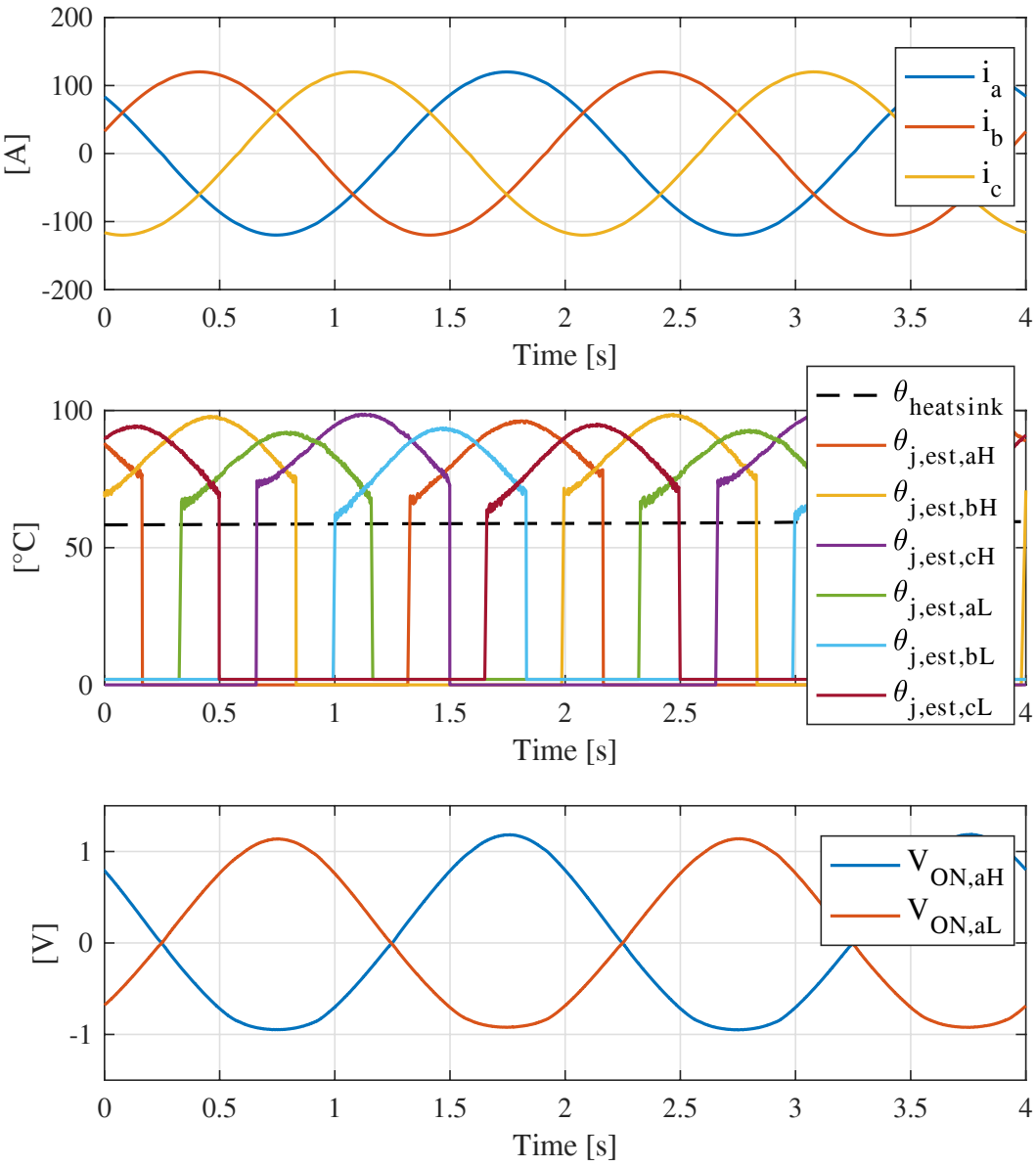


Fig. 7.16: Top: Output phase currents. Middle: $\theta_{J,est}$ of the six switches and measured heatsink temperature. Bottom: V_{ON} of SWaH and SWaL.

7.2.2 Online Temperature Estimation Considerations

As shown in the plot in the middle of Fig. 7.16, $\theta_{J,est}$ of the six MOSFET is sensibly different. $\theta_{J,est}$ of SWaH, SWbH and SWcH, is higher than $\theta_{J,est}$ of SWaL, SWbL and SWcL. The temperature difference in this case can be up to 9 °C. Taking into account the available data the author is not able to provide a precise answer. However, a couple of hypotheses can be done.

- The thermal paths of the MOSFETs SWxH and SWxL are different. Fig. 7.17 shows the internal layout of the power module, the "metallized areas" of the high and low switch have been indicated by a red dashed line. A bigger "metallized area" can help the heat extraction, however in the opinion of the author this is not sufficient to explain the temperature difference.
- The over temperature can be caused by a parametric dispersion due to the manufacturing process. Due to the limited number of tested devices, it is not possible to state that the MOSFET SWxH has always a θ_J greater than SWxL.
- The proposed methodology is estimating the wrong temperature. According to Fig. 7.17 each MOSFET consists of five die in parallel, this can affect the temperature estimation. Also the connections can affect the temperature estimation. More investigation will be done.

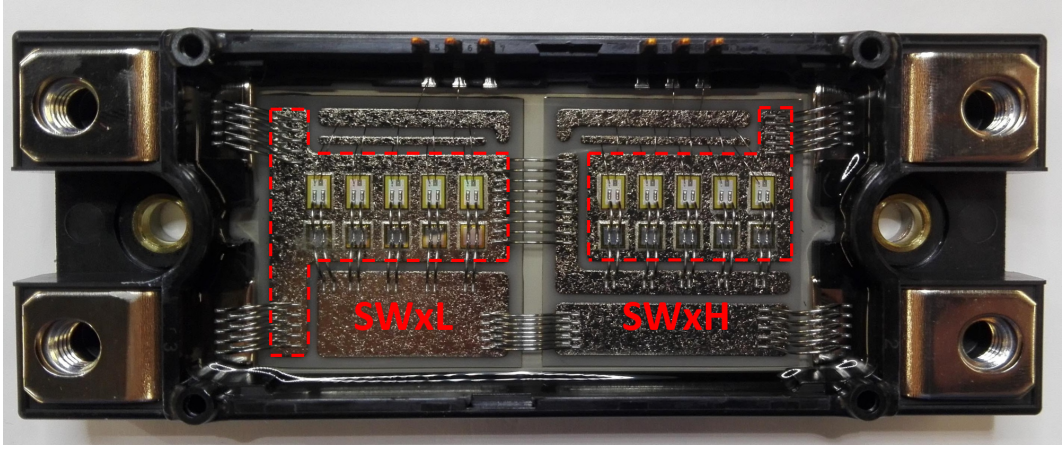


Fig. 7.17: Internal layout of the power module. Red dashed line indicates the two metallized areas.

Chapter 8

Conclusions

Starting from the well known dependency of θ_J from i_{DS} and V_{ON}, a practical method for estimating the junction temperature implementable in real-world converters has been presented. Two prototype converters have been built to demonstrate the feasibility of the proposed methodology. The POC test rig consisting of a SiC power MOSFET module connected in h-bridge configuration has been presented in Chapter 3. The commissioning test procedure to map one device has been presented in Section 4.1.1. Experimental results showing the junction temperature estimation and closed-loop limitation have been presented in Section 4.3. The validation of the proposed method against an IR thermal camera has been presented in Section 4.4.1. The robustness and repeatability of the proposed methodology have been demonstrated in Section 4.4.4 and Section 4.4.3. In Chapter 5 an "advanced" commissioning test that permits to estimate the health state of the SiC MOSFETs has been presented, after accelerated aging of the power module under test. Following the good results obtained from the POC demonstrator, a high power density three phase inverter was realized for the "Squadra corse" of the Politecnico di Torino. The inverter hardware description has been presented in Chapter 6. The commissioning test for mapping all six MOSFETs of the converter and the experimental results showing $\theta_{J,est}$ have been presented in Chapter 7.

The main conclusions of this work can be summarized as follow:

1. The junction temperature is measured in real-time, with high precision.
2. The average die temperature is estimated within 3-4 °C. Hot spot temperature may differ from estimated values by higher values (in the range of 10 °C, according to the observations in this thesis).
3. The temperature map identification is feasible with little modification to the converter (hot plate) and no extra measurement. Moreover, it is repeatable and inherently immune from systematic imprecisions of the V_{ON} measurement system, provided that such imprecision remains the same over the life of the converter.

4. The thermistor used for temperature mapping might be inside the module (any position) or on the heatsink. The method showed little sensitivity to this aspect.

5. The proposed method is extremely robust and feasible, if compared to other TSEP techniques.

6. The precision of the proposed method is comparable to that of having an optical fiber per device, one or two orders of magnitude more precise of any thermistor-based temperature evaluation. Even with the thermistor in contact with the die, temperature errors of 50 °C or more were observed.

7. The temperature estimate becomes pessimistic as the device ages, which leads to a conservative temperature monitoring. However, the over-estimate is not so evident respect to early life condition to be considered a stand-alone prognostic warning.

8. The V_{ON} mapping and temperature monitoring principles were extended to the three-phase voltage source inverter, where all six switches are monitored for both positive and negative currents. Such generalization further validated what shown with the first POC on a more complicated architecture.

9. One important generalization is to have shown that the mismatch of R_{ON} does not reflect into the accuracy of temperature estimate: the non-identical temperature curves of the six devices are real temperature mismatches, related to slightly different thermal paths of the high- and low-side components of each module rather than on the R_{ON} mismatch.

10. A new methodology for putting in evidence the age of the component has been implemented and integrated into the V_{ON} based monitoring package.

11. Altogether, the thesis demonstrates that real-time junction temperature observation is feasible and gives substantial advantages in terms of performance (a lower temperature margin means more output current) and reliability (the power module cannot fail due to over-temperature).

8.1 Prospect Applications

The proposed methodology can be implemented in all types of switching converters with limited extra complication and cost. The applications that would most benefit in using the proposed methodology are:

1. Applications with discontinuous duty-cycle and frequent transient overload of the converter. Examples are automotive and servo-drives.

2. Cost-critical applications, where the cost of the power module represents a non-negligible fraction of the system cost. The temperature feedback permits to design the converter with devices (or modules) of minimum current size, e.g. reducing the cost of the converter. Examples are fields with high production volumes such as automotive and home appliances.

3. Safety critical applications, where failure or malfunctioning may result in serious services disruptions. This include aerospace and medical applications.

4. Applications were the downtime is costly, such as oil and gas, energy production and critical industry applications.

5. Applications where ambient temperature is extremely high, and temperature estimate becomes even more critical.

6. High power applications were safety margins on the components are costly.

7. High power density applications where cooling systems and components must be fully exploited.

In turn, in the short term the benefits of temperature feedback and aging prediction will be of interest of high-end and high-performance applications, where SiC power MOSFETs are more likely to be applied first. In performance-critical applications where the cost of SiC is accepted, the marginal cost of the extra Von circuitry and the customization of the gate-drivers are probably non critical. In the midterm, as the cost of SiC devices will become more competitive for general purpose applications, it is foreseeable that the proposed methods will be usefully adopted for increasing the reliability and the prognostics of power converters in any application.

8.2 Future Work

Future work will focus on:

- **Testing a wider range of devices.** Namely, testing different high-current devices, where multiple dies are connected in parallel, and completing the thermal camera (or the like) validation for this class of devices.
- **Running the commissioning test without the hot plate.** For now, the converter commissioning needs that the heat sink is heated to high temperature, and the temperature map covers a temperature range that coincides with the maximum heatsink temperature during commissioning. Current studies are investigating the possibility of mapping the devices in a limited range of temperatures and then extrapolating the look-up table values at higher temperatures.

- **Thermal network evaluation.** The high bandwidth of the temperature estimate permits to measure the fast thermal transient, that can then be used to calibrate the equivalent thermal network of the component. After the thermal network is known, the aging of a component but also manufacturing defects such as a bad connection with the heat sink can be easily spotted, eventually with the help of artificial intelligence.
- **Integration of the V_{ON} measurement circuitry into the gate-driver.** The additional circuitry must be integrated into the gate driver, with modest extra cost, high accuracy and no deterioration of the gate-driver circuitry layout. Usually, the gate drivers integrate the desaturation protection based on V_{ON} feedback. In turn, the additional measurement seems to be feasible without affecting the cost and reliability of the converter.
- **Junction temperature estimation in the presence of antiparallel diode.** The diode can be mapped separately by turning OFF the MOSFET when i_{DS} is negative. If the look-up table of the antiparallel diode is used in joint with the look-up table of the MOSFET and diode aggregate (the one shown in the thesis), then it should be possible to separate the MOSFET and antiparallel diode temperature estimate.

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