Wake-Up Oscillators with pW Power Consumption in Dynamic Leakage Suppression Logic

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***Abstract*— In this paper, two circuit topologies of pW-power Hz-range wake-up oscillators for sensor node applications are presented. The proposed circuits are based on standard cells utilizing the Dynamic Leakage Suppression logic style [4]-[5]. The proposed oscillators exhibit low supply voltage sensitivity over a wide supply voltage range, from nominal voltage down to the deep sub-threshold region (i.e., 0.3 V). This enables direct powering from energy harvesters or batteries through their whole discharge cycle, suppressing the need for voltage regulation.**

Post-layout time-domain simulations of the proposed oscillators in 180nm show a power consumption of 1.4-1.7pW, a supply-sensitivity of 55-40%/V over the 0.3V-1.8V supply voltage range, and a compact area down to 1,500µm^2. The very low power consumption makes the proposed circuits very well suited for energy-harvested systems-on-chip for Internet of Things applications.

***Keywords*—Relaxation oscillator, wake-up oscillator, pW-power, Internet of Things, Dynamic Leakage Suppression logic**

I. Introduction

The demand for miniaturized and long-lived sensor nodes for the Internet of Things (IoT) has led to the necessity of integrated systems with extremely low power consumption that fits the average power delivered by small energy harvesters [1]-[2]. Such low power consumption is typically achieved by duty cycling the sensor node, which is periodically woken up by oscillators with very low duty cycle and oscillation frequency. Due to their very tight power budget, such sensor nodes invariably rely on asynchronous and event-driven wireless communications [3]. Compared to quartz oscillators, this drastically relaxes the frequency accuracy and stability (e.g., 10-20%) requirements, enabling substantial power savings in the wake-up oscillator. In turn, the power consumption of the wake-up oscillator is critical, since the oscillator is always on, hence its power represents the minimum attainable by the sensor node under heavily duty-cycled operation [5]-[8]. For this reason, various wake-up oscillators with deep sub-nW power have been recently proposed [6]-[12].

Conventional on-chip wake-up oscillators require ancillary circuitry such as current and voltage references, as well as voltage regulation. However, the quiescent power of current state-of-the-art references/voltage regulators is in the order of nWs or higher [13]-[14], and easily exceeds the intrinsic power consumption of the oscillator. Accordingly, the dismissal of voltage regulation and references is essential to truly take advantage of deep sub-nW oscillators [6]-[12].

In this paper, two novel and compact wake-up oscillator topologies are introduced to achieve low sensitivity to the supply voltage at pW-range power consumption, which is the lowest reported. The oscillators are based on the dynamic leakage suppression (DLS) logic style, which was introduced in [4]-[5]. The proposed oscillators can operate with no voltage regulator or current reference in a supply voltage range from 1.8 V down to 0.3 V, which is the widest reported to date. The first topology (AEFF oscillator) targets area efficiency and requires a flying capacitor, which in turn requires the availability of metal-oxide-metal (MoM) or double-poly capacitors in the adopted process. The second topology (NOFLY oscillator) does not have any flying capacitor, hence the capacitors determining the oscillation frequency are grounded, and can be implemented with ubiquitously available MOS gate oxide capacitors.

This paper is structured as follows. The properties of DLS logic relevant to the design of oscillators are first summarized in Section II. Based on the general concept introduced in [6], two novel topologies of DLS-based oscillators are introduced in Section III. Design aspects and validation are discussed in Section IV. Concluding remarks are finally reported in Section V.

II. Class of Wake-Up Oscillators Based on Dynamic Leakage Suppression (DLS) Logic

A. DLS Logic Style

The Dynamic Leakage Suppression (also known as Ultra-Low-Power) logic style was introduced in [4]-[5] to drastically reduce the standby power of digital standard cells, at the cost of substantially degraded speed. In particular, the standby power is typically two-three orders of magnitude lower than regular transistor leakage (i.e., at zero gate-source voltage), and the typical gate delay is in the millisecond range. These two combined features make DLS

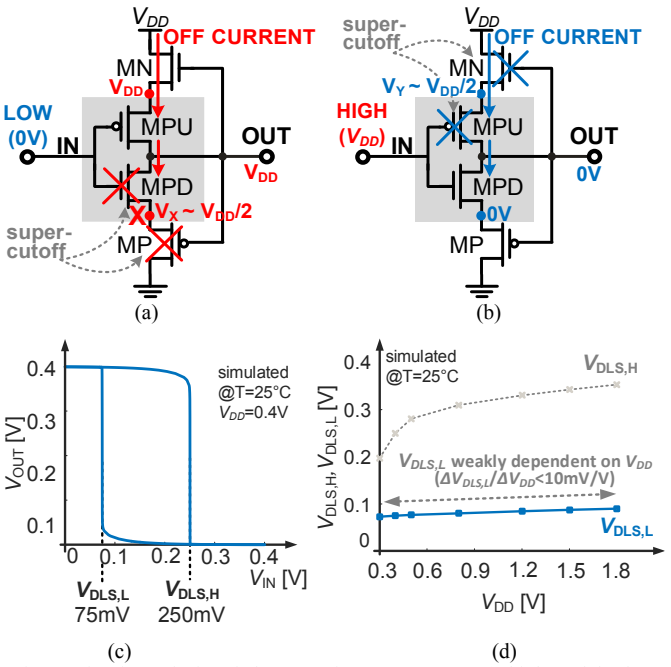

Fig.1. Circuit analysis of the DLS inverter gate at a) high and b) low output, c) static transfer curve characteristics, d) hysteresis windows amplitude over the power supply.

logic very well suited to wake-up oscillator design, as they need to be slow (Hz range [6]-[12]) and hence their consumption is invariably dominated by the standby power. In Subsection B, other relevant and less obvious properties of DLS logic will be uncovered.

As a representative example, the DLS inverter gate is sketched in Fig. 1, where the DLS pull-up (MPU) and pull-down (MPD) transistors are the same as in a standard CMOS inverter (same observations hold for any other standard cell). In addition, DLS gates include an NMOS header transistor MN and a PMOS footer MP, whose gate terminal is driven by the cell output, thus creating a feedback loop. In turn, this loop is responsible for significant standby current reduction and hysteretic behavior, as discussed below.

Regarding the standby current drawn by DLS logic gates, Fig. 1a shows that a low input turns off MPD and sets the output high, which in turn switches off the PMOS footer MP. Since the drain currents of MPD and MP are equal, the voltage V_x of their common node X settles to a value that is close to $V_{DD}/2$ [4]-[5]. This translates into a negative gate-source (source-gate) voltage in MPD (MP) around $-V_{DD}/2$, and hence super-cutoff operation [15]. Dual considerations hold for a high input, which leads to super-cutoff operation in MN and MPU, as shown in Fig. 1b. Being in the super-cutoff region, the standby current of DLS logic gates is two to three orders of magnitude below the regular leakage current. In 180-nm CMOS, the inverter gate standby current becomes 10 fA/gate [4] (i.e., about 700X lower than regular leakage), and is even lower for other logic gates with stacked transistors.

The positive feedback loop in DLS logic also introduces hysteresis in the static transfer characteristics. As shown in Fig 1c, the DLS inverter has low (high) input threshold $V_{DLS,L}$ ($V_{DLS,H}$) equal to 75 mV (250 mV) at V_{DD}=0.4 V. Interestingly, from the plot of the hysteresis thresholds versus V_{DD} in Fig. 1d, both DLS thresholds weakly depend on V_{DD} . In detail, the low hysteresis threshold $V_{DLS,L}$ exhibits a very low supply sensitivity of 10 mV/V over the wide supply voltage range from 1.8 V down to 0.3 V.

The above interesting properties make DLS logic very well suited for wake-up oscillators. First, the current delivered to the load by DLS gates is very small (pA range), allowing Hz-range operation with small on-chip capacitors, and hence low area. Second, the transistor ON current is rather insensitive to V_{DD}, and permit to eliminate the voltage regulator. Similarly, the hysteresis thresholds of DLS logic gates are relatively independent of the supply voltage, and can hence be leveraged to create a stable switching threshold that sets the oscillation frequency, as routinely required by relaxation oscillators. Third, the dominant standby current drawn by the DLS logic style is also relatively voltage-independent, which avoids the traditional drastic increase in the power consumption, when V_{DD} is increased from sub-threshold to nominal voltage. In the next section, these properties of DLS logic will be exploited to introduce two novel relaxation oscillators.

B. Prior Art in DLS-Based Oscillators

The broad class of oscillators based on DLS logic was recently introduced in [7], which leveraged the properties discussed in the previous subsection to derive a first example of oscillator topology with pW-power. The oscillator in [7] is shown in Fig. 3a, where all gates are in DLS logic style. The oscillation frequency is set by the Metal-on-Metal (MoM) capacitor C. Nodes A and B drive the DLS inverter gates G1a-b, and are driven by the outputs $\overline{Q}$ and Q of the latch G3a-b. G3a-b are loaded by G4a-b with short-circuited input/output. G4a-b act like inverter gates and hence serve as active load of G3a-b, once the terminal ENABLE in Fig. 3a is asserted to start the oscillation. The size ratio of G3a-b and G4a-b sets the high (low) DC voltage $V_{AB,H}$ ($V_{AB,L}$) of v_A and v_B, which is 275mV (32mV) under minimum-sized gates and V_{DD}=0.4V (see Fig. 4).

The waveforms of the voltage v_A (v_B) at node A (B), as well as the oscillator output voltage, are reported in Fig. 3b. If $\overline{Q}$ is assumed to be high (Q is assumed to be low) at the beginning of a period (t_0 in Fig. 2b), $v_A = V_{AB,H}$ since G3a is pulling $\overline{Q}$ high and is loaded by G4a (see above). On the other hand, $v_B = V_{MAX} > V_{AB,H}$ at t=t_0, from the analysis at the end of the oscillation period (see below). After t_0, v_B is pulled down by the DLS gate G3b, which draws a small (~3pA) and nearly supply-independent current I_{DLS} that discharges C. During this transient, v_B drops down until it crosses the switching threshold $V_{DLS,L}$ of G1b at t=t_1 in Fig. 3b, whereas node A remains "inactive" at the voltage $V_{AB,H}$.

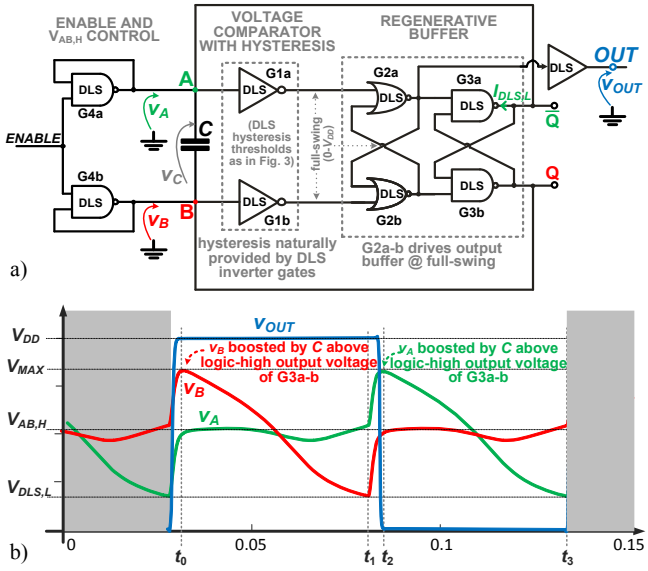

Fig. 2. a) DLS wake-up oscillator in [7] and b) related waveforms.

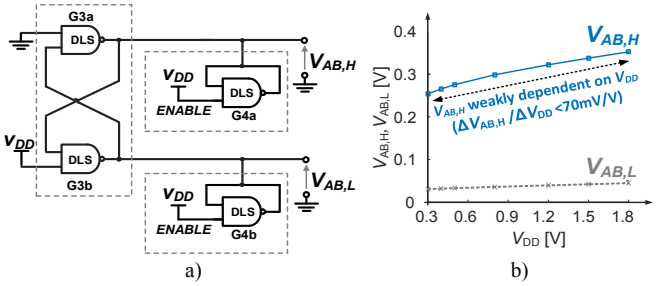

Fig. 3. a) DLS latch G3a-b loaded by G4a-b with short-circuited input/output, has b) weak supply dependence of high and low output voltage $V_{AB,H}$ and $V_{AB,L}$.

Hence, the capacitor voltage at $t=t_1$ becomes $v_C = v_A - v_B = V_{AB,H} - V_{DLS,L}$. Right after t_1, the low value of v_B and the inverting behavior of G1b, G2b and G3b pull Q high, raising v_B to the G3b high output voltage $V_{AB,H}$ (see $t=t_2$ in Fig. 3b). As C maintains the same voltage $v_C = V_{AB,H} - V_{DLS,L}$ before/after the transition, $v_A = v_B + v_C$ is pulled up from $V_{AB,H}$ to $V_{MAX} = V_{AB,H} + (V_{AB,H} - V_{DLS,L}) > V_{AB,H}$. At this point, a semi-period $T/2$ is completed, and a new semi-period with inverted signals starts (same as above, swapping Q and $\overline{Q}$, v_A and v_B). A full-swing output OUT is restored by the G2a-b latch, and is a square wave with nearly 50% duty cycle and period $T \approx 4C(V_{AB,H} - V_{DLS,L})/I_{DLS}$ (constant-current discharge of C, see Fig. 3b). The period T has low sensitivity to the supply voltage since $V_{AB,H}$, $V_{DLS,L}$ and I_{DLS} are all weakly supply-dependent in DLS logic (see Figs. 1d and 4b). The power consumption is dominated by the static sub-leakage current drawn by transistors, which is again rather insensitive to V_{DD} in DLS logic [7].

III. Proposed DLS-based Wake-up Oscillators

In this section, two oscillators belonging to the broad class of DLS-based oscillators are explored.

A. AEFF Oscillator: Area-Efficient Topology

The AEFF relaxation oscillator in Fig. 4a eliminates the active loads G4a-b to further reduce complexity, the associated standby power and to allow full-swing voltage at nodes A and B. Moreover, the inverters G1a-b in Fig.2a are replaced with NAND gates, equivalent to the inverters G1a-b when the ENABLE signal is high. Accordingly, the oscillation period in the circuit in Fig. 4a is defined directly by the low hysteresis threshold of the NAND gates G1a-b in Fig. 4a, which set the lowest voltage at node A and B below which the output makes the opposite transition.

The comparison of Fig. 2a and Fig. 4a reveals that the elimination of G4a-b results in larger voltage fluctuations in the "inactive" node between A and B (e.g., A between t_0 and t_1 in Fig. 4a), when the active node between A and B (e.g., B between t_0 and t_1 in Fig. 4a) is instead being pulled down by G3a. Also, the voltage swing of nodes A and B increases compared to Fig. 2a, which in turn takes more time to complete a transition. In turn, this allows operation at even lower oscillation frequency at the same capacitance C, compared to Fig. 2a. Equivalently, the same (low) oscillation frequency is achieved with a smaller capacitor and lower area, compared to Fig. 2a. In summary, the area efficiency of the AEFF oscillator in Fig. 4a stems from the reduction in the area of capacitor C, and only to a minor extent from the suppression of the inverter gates.

B. NOFLY Oscillator: Topology without Flying Capacitor

Another topology based on the general concept in [7] is presented in Fig. 5a (NOFLY oscillator). In this figure, the active loads of the original topology are dropped as in Fig. 4a. In addition, the flying capacitor C is replaced by two grounded capacitors connected at nodes A and B. Unlike the circuit in [7] and in Fig. 4a, the grounded capacitors can be implemented with MOS capacitors. This is particularly beneficial since the NOFLY oscillator does not require MoM

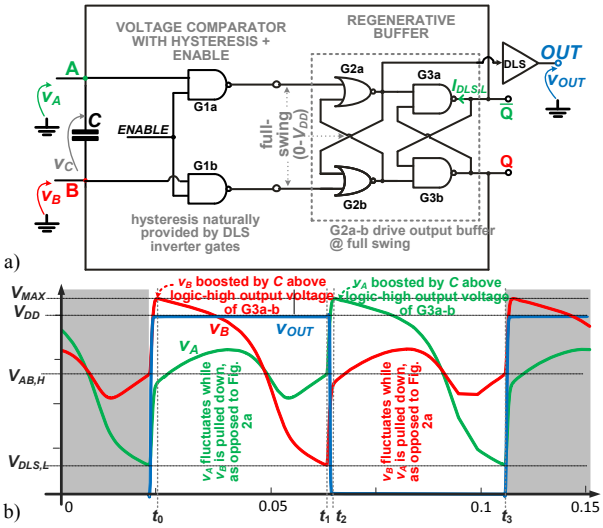

Fig. 4. a) Gate-level architecture of the proposed area-efficient wake-up Oscillator (AEFF Oscillator) and b) related waveforms.

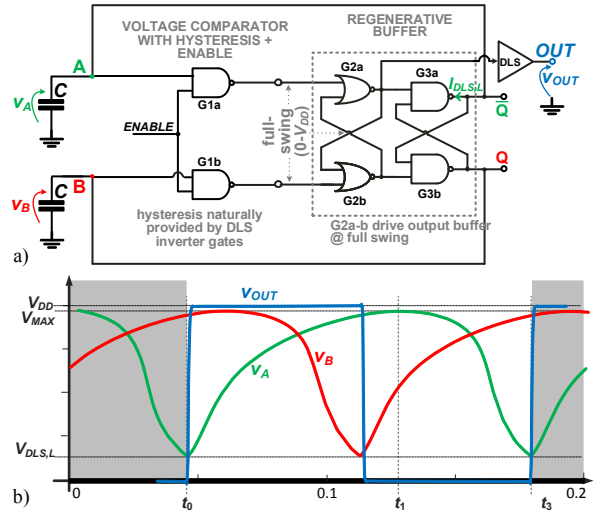

Fig. 5. a) Gate-level architecture of the proposed wake-up oscillator without Flying Capacitor (NOFLY Oscillator) and b) related waveforms.

or double-poly capacitors, as is normally needed to implement a flying capacitor. In other words, the NOFLY topology in Fig. 5a can be implemented in very low-cost processes with very limited metal layers available (which would make MoM capacitors impractical, and area-hungry), and single poly (since no double-poly capacitors are needed). In addition, the ability to operate with simple MOS capacitors in Fig. 5a takes advantage of the relatively high capacitance per unit area associated with such capacitors, which again reduces the area of the capacitor C.

In spite of the seemingly limited circuit differences between Figs. 2a, 4a and 5a, the operation of the NOFLY oscillator is rather different. Indeed, nodes A and B are no longer capacitively coupled to each other. As an interesting consequence, no voltage boosting of node A (B) beyond the logic-high output voltage of G3a-b occurs in Figs. 5a-b during the rising transition of node B (A) at $t=t_0$, as opposed to Figs. 2a and 4a. Accordingly, from Fig. 5b the charge and discharge transient of nodes A and B in the NOFLY oscillator is pronouncedly much more symmetric than in Figs. 2b and 4b. Similar to Fig. 4b, neither A or B is really inactive (i.e., relatively constant) at any point of time, as opposed to Fig. 2b.

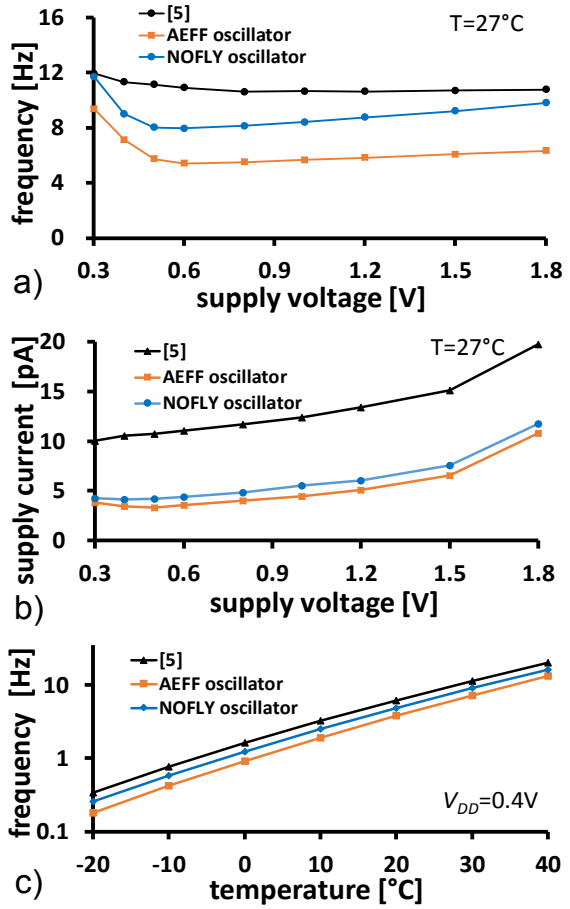

Fig. 6. a) Oscillation frequency versus Supply Voltage b) Power consumption versus Supply Voltage c) Oscillation frequency versus Temperature for the different DLS-based oscillator.

IV. Validation and Performance Comparison

The wake-up oscillators proposed in Section III were designed in 180-nm CMOS, with a relatively small capacitor *C* of 500fF. The oscillators' performance was analyzed via post-layout time-domain simulations. From Fig. 6a, the AEFF (NOFLY) oscillator is expectedly slower than the oscillator with lowest power to date [7] up to 36% (18%), at the same capacitance *C*. In other words, AEFF and NOFLY oscillators need a smaller capacitor than [7], when same frequency is targeted.

The AEFF and NOFLY oscillators preserve the ability to operate from nominal voltage (1.8 V) down to deep sub-threshold (0.3 V), as in [7] and as opposed to the rest of prior art [8]-[12] (see voltage range in Table I). At the same time, the proposed AEFF and NOFLY oscillators can be directly powered from a harvester without voltage regulation (or from a battery across the entire discharge process). Indeed, the frequency sensitivity to V_{DD} of AEFF (NOFLY) is only 14%/V (18%) in the very wide 0.6-1.8V range. This is even lower than prior voltage-regulated oscillators [10]-[11] and assures an error of only 1%(4%) when V_{DD} fluctuates by 100 mV, as certainly acceptable in wake-up oscillators[7]-[12].

Similarly, Fig. 6b shows a very low sensitivity of the current drawn from the supply to V_{DD}, which changes by less than 2X when increasing V_{DD} from sub-threshold to nominal voltage. This means that the proposed oscillators draw approximately the same current from the harvester or battery, even if the supply voltage changes drastically. On the contrary, the current drawn by conventional CMOS oscillators is well known to increase by several orders of magnitude, thus requiring again voltage regulation [8]-[12].

Fig. 6c and Table I show that the sensitivity to the temperature is in line with oscillators employing temperature-compensated references [11]. Since such references are used in AEFF and NOFLY, from Table I these oscillators need to be used in applications where temperature fluctuations are limited (e.g., implantables, indoor sensors, smart clothing, food supply chain management, and so on). In such applications, from Table I the frequency shift is comparable or better than prior art [7], [10], [11], and below 10% under 10% V_{DD} fluctuations.

The proposed AEFF (NOFLY) oscillator exhibits the lowest power to date of 1.4 pW (1.6 pW) at 0.4 V. The 2.5-2.6X improvement over the previous best in class allows true pW-range power consumption, as no additional (and typically much greater) power contribution needs to be considered thanks to the suppression of voltage regulation and reference, as opposed to prior art [8]-[12]. As expected, the area is comparable to [7] and 10% lower in the case of the AEFF oscillator, and 4-160X lower than other prior art.

V. Conclusion

In this paper, two DLS-based relaxation oscillator topologies were introduced. The AEFF oscillator has the lowest area reported to date, whereas the NOFLY oscillator can be implemented in low-cost processes with limited metal stack and no double-poly option. Both oscillators can operate in the very wide voltage range from deep sub-threshold to nominal voltage, and achieve the lowest power reported to date (1.4-1.6 pW), outperforming the previous best in class by 2.5X. Accordingly, the proposed oscillators are well suited for miniaturized (e.g., millimeter-sized) energy-harvested sensor nodes for the Internet of Things.

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Table I. Comparison Table (Best Performance in Bold)

	proposed AEFF	proposed NOFLY	[7]	[8]	[9]	[10]	[11]	[12]
Technology [nm]	180	180	180	55	65	65	180	180
Supply voltage [V]	0.4	0.4	0.4	1.2	0.6	0.5	0.6	1.2
Power* [pW]	**1.4**	1.6	4.2	224	124	44.4	4.2	5,800
Frequency* [Hz]	7	9	11	90	9.3	2.8	18	11
Voltage range [V]	**0.3 - 1.8**	**0.3 - 1.8**	**0.3 - 1.8**	1.1 to 3.3***	0.6 to 1.1	0.48 to 0.52	N/A	1.2 to 2.2
Supply sensitivity [%/V]	14**	18**	0.8**	0.93****	1.6****	160****	50****	1****
Temperature range [°C]	-20 to 40	-20 to 40	-20 to 40	-5 to 95	-40 to 120	-40 to 60	-30 to 60	-10 to 90
Thermal drift**[ppm/°C]	13,000	16,000	20,000	260	1,000	1,260	20,000	45
Frequency shift @ 10% V_{DD}, 5°C temper. change	7.9	9.8	10.1	0.22	0.66	16.63	15	0.12
Area (μm²)	**1,500**	2,100	1,600	57,000	9,100	6,035	N/A	240,000
Volt. regulator/temp.-comp. curr. ref. requires	**NO / NO**	**NO / NO**	**NO / NO**	YES / YES	YES / YES	YES / NO	YES / YES	YES / YES

* Performed at V_{DD}=0.4V ** On the supply voltage range [0.6 - 1.8V] *** 3.3V operation is due to thick-oxide transistors **** Obtained with regulated supply

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