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PhD Thesis - Abstract

The world of wireless communications is in rapid evolution and communication service providers presently face several challenges related to the evolution to next generation (5G) networks. A major one is how to build the capacity required, while keeping the system as efficient and flexible as possible. Simultaneously, the increasing pervasiveness of the infrastructure calls for limited cost and complexity. In a microwave transceiver front end, the power amplifier present in the transmitting chain is often the bottleneck to the overall system efficiency and, at the same time, it strongly affects linearity.

This thesis is split into two focus areas, each facing some of these challenges from a different perspective of the design and operation of power amplifiers. The first part analyses some solutions that involve the circuit- and system-level architecture. Two power amplifier architectures based on load modulation, which aim at enhancing the efficiency of transmitters operating with envelope modulated signals, are investigated, realised and experimentally characterised. The design of a Chireix outphasing transmitter is first presented, based on the guidelines extracted from a simplified analysis on the bandwidth limiting factors. It is observed that the device parasitics often represent the main limitation to the achievable bandwidth, and some design strategies are proposed to partially overcome this issue. Secondly, the Doherty architecture is investigated from the point of view of its driving strategies. A comparison of analogous single and dual input Doherty amplifiers is carried out with the aim of quantifying the trade-off between the advantages of the dual input architecture in terms of performance and flexibility, and the increase of cost and complexity brought about by its employment in place of the conventional single input one.
Hence, the second part of this thesis is dedicated to developing cost effective architectures that may replace a single active device with high frequency and high power capabilities. In this framework, the stacked architecture is analysed to exploit a GaAs multi-transistor structure whose performance is comparable to a single GaN device, at a lower cost. The strategy of stacking several transistors in such a way as to overcome the breakdown limit of a single one, which is already quite popular in CMOS, is gaining increasing interest for compound semiconductors, though with several challenges both from the stability and from the layout compactness points of view. The concept is verified by a MMIC cell meant for source and load pull characterisation.

Further investigation of each topic is planned as future development. Concerning the two dual input load modulation architectures, system level characterisation is still ongoing, targeting a fully LUT based approach that enhances flexibility and potentially allows to embed linearisation into the signal conditioning itself. Eventually, the development of GaAs stacked transistor cells with high frequency performance comparable to GaN devices can be merged with the explored complex efficiency enhancement architectures to realise a cost-effective transmitter front end, suitable for next generation wireless systems.