Modular Design of RF Front End for a Nanosatellite Communication Subsystem Tile Using Low-Cost Commercial Components

(Article begins on next page)

24 April 2024

Research Article

Modular Design of RF Front End for a Nanosatellite Communication Subsystem Tile Using Low-Cost Commercial Components

Haider Ali [ID],[1] **Anwar Ali** [ID],[2] **M. Rizwan Mughal** [ID],[3,4] **Leonardo Reyneri,**[5] **Claudio Sansoe,**[5] **and Jaan Praks**[4]

[1]*Department of Electrical Engineering and Technology, University of Technology, Nowshera 24100, Pakistan*
[2]*School of Information Science and Technology, Zhejiang Sci-Tech University, Hangzhou 310018, China*
[3]*Department of Electrical Engineering, Institute of Space Technology, Islamabad 44000, Pakistan*
[4]*Department of Electronics and Nanoengineering, School of Electrical Engineering, Aalto University, FI-00076 Aalto,*
 02150 Espoo, Finland
[5]*Electronics and Telecommunication Department, Politecnico di Torino, Torino 10129, Italy*

Correspondence should be addressed to Haider Ali; haider.ali@uotnowshera.edu.pk

In recent years, the development market for low-cost nanosatellites has grown considerably. It has been made possible due to the availability of low-cost launch vectors and the use of "commercial off-the-shelf components" (COTS). The satellite design standardization has also helped a great deal to encourage subsystem reuse over a number of space missions. This has created numerous opportunities for small companies and universities to develop their own nanosatellite or satellite subsystems. Most COTS components are usually not space qualified. In order to make them work and withstand the harsh space environment, they need extra effort in circuit redesign and implementation. Also, by adopting the modularity concept and the design reuse method, the overall testing and nonrecurring development cost can be significantly reduced. This can also help minimize the subsystem testing times. The RF front-end design presented in this paper is also considered one of the better and feasible choices based on the above approach. It consists of an S-band transceiver that is fully implemented using COTS components. In the transmit chain, it is comprised of the transmitting CC2510 RF matching network and a power amplifier (PA) with an RF output power of up to 33 dBm which connects to an antenna using two RF switches. The receive chain starts from the antenna that is connected through two RF switches to the low-noise amplifier (LNA) that further connects to the receiving CC2510 via the RF matching network. The receiver sensitivity is -100 dBm. This is a half-duplex system using the same antenna for transmitting and receiving. The receiver and transmitter chains are isolated together using two RF switches which together provide an isolation of up to 90 dB at 2.4 GHz. The concept behind using two RF switches is to provide better isolation from the transmit chain to the LNA. The matching network of CC2510 has been designed in a symmetric fashion to avoid any delays. All the RF COTS used have been selected according to link budget requirements. The LNA, PA, and RF switches were tested individually for compliance. The passive components used in the overall design of the matching network are chosen on the basis of minimum dimension, least parasitic behaviour, and guaranteed optimum RF matching. Also, the RF COTS used are non-CMOS which makes them more robust against space radiations associated with the LEO environment and enables them to provide a radio communication data rate of up to 500 kbps in both uplink and downlink. The vacant spaces on the implemented PCB are shielded with a partial ground plane to avoid RF interference.

1. Introduction

In recent years, nanosatellites have gained significant importance in the aerospace market due to their low cost and comparatively shorter development time. However, this has created more demanding requirements for such small missions [1]. One of its key aspects includes the development of an efficient communication subsystem which can fulfill all these requirements [2, 3].

A communication subsystem is a vital functional element for any satellite, and it cannot be overlooked. The ever-increasing bandwidth requirements have driven the designers to move from conventional VHF/UHF bands to more high-frequency bands. This shift is more fluent for medium and large satellites which have abundant resources in terms of power budget and available space. In contrast, for micro-/nanosatellites this technological shift is not so convenient mainly due to the scarcity of available space and power budget [4]. For CubeSat standards, this shift is even more difficult because of hard constraints on space, power budget, and cost [5]. The aim of this work is to implement a feasible design solution that could cater to bandwidth requirements while satisfying these constraints.

This design approach is based on the novel AraMiS (Italian acronym for Modular Architecture for Satellites) approach. The major aim of the AraMiS Project is to go beyond the CubeSat concept and develop a truly modular architecture. In AraMiS, the modularity is employed at several levels that include inception, design, mechanical and electronic implementation and testing levels. Once the modules are developed, they are assembled together as per target mission requirements. This enables various missions to share the cost and human efforts in an effective manner [4].

The AraMiS-C1 (CubeSat standard equivalent of the AraMiS Project) has been realized over a single standard CubeSat module called a tile. In this design, the S-band transceiver has been implemented over half of the telecommunication tile which is not a trivial job. This has been possible by using several design techniques employed for a reduction in terms of dimensions, weight, and power dissipation while still providing desirable performance for telecommunication [4, 5].

2. Modular Architecture Design Approach

According to the AraMiS Projects, the modular architecture approach has been adopted on (i) design, (ii) schematic, and (iii) physical levels. All these approaches have created more reusable, reconfigurable, and upgradable subsystems and modules. It has also reduced the overall design and delivery time of different modules enabling them to meet hard mission deadlines. On the financial front, the overall mission cost has also been reduced significantly as module-wise space qualification almost eliminates the retesting of the same module over another mission (only system integration testing is required for a newer mission) [4, 6].

2.1. Design Level Modularity. UML (Unified Modeling Language) is a modeling language used extensively in high-level object-oriented designs and has become a standard in various applications. UML renders quite a few diagrams that include the class diagram, sequence diagram, use case diagram, requirement diagram, and state diagram. Different diagrams represent system properties in different perspectives. The choice of diagram selection is based upon the system characteristics [7].

UML has been employed for the design and documentation of the AraMiS project. All the subsystem blocks and their functionalities have been described using UML. With regard to the hardware/software architecture of AraMiS, a detailed documentation of each subsystem has been implemented using UML [8]. This design method utilizes a UML class diagram for each module. Under the given approach, each subsystem consists of a hardware part (HW) and a corresponding software (SW) support.

The 1B9_CubeTCT UML class diagram is given in Figure 1. All the subsystem names follow the nomenclature used for their classes in UML. The subsystem names for the 1B9_CubeTCT (or CubeTCT) follow the nomenclature used for them inside UML diagrams [7]. The yellow blocks represent the analog class (or object) that encompasses an inherent software and hardware electronic design. The blue-coloured block represents a class (or object) at the module level that has an association (depicted via arrows) with other subclasses (or objects) and with amber-coloured blocks called component classes (or objects). All these classes have complete characteristics which are required for its description (including operations, arguments, and outputs).

2.2. Schematic Level Modularity. As in the case of the UML class diagram, the schematics were also designed in a modular manner by utilizing Mentor Graphics Schematic Capture and Expedition PCB™ [9]. The main schematic was bifurcated into several blocks and subblocks. This created several advantages over conventional schematic designing, such as ease of reuse for an identical block, convenient upgrading of the same subsystem's module by simply replacing an instance of the same block with an updated one, and ease of schematic troubleshooting and hardware debugging. In a more macro perspective, it helped create a library with several schematic blocks and subblocks that could be used for other space missions. The same methodology can also be followed to design and develop projects in other engineering and technological domains.

In the AraMiS C-1 CubeTCT subsystem, the same approach has been adopted for a schematic design. It includes several blocks and subblocks that assemble to create the final CubeTCT schematic. This helps to ease upgrading, replacing of components, and troubleshooting of CubeTCT.

Figure 2 shows the mentor schematic of the 1B31B1W_OBRF_2_4_GHz (CubeTCT) transceiver, where each block represents a separate schematic. Each schematic block has further subblocks that represent nested schematics. Figure 3 gives another view of the schematic for the onboard RF front-end block (1B131B_OBRF_RF_FrontEnd). Similarly Figures 4, 5, and 6 depicts subblocks that comprises different ICs and passive components. To give an idea on the ease of upgrading, consider a scenario for upgrading the transceiver.
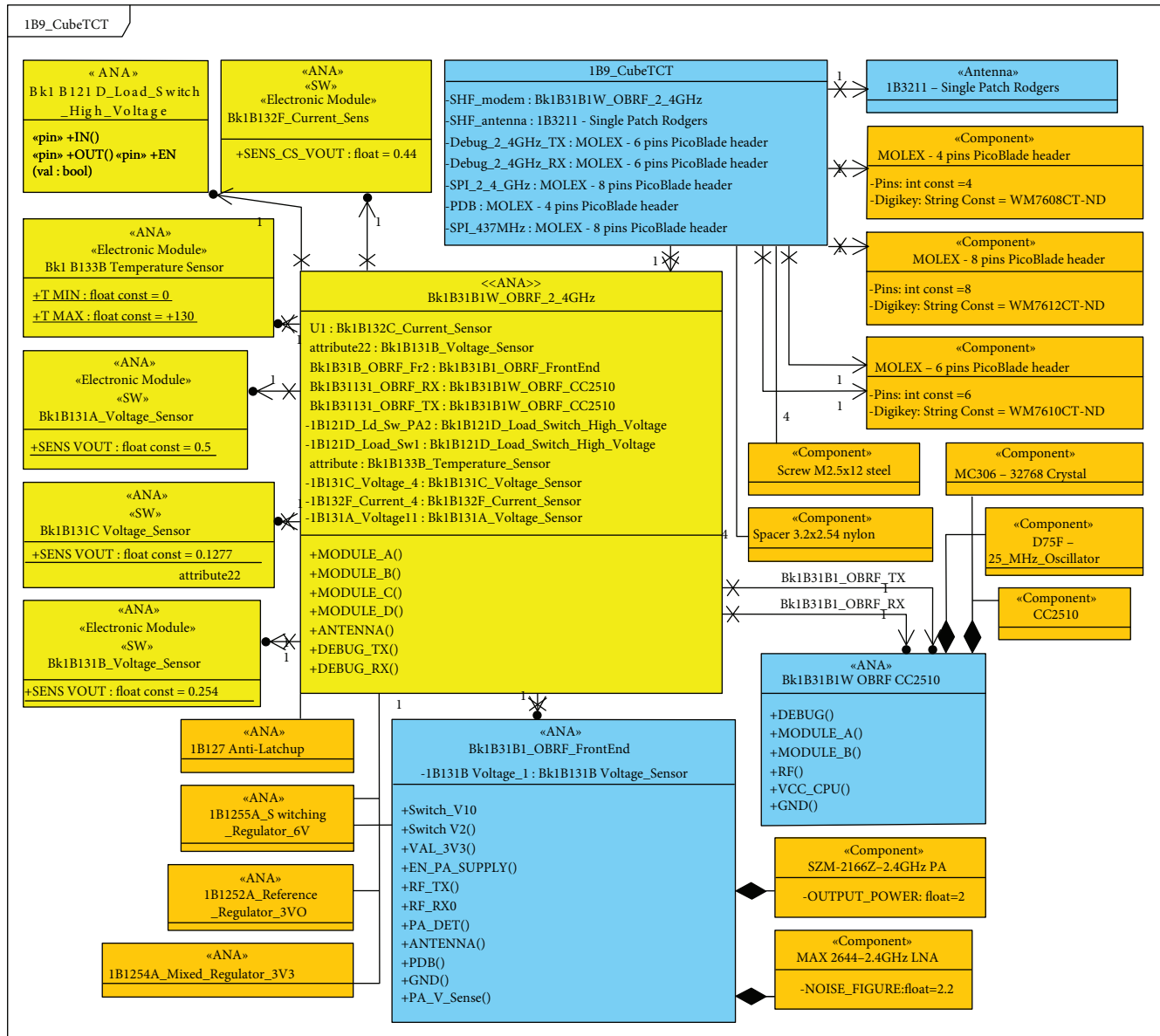
FIGURE 1: UML class diagram for 1B9_CubeTCT showing association with all other subclasses and modules.

It will simply require replacing this schematic block with a new one without redoing the whole subsystem. This schematic hierarchy and classification is a true implementation of the AraMiS modular architecture at the schematic level.

2.3. Physical Level Modularity. A further extension of the modularity concept is based on a plug-and-play modular architecture [6]. This means that a mother board can dock a daughter board by using a module connector. These module connectors are identical in terms of signals (on a schematic level) as depicted in Figure 4 and pin connections (on a hardware level) as shown in Table 1 [9]. Different daughter boards can be connected onto a standard mother board having a number of module connectors. This provides a more instant modular solution with an off-the-shelf choice from already developed daughter boards. It renders a

customization level where one simply physically undocks or disconnects a mother board and replaces it with another one as per mission requirements. For the CubeTCT, this plug-and-play architecture has been provided on a limited schematic and mapping level which is extendable in the future to a physical daughter board level CubeTCT.

3. Aramis C1 and Telecommunication Tile

The AraMiS-C1 is the most recent implementation of AraMiS architecture that is based on CubeSat standard. The design process of AraMiS is based on tiles. Tiles are printed circuit boards that also form the outer structure of the satellite. They have dual functionality: (i) they provide mechanical strength and structure to the satellite and (ii) they provide operational functionality (such as power
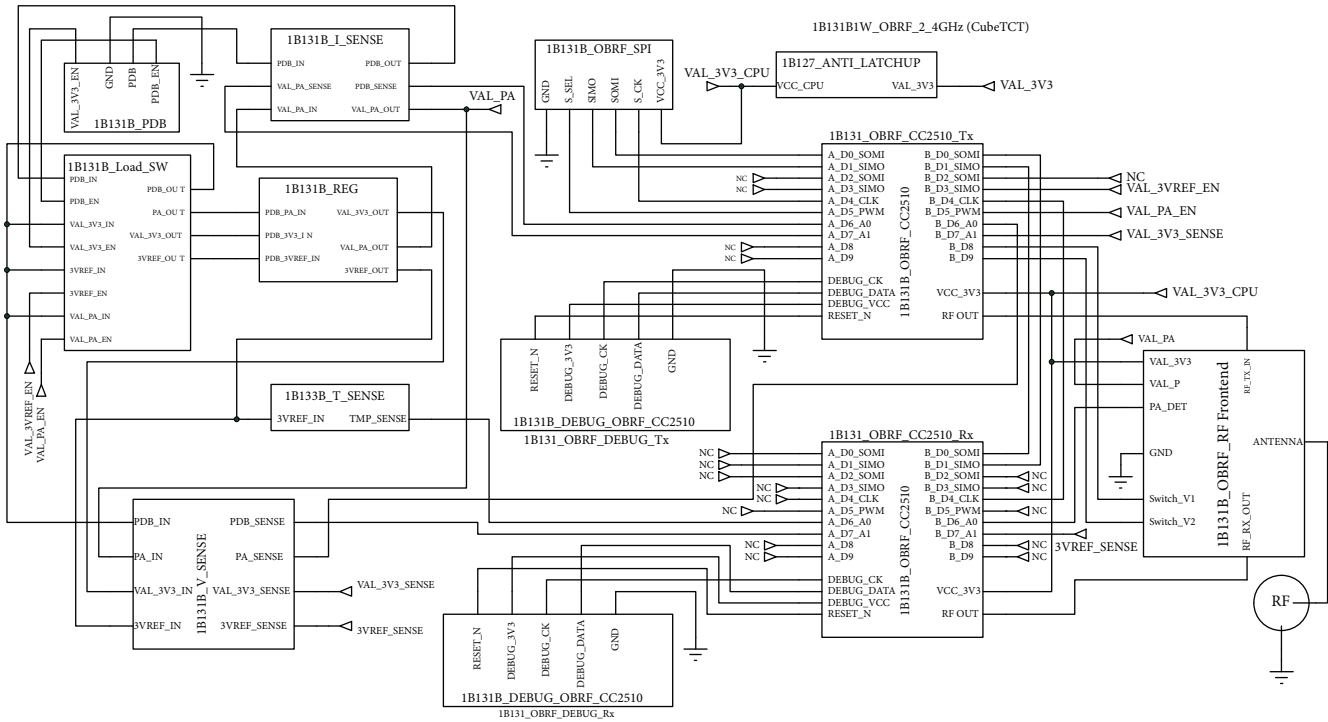
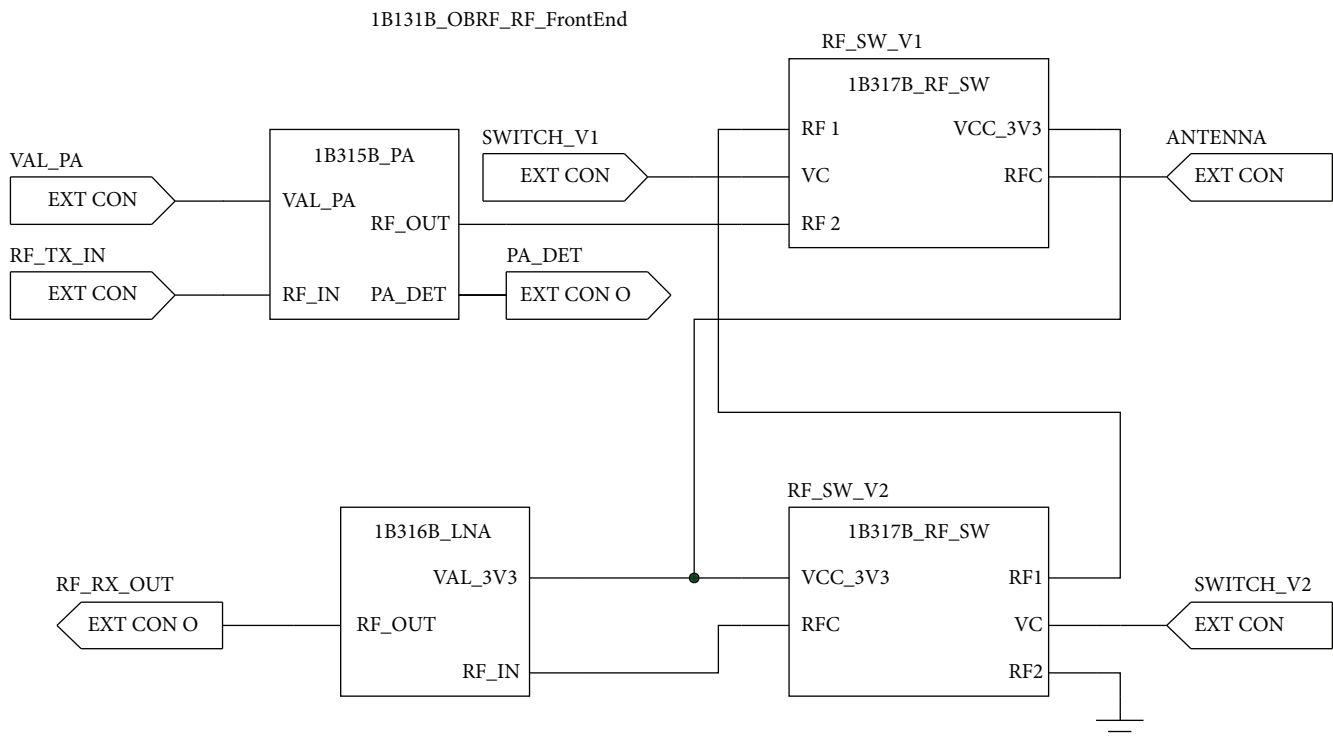FIGURE 2: Mentor schematic of 1B31B1W_OBRF_2_4_GHz (CubeTCT) transceiver.

FIGURE 3: Mentor schematic of 1B31B_OBRF_RF_front end.

management, telemetry, and telecommunications). Inside the satellite, there is room for batteries and payload boards. AraMiS-C1 consists of 4 power management tiles (CubePMT), a telecommunication tile (CubeTCT) with an S-band patch antenna (one side), and a commercial deployable UHF antenna (the other side) mounted on
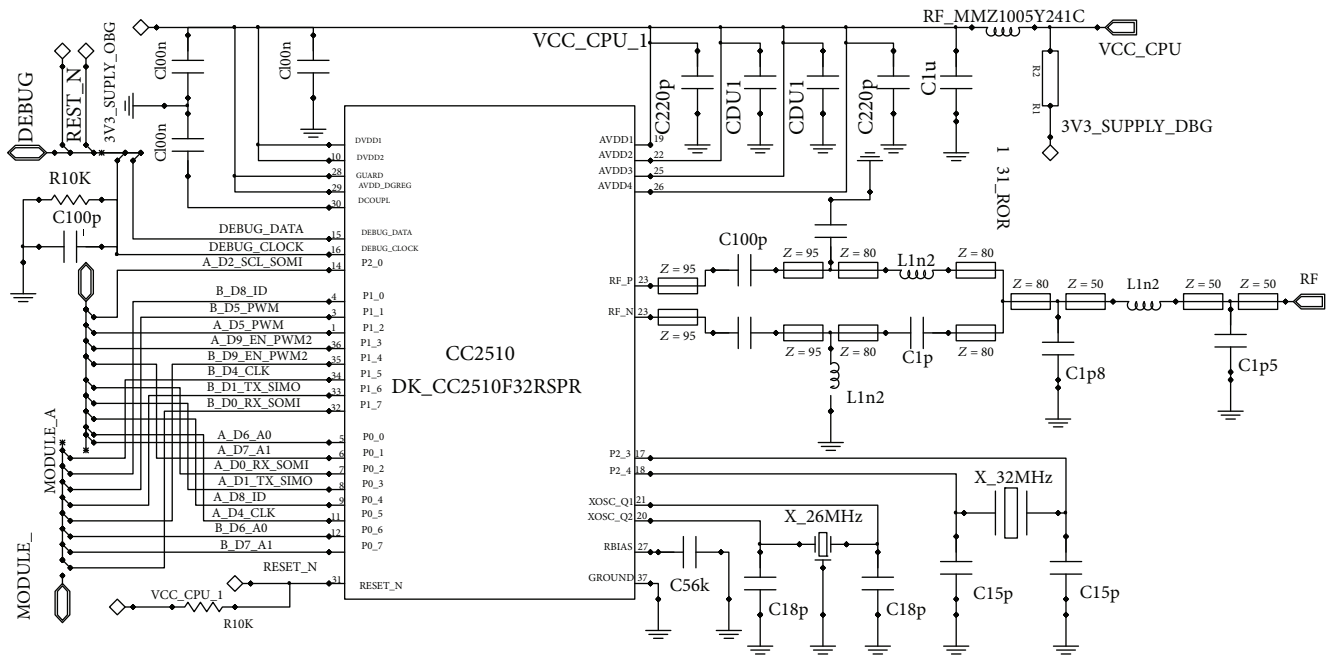
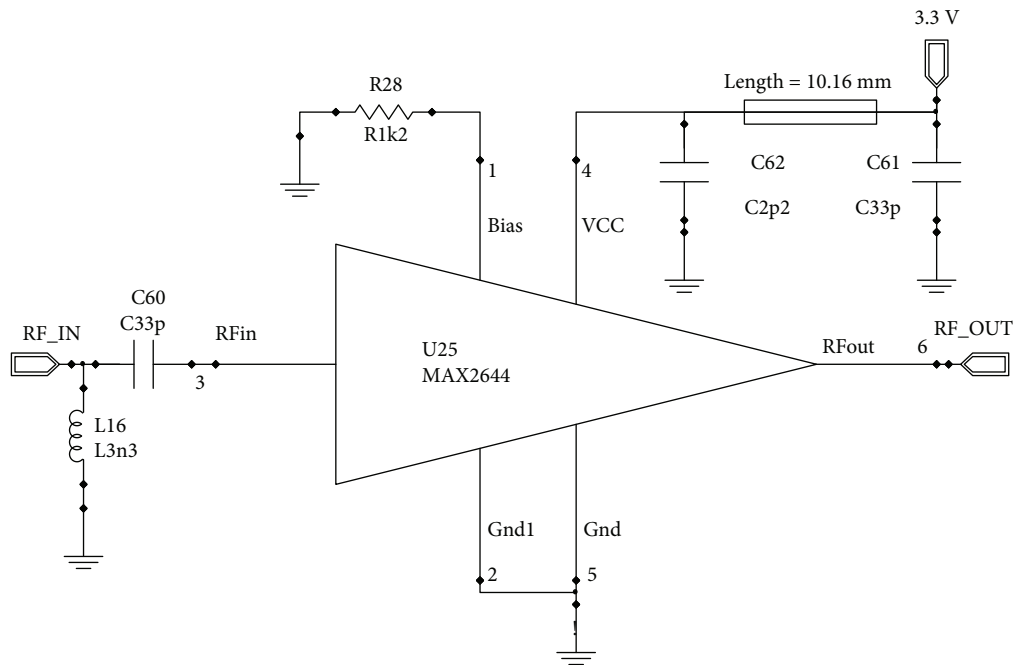Figure 4: Mentor schematic of 1B31B CC2510 transceiver.

Figure 5: LNA schematic of RF front end.

the external face. A photograph of 1U AraMiS-C1 is shown in Figure 7.

The main approach for designing CubeTCT is to realize a high-bandwidth communication link using low-cost COTS components which are available in the market. This modular design approach of AraMiS-C1 makes the redesign convenient by the reuse of similar modules [10, 11].

The current version of CubeTCT consists of an S-band subsystem. In the future, the CubeTCT design will also incorporate a UHF subsystem. The regulator/sensor module and interface components required by CubeTCT have been implemented on the same communication tile as shown in Figure 8. From here onwards, CubeTCT will refer to the current version which only contains an S-band subsystem.
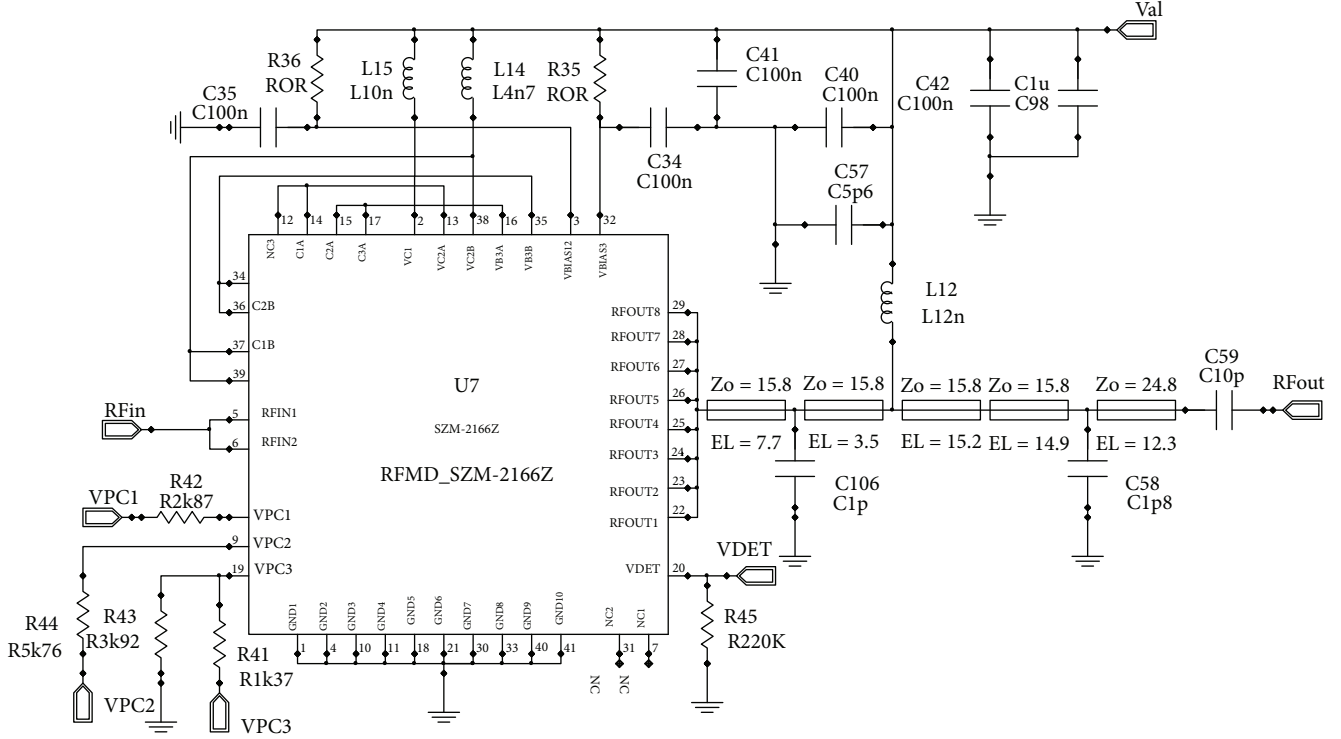
Figure 6: Schematic of power amplifier (SZM-2166Z).

Table 1: Mapping of CC2510 pins onto the AraMiS module.

Connector	Pin	A	B
D0/RX/SOMI	11	P0.2	P1.7
D1/TX/SIMO	9	P0.3	P1.6
D2/SCL/SOMI	7	P2.0	P2.0
D3/SDA/SIMO	5	—	—
D4/CLK	3	P0.5	P1.5
D5/PWM	1	P1.2	P1.1
D6/A0	12	P0.0	P0.6
D7/A1	10	P0.1	P0.7
D8/ID/INT	4	P0.4	P1.0
D9/EN/PWM2/INT	2	P1.3	P1.4

CubeTCT is a four-layered PCB with dimensions of 98.0 mm × 98.0 mm × 1.55 mm. All of these components are mounted on the bottom layer (layer 4), while the top layer (layer 1) contains a feed point for mounting a detachable S-band patch antenna (2.4 GHz). The routing for RF, power, and other analog traces are performed on the bottom surface. All the digital traces are routed on the third layer. The second and fourth layers are ground planes which help in shielding RF, power, and analog traces from digital signals. Therefore,this ensures having a considerably better signal integrity. The 1B9_CubeTCT communicates with an onboard computer (OBC) through a 6-pin SPI connector. A Power Distribution Bus (PDB) is made available using a separate 4-pin connector. Two 8-pin connectors are available for separate programming and debugging of the Texas Instruments CC2510 transmitter Tx and receiver Rx. The data processing, monitoring, and various control operations for 1B9_CubeTCT is also performed by these commercially available transceivers which has an internal 8051 core microcontroller [12].

The main focus for the CubeTCT design is to realize a high-bandwidth communication link using low-cost COTS components which are available in the market. This has made it feasible for the universities and small industries to enter the field of satellite design. Moreover, a modular architecture approach has been employed for complete nanosatellite design. This modular approach makes the redesign convenient by the reuse of the identical modules.

To ensure a consistent communication radio link, CubeTCT has been designed as a separate subsystem from a satellite standpoint. It can communicate with other subsystems and the "On Board Computer" (OBC) via an SPI interface. CubeTCT draws power from an onboard Power Management System (EMS) via a Power Distribution Bus (PDB). Power regulation is performed by the CubeTCT Power Regulation module. There are three power regulators that provide voltage levels of 6 V, 3.3 V, and 3 V Ref on CubeTCT. An antilatchup protection system is there to protect CMOS circuitry against radiation hazards. Real-time monitoring of voltage, current, and temperature is also performed by voltage, current, and temperature sensors on CubeTCT to ensure proper functionality and housekeeping.

1B9_CubeTCT communicates with OBC and other modules using the SPI interface of the Rx. The Rx is always periodically sniffing for a radio packet from the ground
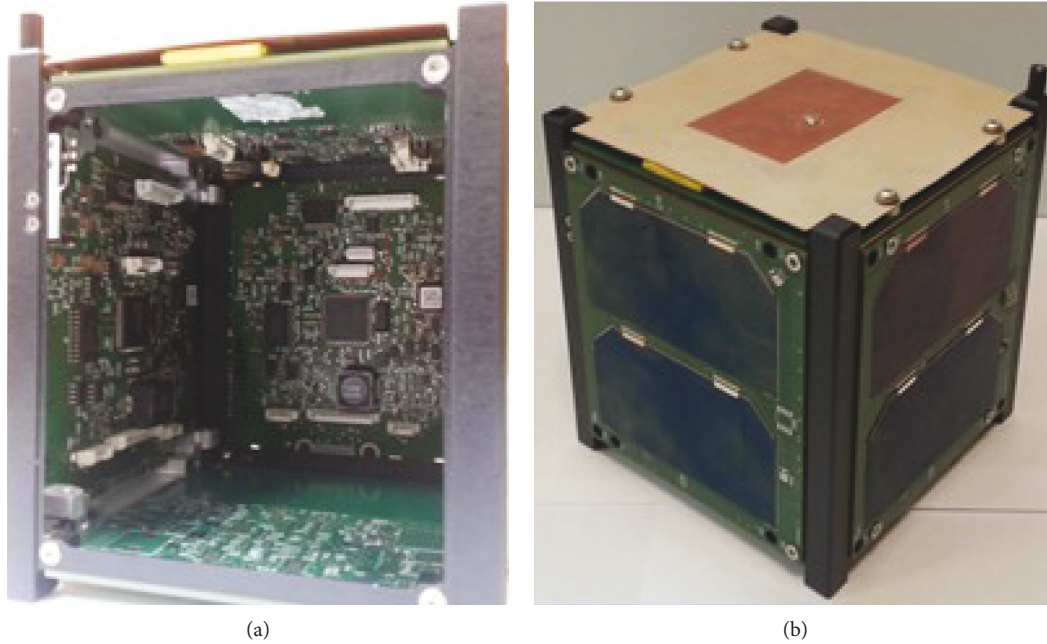
(a)

(b)

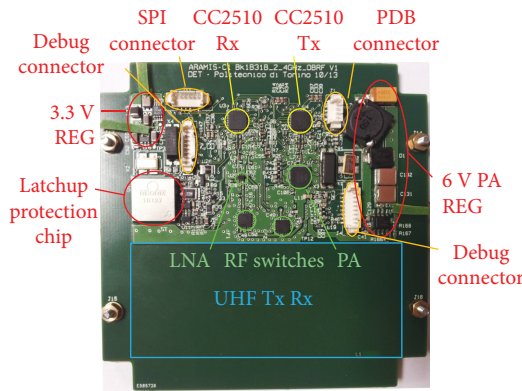FIGURE 7: Photograph of AraMiS-C1 with 4 CubePMT and 2 CubeTCT tiles.

FIGURE 8: Photograph of CubeTCT.

FIGURE 9: Block view of the S-band 1B9_CubeTCT system.

station. In this case, when a packet is received by Rx, it performs a CRC check and FEC. The received packet is decapsulated and sent to OBC. For transmission, OBC forwards data to Tx which is encapsulated and transmitted to the ground station. Besides performing radio communication, the CubeTCT transceiver also performs various status monitoring and control tasks. Different sensors (temperature, voltage, and current sensors), PA, and antilatchup circuits are monitored by these transceivers via analog and digital I/O ports. The PA load switch, regulators (3 V Ref, 3.3 V, and 6 V), PA, and RF switches are also controlled by Tx and Rx as shown in Figure 9.

Most efforts to use COTS components in the space environment are aimed to protect the CMOS circuits against fatal events such as a latchup due to radiation hazards. To protect against such events, a commercial antilatchup circuit component is being used on CubeTCT
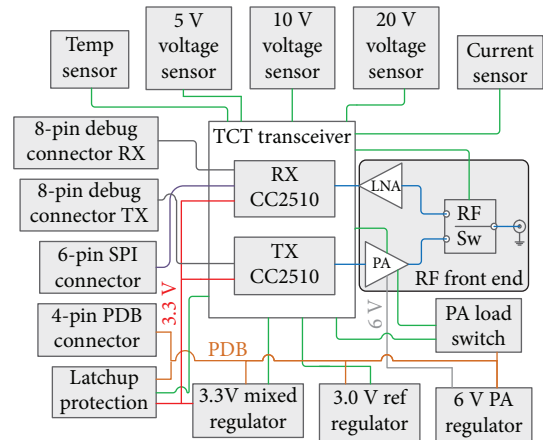
which isolates power to the load for a finite time to ensure that a latchup is extinguished [13].

The main subsystems of CubeTCT include:

(i) CubeTCT transceiver

(ii) CubeTCT power regulator and load switch

(iii) Housekeeping sensors

(iv) 1B9_CubeTCT antilatchup protection

(v) CubeTCT RF front end

3.1. RF Front End. The RF front end is the most important subsystem of the CubeTCT tile. In the transmit chain, it is composed of the transmitting CC2510 RF matching network
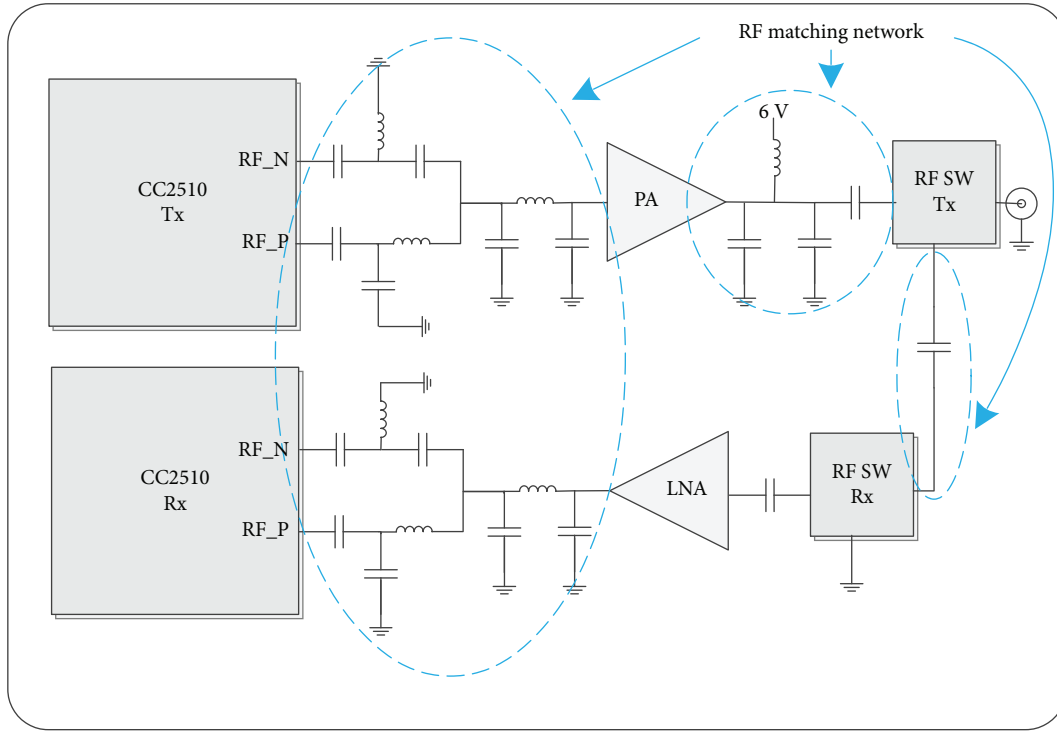
Figure 10: RF front-end block diagram.

and a power amplifier that connects to the (external) patch antenna using two RF switches. The receive chain starts from the antenna that is connected through two RF switches to the LNA that further connects to the receiving CC2510 via the RF matching network as depicted in Figure 10. This is a half-duplex system using the same antenna for transmitting and receiving. The receiver and transmitter chains are isolated together using two RF switches. The concept behind using two RF switches is to provide a better isolation to the LNA.

The matching network of CC2510 has been designed in a symmetric fashion to avoid any delays and lags. The RF front end consists of COTS components which have been selected according to certain design requirements. The LNA, PA, and RF switches were tested individually for compliance. The passive components used in the overall design of the matching network are chosen on the basis of the least parasitic behaviour and to ensure optimum matching (according to the manufacturer's specifications).

3.1.1. RF Front-End Design. This section provides a more detailed designed description of the major modules constituting the RF front end which includes LNA, PA, and RF switches and the RF matching network. The RF front end is designed with focus on low cost and use of commercially available components which make them comparable to other such subsytem approaches [14].

3.1.2. LNA Design. The communication data rate attained by using CC2510 is 500 kbps. The corresponding sensitivity was observed to be -85 dBm for the given data rate. Therefore, it was necessary to use a low-noise amplifier (LNA) to mitigate

the noise power from the received signal. The purpose of using LNA was to provide a high gain and the least possible noise figure (NF). For LNA design, different COTS components were analysed on the basis of gain and NF.

Among them, the Maxim MAX2644 was selected as the best suitable option because it provides a maximum gain of up to 17 dB and a NF of 2.2 dB (at 2.43 GHz). It can be used in two different configurations. First, it can be used as a high-gain option, one that is not very linear, so it has a value of IIP3 equal to -3 dBm. The second allows for a gain of 16 dB and an IIP3 of 1 dBm which has been chosen for our design, as shown in Figure 5. A length of 10.16 mm has been added between the bypass capacitors C_{62} and C_{61} to mitigate 3.3 V supply noises to the LNA [15].

3.1.3. PA Design. The power amplifier (RFMD SZM-2166Z) selected is a COTS component. It is a high-linearity class AB power amplifier that is designed using HBT (Heterojunction Bipolar Transistor) technology with both InGaP and GaAs semiconductor devices which are used in high-frequency RF design (suitable for the space environment). The power amplifier provides an output RF power of 33 dBm and a gain of 36 dB. This power amplifier incorporates an active bias circuit which provides designers the flexibility to optimize performance in specific applications as shown in Figure 6. There is a power detector and a power-enabling signal available for its control and monitoring. In our case, a power of 2 W is consumed by PA. A voltage regulator downconverts the Power Distribution Bus into 6 V which then drives this PA.

The PA separate module was also tested for actual output power by connecting CC2510 at the input power which

provided a maximum power of 36 dBm at 2.43 GHz. The input power was varied and the correspondent output power values are reported as in Table 2.

Using these measured values, the gain (GdB) and efficiency (η) were calculated as follows:

$$GdB = P_{out}dBm - P_{in}dBm, \tag{1}$$

$$\eta = \frac{P_{out}}{P_{al}}, \tag{2}$$

where

$$P_{al} = VI. \tag{3}$$

Figure 11 describes the measured gain of the PA which is acceptable for 1B9_CubeTCT. The efficiency is also reported in Figure 12, which seems to agree with the manufacturer's values reported in [16].

3.1.4. RF Switch Design. The RF switches designed for the RF front end uses two COTS components from TriQuint (TQP4M0010). These are high-absorption GaAs SPDT switches that provide the most suitable results among the other contenders. Each switch can sustain a maximum input power of 36 dBm and provides an isolation of 45 dB between each RF port with an insertion loss of 0.9 dB at 2.43 GHz [17].

The RF switch operates on 3.3 V and both of them are controlled by the enabling control signals V_c from the transceiver core as shown in Figure 13(a). When V_c is low, RF_C and RF_1 are connected, whereas RF_C and RF_2 are isolated, or in other words, the receive chain is enabled. On the contrary, if V_c is high, RF_C and RF_2 are connected while RF_C and RF_1 are isolated; therefore, the transmit chain is enabled as shown in Figure 13(b). Here, a precautionary measure is mandatory to ensure that the power amplifier is only enabled once the transmit chain is enabled to avoid high power dissipation within the RF switch which can cause physical damage.

3.1.5. RF Matching Network Design. The telecommunication tile has been realized on a 4-layer PCB. The RF traces have been placed on the topmost layer. The RF front-end network has been designed on an enhanced FR-4 substrate with a dielectric constant (ε_r) of 4.7 and height (h) of 0.36 mm with an operating frequency of 2.43 GHz as shown in Figure 14. This increases the need for a proper RF matching network to yield acceptable results. Thus, all the selected RF COTS components were closely analyzed and a matching network was designed for each of them in close compliance with the manufacturer's specifications and design requirements. The matching impedances for CC2510 chips' RF front end, PA, LNA, and switches were transformed into equivalent trace widths along with electrical lengths into physical lengths using the AWR microwave office Tx-line tool [18].

TABLE 2: PA, input vs. output power, and output current.

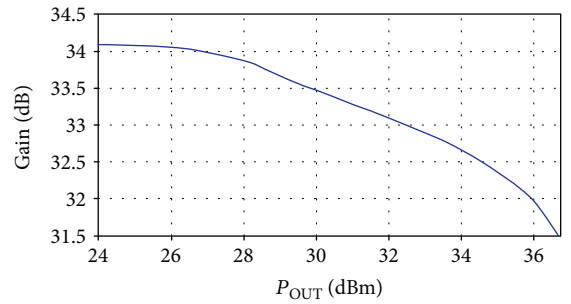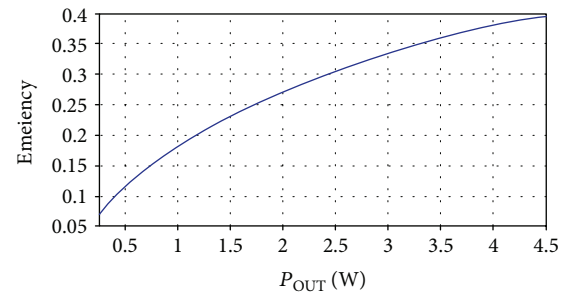| P_{in} (dBm)	P_{out} (dBm)	I_{out} (A)
-10.0	24.1	0.606
-9.0	25.1	0.63
-8.0	26.05	0.66
-7.0	27.0	0.70
-6.0	27.9	0.75
-5.3	28.5	0.79
-4.2	29.38	0.855
-3.2	30.25	0.931
-2.1	31.14	1.01
-1.1	32.0	1.11
0.0	32.9	1.2
1.0	33.74	1.33
2.1	34.6	1.46
3.0	35.3	1.6
4.0	36.0	1.75
5.0	36.55	1.9

FIGURE 11: Measured gain of PA (SZM-2166Z).

FIGURE 12: Efficiency of PA (SZM-2166Z).

The matching impedances used in the given design are tabulated with their equivalent trace width (W) in Table 3.

4. Conclusion

The paper presents a modular approach for a RF front-end design by using COTS components that are low priced and readily available for development. This makes the design
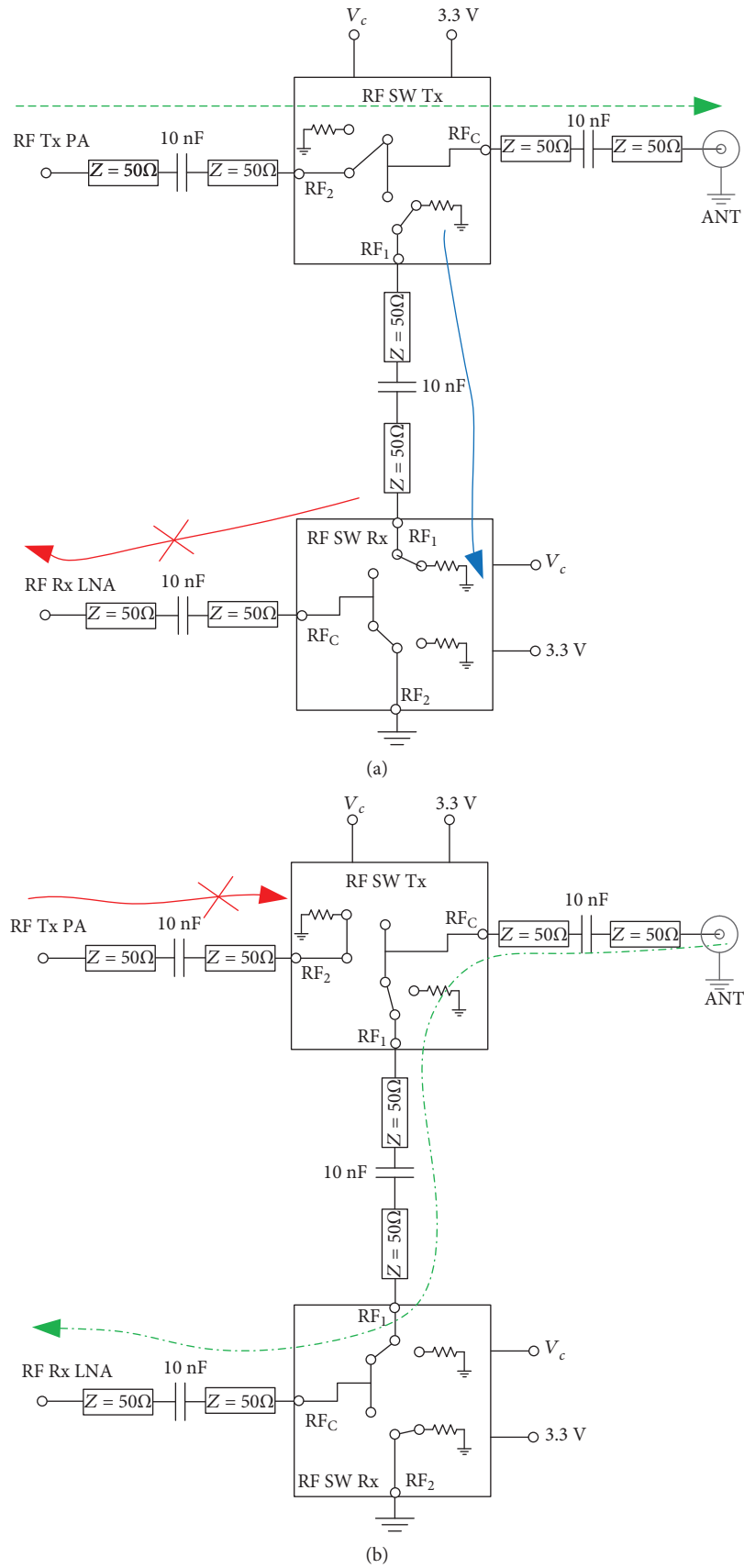
FIGURE 13: RF switches: (a) transmit mode with V_c = low and (b) receiving mode with V_c = high.
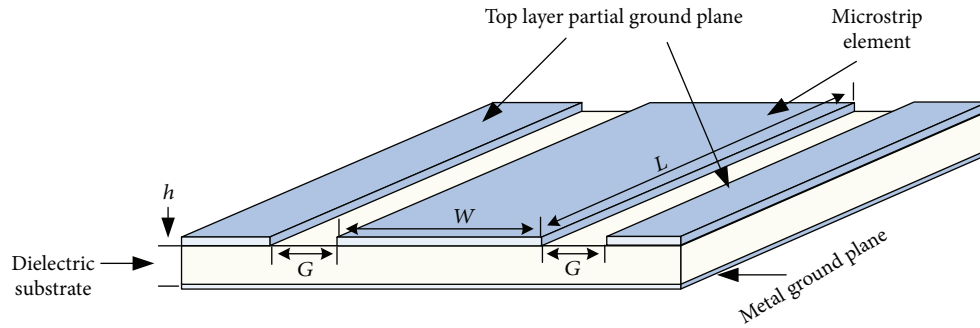
Figure 14: Telecom tile PCB layout; top 2 layers.

Table 3: Computed trace widths with AWR Tx-line tool for RF front-end matching.

Impedance, Z_0 (Ω)	Trace width, W (mm)
15.8	3.17
24.8	1.71
50	0.6
80	0.12
95	0.10

more feasible for small industries and academia to develop their own satellite subsystems. Moreover, there is a degree of modularity at the design, schematic, and physical levels which can significantly reduce the subsystem manufacturing and design cost and development time.

Data Availability

The abovementioned work is the authors' intellectual property and research work. All the data needed to support the research work is available.

Disclosure

An earlier version of this study was presented as an abstract at the 65th International Astronautical Congress 2014.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] J. Bouwmeester and J. Guo, "Survey of worldwide pico- and nanosatellite missions, distributions and subsystem technology," *Acta Astronautica*, vol. 67, no. 7-8, pp. 854–862, 2010.

[2] O. Popescu, J. S. Harris, and D. C. Popescu, "Designing the communication sub-system for nanosatellite CubeSat missions: operational and implementation perspectives," in *SoutheastCon 2016*, pp. 1–5, Norfolk, VA, USA, 2016.

[3] "Guest editorial. Satellite communications and antennas," *IET Communications*, vol. 12, no. 1, pp. 1–1, 2018.

[4] S. Speretta, L. M. Reyneri, C. Sanso'e, M. Tranchero, C. Passerone, and D. D. Corso, "Modular architecture for satellites," in *58th International Astronautical Congress*, pp. 24–28, Hyderabad, India, September 2007.

[5] D. Wood and A. Weigel, "Architectures of small satellite programs in developing countries," *Acta Astronautica*, vol. 97, pp. 109–121, 2014.

[6] M. R. Mughal, A. Ali, and L. M. Reyneri, "Plug-and-play design approach to smart harness for modular small satellites," *Acta Astronautica*, vol. 94, no. 2, pp. 754–764, 2014.

[7] "UML tutorial," http://www.tutorialspoint.com/uml/index.htm.

[8] M. R. Mughal, L. M. Reyneri, and A. Ali, "UML based design methodology for serial data handling system of nanosatellites," in *2012 IEEE First AESS European Conference on Satellite Telecommunications (ESTEL)*, pp. 1–6, Rome, Italy, 2012.

[9] M. R. Mughal, A. Ali, H. Ali, and L. M. Reyneri, "Smart honeycomb tile for small satellites," in *2014 IEEE Aerospace Conference*, pp. 1–8, Big Sky, MT, USA, 2014.

[10] A. Ali, L. M. Reyneri, H. Ali, and M. Rizwan Mughal, "Components selection for a simple boost converter on the basis of power loss analysis," in *63rd International Astronautical Congress*, pp. 1–5, Naples, Italy, October 2012.

[11] A. Ali, M. R. Mughal, H. Ali, and L. Reyneri, "Innovative power management, attitude determination and control tile for CubeSat standard nano-satellites," *Acta Astronautica*, vol. 96, pp. 116–127, 2014.

[12] "CC2510, datasheet," http://www.ti.com/lit/ds/symlink/cc2510.pdf.

[13] "1B127, datasheet," http://ptc.partcommunity.com/3d-cad-models/FileService/File/tpa/neohm/pdf/1b127.pdf.

[14] Y. Wang and R. Shi, "Low cost and convenient design for receiver front-end," in *2016 CIE International Conference on Radar (RADAR)*, pp. 1–4, Guangzhou, China, 2016.

[15] "Maxim-2644, datasheet," http://datasheets.maximintegrated.com/en/ds/MAX2644.pdf.

[16] "RFMD SZM-2166Z datasheet," https://www.qorvo.com/products/d/da001999.

[17] "TriQuint TQP4M0010 datasheet," http://www.triquint.com/products/p/TQP4M0010.

[18] "Tx-line tool AWR microwave Office," https://www.awrcorp.com/products/additional-products/tx-line-transmission-line-calculator.