Experimentally validated methodology for real-time temperature cycle tracking in SiC power modules

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Abstract

The ability to monitor temperature variations during the actual operation of power modules is key to reliability investigations and the development of lifetime prediction strategies. This paper proposes an original solution, specifically devised with novel fast-switching silicon carbide (SiC) power MOSFETs in mind. The results show ability to track temperature variations resulting from active power cycling of the devices, including high speed transients, thus enabling to discriminate among different potential failure mechanisms. Validation of the proposed methodology and its accuracy is carried out with the support of infrared thermography.

1. Introduction

Wide-bandgap semiconductors such as SiC MOSFETs have been developed over two decades ago. However, for many years their application has been extremely limited due to high cost and unsolved reliability problems. SiC-based devices present numerous advantages if compared to the classical Silicon- (Si-) based devices, such as lower conduction and switching losses, and high breakdown voltage and operating temperature. Only recently, semiconductor manufacturers started to introduce the first commercial SiC MOSFETs power modules for industrial applications [1]. The tremendous increasing of the power density of such devices conjoint to an extremely low thermal inertia, requires an accurate thermal management. As the failure rate of power semiconductors is closely related to their junction temperature during operations, it is mandatory not to exceed the maximum allowable junction temperature even for a very short time. Different techniques to estimate or measure the junction temperature have been developed, for Si- and SiC-based components, like the ones presented in [2], [3] and [4].

TSEPs (Temperature Sensitive Electrical Parameters) techniques are widely used to estimate the junction temperature of wide bandgap semiconductors, however most of them are not suitable to be implemented in a commercial converter.

In [5] there is a comparison between different TSEPs techniques.

The main TSEPs are:

1. The temperature dependency of the gate threshold voltage.
2. The temperature dependency of the transconductance.
3. The temperature dependency of the current commutation.
4. The temperature dependency of source-drain reverse bias voltage when V_{GS}=0.
5. The temperature and current dependency of the voltage-drop of the power device when it is ON.

The first three TSEPs present a good temperature sensitivity and according to [5], “the temperature dependency of the gate threshold voltage” is one of the best parameters in terms of temperature sensitivity. However, the first three solutions are hardly implementable in a commercial power converter, because they are required to measure voltages and currents in very short timescales. Usually in SiC MOSFETs commutations are in the order of 100 ns (sometimes less depending on the size of the

component), this means that the acquisition system should have a bandwidth comparable to that of an oscilloscope. Furthermore, in a real application multiple switches are commutating simultaneously, this means that the measurement system should be able to reject the noise due to the other sources. A measurement system with such characteristics is technologically hard to implement and not economically justifiable. TSEP number 4 is one of the most used, however it requires the injection of a calibrated bias current. This solution is not feasible in a classical two-level converter working with a PWM modulation. It is not possible to inject a bias current between the source and the drain while the MOSFET is in interdiction state, because during the OFF state, the MOSFET is subject to the full DC-link voltage. The solution number 5 requires the measurement of the current flowing through the device and the voltage drop when the device is in conduction state. This measurement is not critical and can be done during the conduction time of the switch. In the case of a classical two-level converter working with a PWM modulation and using a triangular carrier, one of the vertexes of the triangle can be used as a sampling time reference, so that is possible to ensure that no commutation is occurring during the sampling time. All the presented techniques require that the device under test is previously calibrated to find the relationships between the TSEP and the temperature. In a laboratory environment the calibration process can be carried out with the use of dedicated equipment like curve tracers and hotplates, however this is not a feasible solution for industrial power converters. The proposed solution starting from the well-known dependency of the V_{ON} with the temperature, provides also a robust low-cost measurement system and a commissioning test that can be run directly on the final application.

This paper presents the **validation** of a technique for the indirect junction temperature estimation via on-state voltage measurement, applicable to all types of PWM commanded power converters. This on-line estimation method was proposed in [6]. The junction temperature is estimated at every PWM period by a temperature LOOK-UP TABLE (LUT) whose inputs are the ON voltage and current of the power switch under observation.

The strengths of the proposed method deal with its simplicity (off the shelf low cost hardware), accuracy and fast dynamic response. In turn:

- The converter commissioning does not need dedicated equipment like a curve tracer: it can be performed directly on the final application.
- Hardware modification respect to a "classical converter" are minor and non-costly.
- Temperature detection does not affect the converter operation with either noise injection or additional parasitics.
- Temperature detection has a fast-dynamic response.

2. Real-time temperature estimate

The device under test is labelled SW1L in Fig. 1 and it is part of a custom build power module connected in H-bridge configuration. The quantities in red are the ones sampled at each PWM period. The prototype converter built to validate the proposed method is depicted in Fig. 2. The MOSFETs inside the power module under test have a rated current of 20 A (T_{sink}=80°C). A detailed description of hardware needed to measure the V_{ON} can be found in [7].

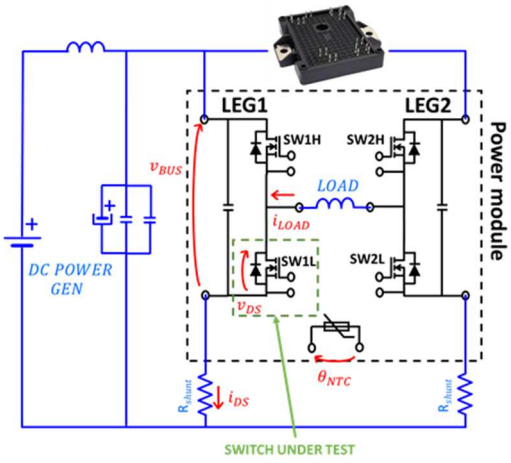


Fig. 1: Schematic diagram of the proposed setup: red quantities are measured at each PWM period.

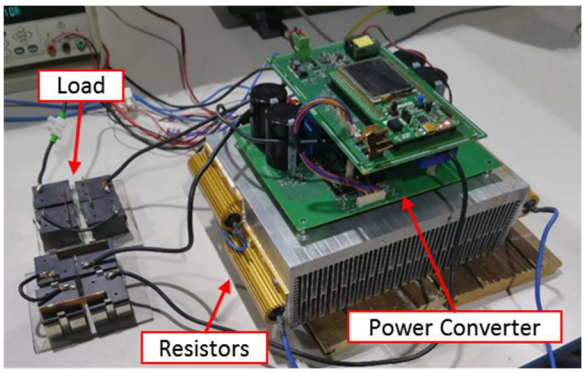


Fig. 2: Picture of the proposed test setup.

A dedicated commissioning test is preliminarily

run to build the look-up-table $\theta_J(i_{DS}, V_{ON})$. The heatsink is preliminarily heated up to 145 °C with the use of two external resistors, then the resistors are shut off and the heatsink is left to cool naturally. While the heatsink is cooling a series of current pulses of short duration from 1A to 28 A are imposed to the load (and to the switch SWL1). The short duration of the current pulses ensures that the temperature of the junction equal the temperature DBC (that can be measured with the embedded NTC thermistor). Every time that the temperature of the heatsink drops by a value of 5°C degree a new set of current pulses is imposed. Fig. 3 shows the data acquired during the pulse test. Afterward the data obtained from the pulse test are interpolated and the LUT $\theta_J(i_{DS}, V_{ON})$ can be obtained. A detailed description of the commissioning test can be found in [7].

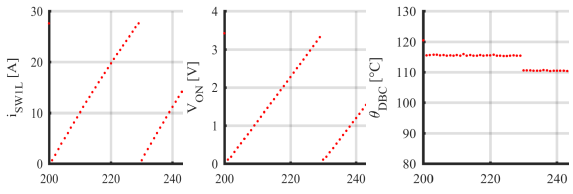


Fig. 3: Pulse current test

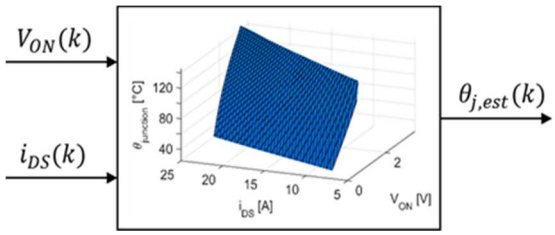


Fig. 4: Functional block for the online temperature measurement

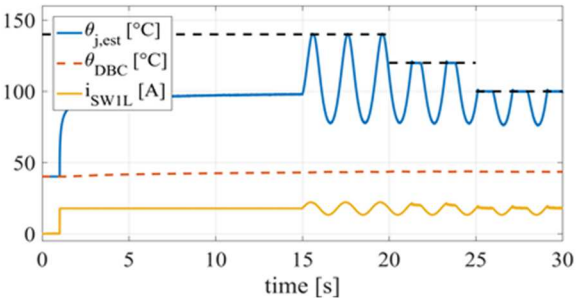
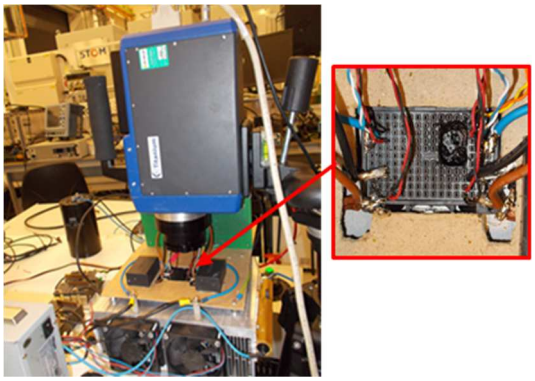


Fig. 5: Estimation and limitation of the junction temperature.

The obtained LUT is used for on-line estimation of the junction temperature according to the functional block shown in Fig. 4. Fig. 5 shows a test where the junction temperature is online estimated and actively limited through current limitation. The orange line is the load current, which is related to the current of SW1L according to the duty-cycle of LEG1 of the converter, while the blue line is the estimated junction temperature using the proposed method. The black dashed line represents the accepted temperature limit: if the monitored temperature reaches such threshold, the load current is closed-loop limited. It is possible to notice that when the maximum junction temperature limit is lowered from 140°C to 120°C and then to 100°C, the junction temperature is exactly clamped to the limit. The clamping of the current waveform (yellow) is also visible. A simple PI regulator was used in this test to limit maximum temperature in closed loop. More sophisticated techniques can be adopted, like the ones presented in [8] and [9]. This family of techniques allow for active control of the junction temperature and makes it possible to reduce the thermal transients in power electronic modules. The dotted red line in Fig. 5 represents the temperature measured by the thermistor embedded in the module which is a measure of the DBC (Direct bonded copper) temperature. In most of applications, this is the temperature feedback used for thermal protection of the module. This test shows that the distance between junction and DBC temperature is high (up to 140 – 40 = 100°C) and variable. The module thermistor is neither viable for full exploitation of the power module nor for safety against overtemperature.

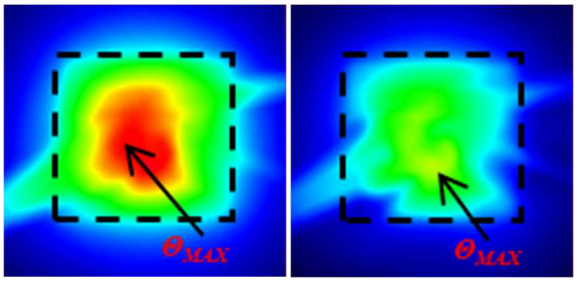
3. Validation of the methodology with IR thermography

The proposed methodology has been validated with the use of the thermal camera showed in Fig. 5. The thermal camera used is the CEDIP Titanium camera which is capable of taking high temperature pictures using infrared technology. The module gel filling has been removed and the layout of the converter has been appropriately modified as showed in Fig. 6 to permit visual access to the die inside the module. Following the gel removal, the tests have been performed at reduced voltage to avoid the voltage breakdown of the component.



a) **b)**

Fig. 6: a) Test rig with modified layout and thermal camera. b) Zoom of the test setup showing the device under test



a) **b)**

Fig. 7: Thermal image of the switch SW1L, the black dotted line represents the area of the chip a) heating phase b) cooling phase

Fig. 7 shows the infrared image of the switch under test when the converter is working under PWM conditions. Although the dimensions of the die are modest (3.1 mm x 3.36 mm), the temperature gradient is anything but negligible. For example, in Fig. 7 a) the temperature gradient between the borders of the chip and the center is around 35 °C. It is possible to notice that the bonding wires that are connected between the die and the DBC, help to extract the heating from the center of the die, causing an even more irregular temperature distribution. During the cooling phase of the die shown in Fig. 7 b), the temperature distribution is also quite irregular.

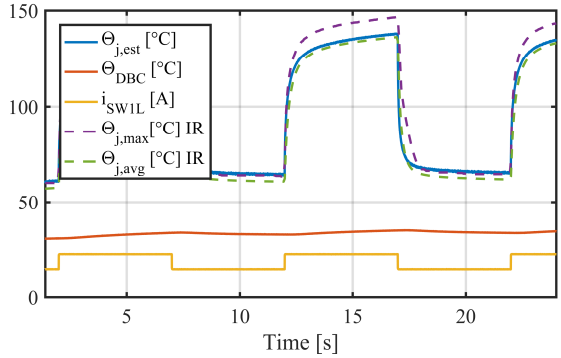


Fig. 8: Validation with IR camera: comparison estimated temperature (blue) and measured temperature (dashed). Maximum and average measurements are reported.

Fig. 8 shows the comparison between the estimated junction temperature and the temperature measured with the thermal camera. The dashed purple line represents the maximum temperature measured across the chip (hotspot), while the green dotted line is the average temperature of the chip. The difference between average and maximum temperature is significant, especially when the temperature is high. In these working conditions, such difference can reach 12°C. The estimated temperature has a good matching when compared with the average temperature of the chip. Time wise, the hotspot curve (purple dashed) has a slow tail when passing from the high level to the low level at the step down of the load current. This is also visible in Fig. 7b in the form of “persisting” hotspots during the cooling phase of the chip. It must be remarked that the hotspot is not a single physical point on the chip, but the point at the highest temperature in each timeframe.

4. Dynamic response

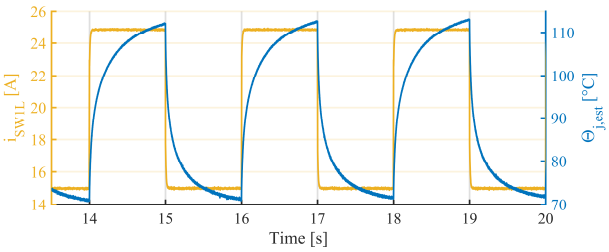


Fig. 9: Current square wave temperature estimation.

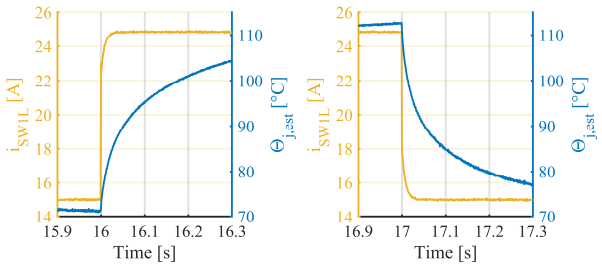


Fig. 10: Detail of Fig. 9. Left: heating phase. Right: cooling phase.

Fig. 9 shows a current step test where the LEG1 of the H-bridge power module is working with a fixed duty cycle equal to 0.5, while the duty cycle of the LEG2 is variable so to impose the load current. The switch under test SWL1 is in conduction for 50% of the period. Fig. 10 is the zoom of Fig. 9, showing a close-up of the thermal transients for the heating and cooling phases. In this example, the converter is working at 10 kHz and the junction temperature is updated every 100 µs. The results show that is possible to track temperatures variations resulting from active power cycling of the device, including high speed thermal transients. The thermal transient analysis can be used for the thermal characterization of the power module, allowing to discriminate between different potential failure mechanism. According to [10] and [11], the thermal impedance can be derived from the cooling curve of the component. Subsequently, the Foster and Cauer thermal models of the power module can be computed using mathematical transformations. Performing this measurement directly on the final application enables the collection of precious information on the power modules and the whole converter system. For example, from the Cauer thermal model it is possible to spot a bad thermal connection between the power module and the heatsink which could have occurred due to a bad assembly while building the converter.

5. Ageing

Although, SiC chips have superior electrical and thermal proprieties when compared to Silicon chips, currently available commercial SiC MOSFETs modules are also made up of multi-layered materials with different thermal expansion coefficients [12] like Silicon modules. The useful life of semiconductor is strongly influenced by the thermal cycling that it undergoes in the course of its operation. Due to the aging of the component, there is an increase in the R_{ON} value which in turn will affect the real junction temperature and its estimation. The junction temperature tends to be overestimated, and if an active temperature control is being used the current will be over-limited and the converter will tend to underperform. Following the aging of the component, the user can accept the derating of the component to increase its useful life, or run a new commissioning test and obtain a new LUT for the estimator. It is good to emphasize that the R_{ON} increase of a SiC MOSFET due to ageing is relatively low when compared to that of a classical Si IGBT. The same power module under test in this work has been aged in [13] using a highly accelerated power cycling test platform and the R_{ON} increase has been evaluated.

6. Conclusions

The presented methodology can be integrated into a commercial power converter with little extra complication, provided that the V_{ON} measurement is embedded inside the gate drivers. The proposed method has been validated against the results from an infrared thermal camera and proven to be able to estimate correctly the average temperature of the die, with high accuracy and fast dynamic response. However, it is important to take a margin between the estimated average temperature and the presumed hotspot value, to guarantee operation within the safe operating area of the device. The capability to measure high speed thermal transients, allows to distinguish between different potential failure mechanisms. During the tests, the modulation frequency was set to 10 kHz. This allows to obtain one temperature estimation every 100 µs. The same measurement system has been tested up to 80 kHz, this means that is possible to obtain one temperature estimation every 12.5 µs. In the future, the method will be validated for SiC MOSFETs with a bigger die size, where it is reasonable to expect a more marked temperature gradient.

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