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Coordinated On-line Junction Temperature Estimation and Prognostic of SiC Power Modules / Stella, F., Pellegrino, G., Armando, E.G.. - ELETTRONICO. - (2018), pp. 1907-1913. (IEEE Energy Conversion Congress and Exposition (ECCE 2018) Portland (USA) September 23 – 27, 2018) [10.1109/ECCE.2018.8557850].

Availability:
This version is available at: 11583/2713892 since: 2020-11-18T22:13:15Z

Publisher:
IEEE

Published
DOI:10.1109/ECCE.2018.8557850

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12 October 2026

Coordinated On-line Junction Temperature Estimation and Prognostic of SiC Power Modules

Fausto Stella
Dipartimento Energia, "G. Ferraris"
Politecnico di Torino
Torino, Italy
fausto.stella@polito.it

Gianmario Pellegrino
Dipartimento Energia, "G. Ferraris"
Politecnico di Torino
Torino, Italy
gianmario.pellegrino@polito.it

Eric Armando
Dipartimento Energia, "G. Ferraris"
Politecnico di Torino
Torino, Italy
eric.armando@polito.it

***Abstract*— The long-term reliability of power modules is a key factor for most of power electronics applications. Previous work was dedicated to the online monitoring of junction temperature of SiC power MOSFETs via on-state resistance measurement. Among several advantages, temperature monitoring avoids the components failure due to instantaneous thermal overstress. Moreover, as the on resistance tends to grow with the age of the component, temperature monitoring inherently behaves as a precursor of failure, because temperature will be overestimated progressively throughout the lifetime of the component. In this paper the systematic detection of aging of the power semiconductors is proposed, still using the direct measurement of the on-state resistance. A new joint methodology is proposed, based on the initial commissioning of the module both for temperature monitoring and aging evaluation. The identification and monitoring technique is tested on a SiC MOSFET power module.**

Keywords—on-resistance, forward voltage, SiC power MOSFET, prognostics, aging, junction temperature monitoring, TSEP.

I. INTRODUCTION

Power modules reliability is of paramount importance for the long-term reliability of power conversion systems and actuators [1]. The adoption of power electronic converters has been growing tremendously in automotive and energy conversion, as well as in aviation and medical applications. In all such fields the downtime due to failure must be avoided for cost reasons and - or for aspects related to safety. Fig. 1 shows that semiconductors are among the weakest parts of modern power converters. In turn, while most of performance targets of power converters such as efficiency and compactness are within reach, a lot of work is still to be done concerning their reliability [2].

Different failure mechanisms can occur in a power module, for instance: bond wire fatigue, chip cracking, delamination at the interface between mold and copper and solder fatigue. The failure rate of power semiconductors is closely related to their junction temperature during operations, which is known very approximately. In most of cases a temperature sensor is placed within the power module, giving a very rough underestimate of the devices temperature. Besides the maximum instantaneous junction temperature, also thermal cycling tends to stress the component and reduce its lifetime in the long term. The ability to periodically monitor health status of the devices can be crucial to improve the long-term reliability of the converter and therefore of the whole system. Prognostics can be used to schedule a maintenance before a catastrophic breakdown occurs.

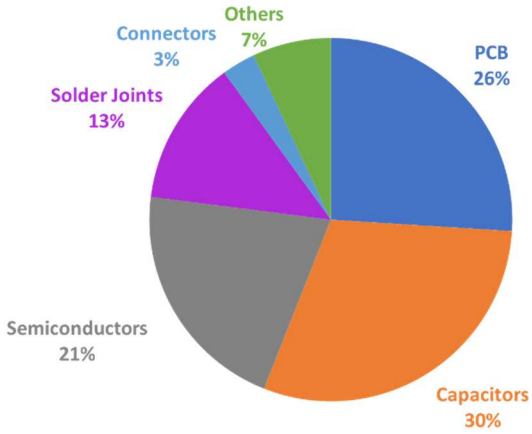

Fig. 1. Failure distribution among major components [3].

According to the literature, health monitoring techniques can be split in three main families [5] - [6]:

1. Model-based techniques.
2. Techniques that requires dedicated sensors embedded in the device.
3. Indirect techniques based on the monitoring of electrical parameters or based on the evaluation of thermal resistance networks.

The first family of techniques requires an intimate knowledge of the physical structure of the power device. This permits to build an **electrothermal model** for estimating the temperature during the load cycles [7], and a **thermomechanical model** for estimating the mechanical stress across the device due to temperature variations [8]. So far, model-based techniques lack accuracy. Moreover, the tests needed to identify the model parameters are complex and require a set of dedicated laboratory equipment.

The second family of techniques requires the use of dedicated sensors embedded in the device: this can be costly and can perturbate the operating conditions of the device. In turn, inserting a sensor inside a power module can significantly affect its reliability.

Regarding the indirect techniques, gate threshold voltage and on-state resistance are universally accepted as reliable aging precursors. Moreover, other less conventional parameters of the semiconductor can be used as health indicators, like parasitic capacitances, gate voltage waveforms, switching waveforms [9] and thermal resistances within the module. This third family of techniques is normally preferred in a laboratory environment with dedicated measurement equipment and controlled testing conditions,

and it is hardly replicable for online evaluation of the device state of health.

This paper presents a methodology for instantaneous estimate of junction temperature and aging of SiC MOSFETs in a power module, using the online measurement of the V_{ON} of one of the devices of the module. Using the on-state voltage of the component for estimating the junction temperature and the aging are well known methodologies in the literature [1], [4], [6], [9]-[11]. The paper illustrates a simple identification and monitoring methodology that is applicable to any kind of power converter directly in-line, without dedicated laboratory hardware or complicated data manipulation. The junction temperature lookup table and one additional R_{ON} curve called **15A-commissioining** in this example are identified at the beginning of the life of the module and then used for junction temperature and age estimation, respectively. Experimental results are presented for SiC MOSFET module rated 19 A, 1200 V, before and after 15,000 thermal cycles.

II. TEST BED

The power section of the proposed setup is reported in Fig. 2. The custom Emipak 2B power module Fig. 3 is connected in H-bridge configuration, supplying a purely inductive load. This mimics realistic operating conditions, while absorbing a fraction of the converted power. The power module is monitored electrically and thermally: Fig. 2 shows the electrical quantities that are sampled from the microcontroller at each PWM period. The load current is closed loop controlled by one leg of the module (LEG2), to impose the test current level. The other leg (LEG1) is open-loop controlled at a fixed duty-cycle, to mimic a constant voltage source or load (depending on the current direction). The 2-leg module (Fig. 3) has two embedded capacitors (green rectangles), to minimize the stray inductance of the power loop, and one embedded NTC thermistor, used for measurement of the DBC (direct bonded copper) temperature. Table 1 reports the ratings of the power module under test.

Table 1- Ratings of the power module

Data from datasheet	
Rated Current (heatsink @ 80°C)	19 A
Breakdown voltage	1200 V
Max Junction Temperature	175°C
R_{ON} @ 25°C, 20 A	78 mΩ
Embedded dc-link capacitors	2 x 47 nF

Although different modules from different manufacturers where tested, this paper will refer to one manufacturer and one size only, for brevity reasons. The setup depicted in Fig. 5 consists of one control board on top, one power board placed on a heatsink and two gate driver boards in between. The custom hardware is based on off-the-shelf components and an industrial microcontroller. Four external resistors (visible in Fig. 5) placed at the sides of the heatsink are used for heating the baseplate of the module when necessary. A detailed description of the hardware can be found in [15].

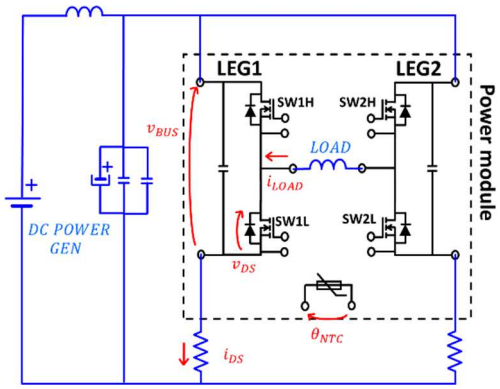

Fig. 2. Schematic diagram of the proposed setup: red quantities are variables measured by the embedded controller.

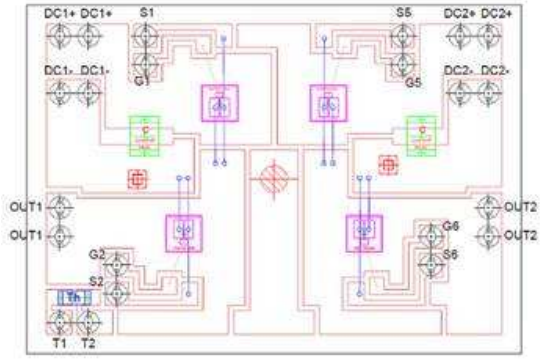

Fig. 3. Layout of the power module. In green the two internal capacitors. In blue the embedded NTC resistor (labelled "Th") measuring the DBC temperature (courtesy of Vishay Semiconductor Italiana).

Fig. 4. Power module package.

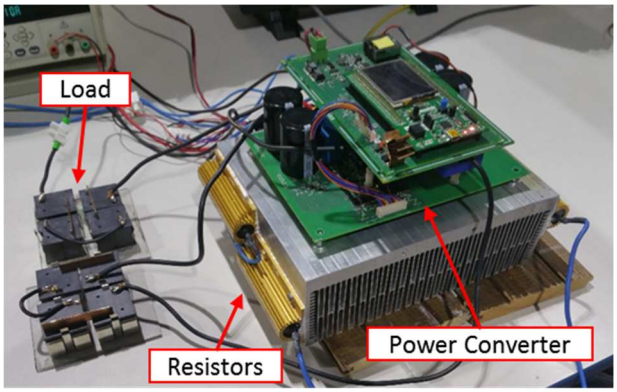

Fig. 5. Picture of the prototypal experimental setup.

III. Commissioning Test Procedure

A. R_{ON} and Junction Temperature Map

The device SW1L of the module (see Fig. 2) is preliminarily characterized. The R_{ON} versus junction temperature ϑ_J and drain current I_{DS} relationships are obtained by imposing to the switch a series of current pulses of short duration and measuring the direct voltage V_{ON} and DBC temperature. The DBC temperature. measured via the embedded NTC thermistor showed in Fig. 3, represents the junction temperature with negligible error, given the short duration of the current pulses. The same current pulses sequence is repeated for different values of the DBC (i.e. junction) temperature. The collected data populate a two-dimensional look-up-table, in the form ϑ_J as a function of I_{DS} and R_{ON}, then used for online temperature estimation, as depicted in Fig. 10. The commissioning process can be schematized as follows (details can be found in [13]):

1. The heatsink is heated until the NTC indicates 145°C, using the external resistors showed in Fig. 5. At 145°C the resistors are turned off.
2. Twenty-eight current pulses from 1 A to 28 A, 100 µs long, are imposed to the load (i.e. to the device). Pulses are separated by a wait time of 100 ms. Altogheter, one sequence takes circa 3 seconds. The 28 values of I_{DS} and V_{ON} are logged and associated to the junction temperature level 145°C.
3. The DBC temperature lowers naturally, helped by the ventilation of the cooling fans. Every time the NTC temperature measurement drops by 5°C, another set of current pulses is imposed and logged (e.g. at 145°C, 140°C, 135°C etc...).
4. The test stops when the heatsink reaches the room temperature (25°C) or when cooling becomes too slow. The total commissioning time for this prototype was 20 minutes.

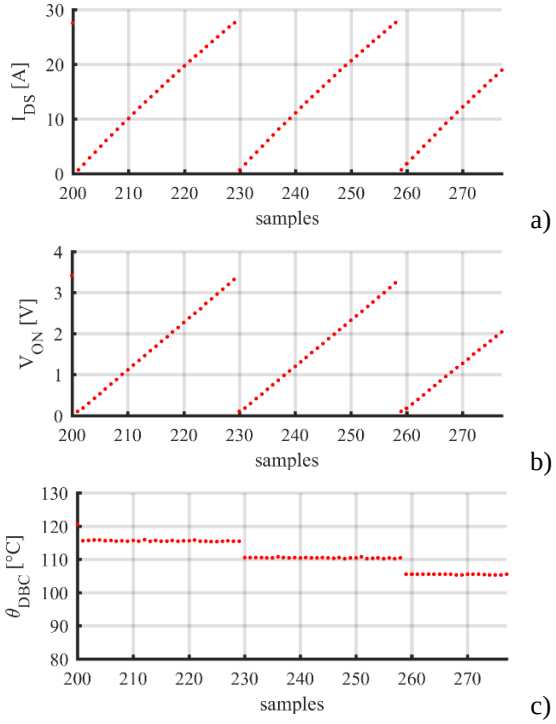

Fig. 6. Log of I_{DS} , V_{ON} and $\vartheta_{DBC} = \vartheta_{junction}$ during the initial mapping of the module.

B. R_{ON} versus DBC Temperature at Fixed Current

The main contribution of this paper consists in the additional commissioning part dedicated to aging prognostics. Respect to previous work, the identification of the R_{ON} versus DBC (not junction) temperature is included in the initial commissioning sequence. This is done at constant, steady-state current: this second R_{ON} curve is measured at a significant current level (15 A in the example), during each temperature step of the commissioning of the temperature lookup table. Upon completion of the 28 short time pulses routine, the continuous load current of 15 A is imposed for 10 seconds. After 10 seconds, the R_{ON} and DBC temperature values are logged and stored in a separate table representing R_{ON} ($I_{DS} = 15\text{A}$, ϑ_{DBC}) also called **15A reference curve**.

Fig. 7 shows the log of one test sequence started at DBC temperature of 35°C: the red samples are the data later used to populate the 2-D junction temperature map, whereas the blue dots are the last ten samples of the 10 s steady-state test at I_{DS} = 15 A, and related V_{ON} and temperature (sampling time is 100 µs). The blue samples are averaged to constitute one point of the steady-state R_{ON} curve, associated to the corresponding DBC temperature (DBC temperature is 37°C in the example, as the 10s, 15 A pulse heats the DBC by 2°C in this case).

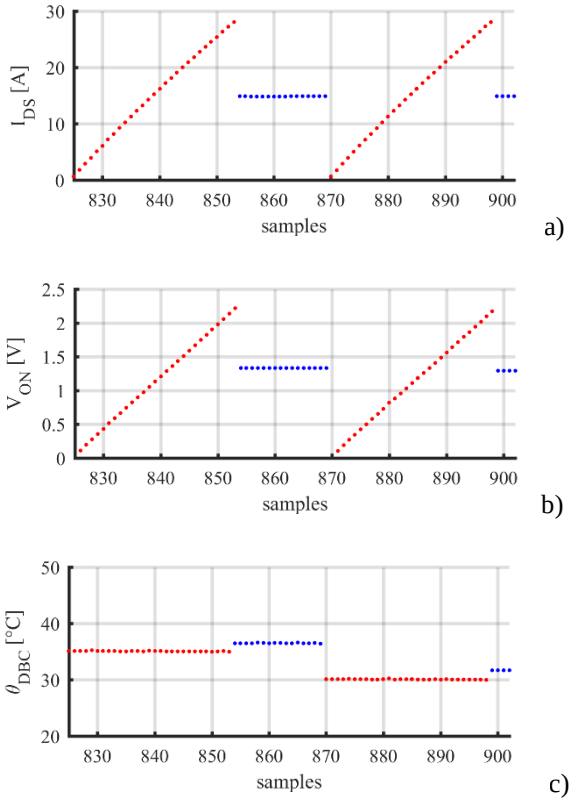

Fig. 7. Impulsive current test for mapping R_{ON} versus current and junction temperature (red dots) and R_{ON} versus DBC temperature at 15 A (blue).

C. Commissioning test results

The commissioning test can be summarized with the flowchart of Fig. 8. Respect to the procedure presented in [13], the 15A-commissioning is highlighted with a red dashed box in Fig. 8. During each of the 10 s, 15 A current tests, the junction temperature can become significantly higher respect to DBC temperature, in the order of 40°C more. If a higher current was used in place of 15 A the junction temperature

would be even higher. For this reason, the 15A-commisioning is limited to the temperature region $\vartheta_{DBC} \leq 85°C$, so to guarantee a suitable margin with respect to the maximum allowed junction temperature of 175°C. It is unnecessary to extend the DBC temperature range of this additional identification, as addressed later in the paper.

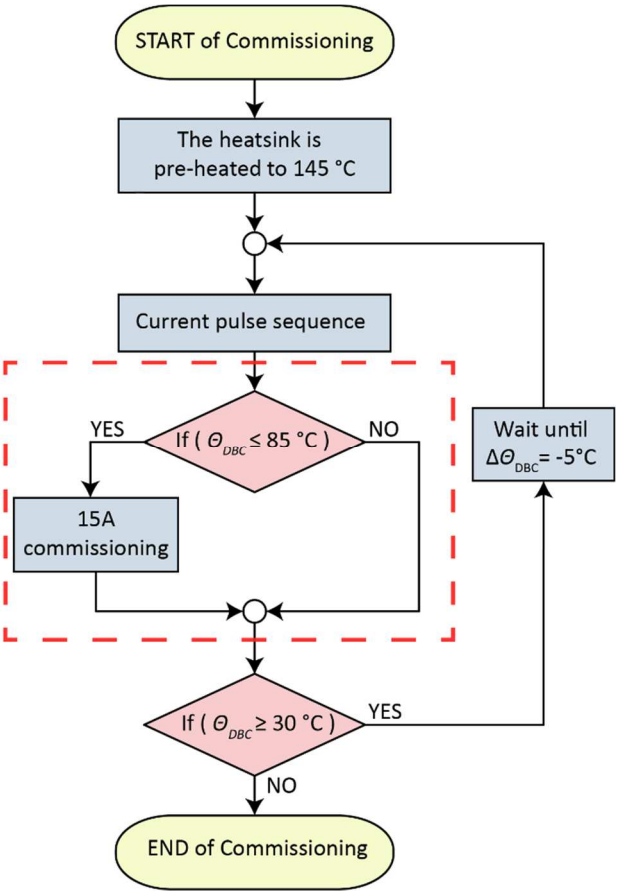

Fig. 8. Commissioning test flowchart.

After the commissioning of the power module, the obtained data are manipulated to build the junction temperature look-up-table $\vartheta_J\ (I_{DS},\ R_{ON})$ showed in Fig. 9. This is used to estimate the junction temperature while the converter is working with a PWM modulation, following the scheme showed in Fig. 10.

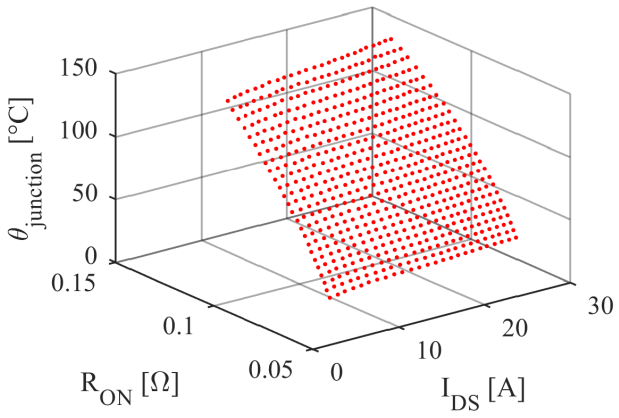

Fig. 9. Pulse current test results $\vartheta_J\ (I_{DS}, R_{ON})$.

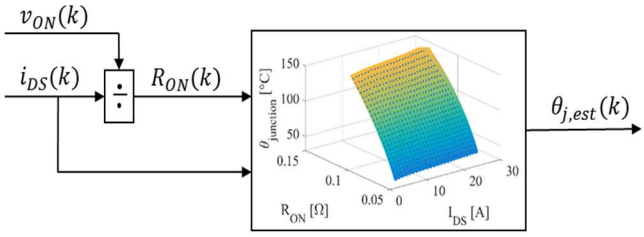

Fig. 10. Block diagram of the on-line temperature monitoring strategy.

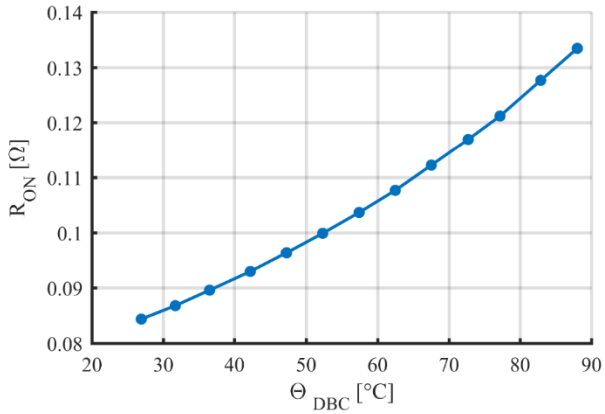

Fig. 11. 15A-test commisioning results $R_{ON}\ (I_{DS} = 15A,\ \vartheta_{DBC})$.

The resistance curve $R_{ON}\ (I_{DS} = 15\text{A},\ \vartheta_{DBC})$ showed in Fig. 11 is the additional result of the commissioning session. This will be used to estimate the aging of the component, in the idle time of the converter, as addressed in the following. As said, such **15A-commisioning** was performed in a limited DBC temperature range, between 25°C and 85°C, for it is unnecessary (and dangerous) to run this identification at higher temperatures.

IV. DEVICE PROGNOSTICS

A. *Accelerated Aging of the Power Module*

To validate the proposed methodology, the module under test needs to be subject to accelerated life tests. Among many possible techniques, **thermal cycling** was selected, as it is recognized as one of the most effective regarding package related failure progress [14]. **Passive thermal cycling** consists of imposing DBC temperature cycles through an external heat source, obtaining a very precise control of thermal swings. However, this method does not reproduce the same temperature gradient within the module typical of the converter's operating conditions. A second method known as **active power cycling** uses the converter's losses for self-heating the power switches. Although the thermal swings are not controllable as accurately as in the former case, active cycling allows to obtain a more realistic temperature distribution, like during operation. Active power cycling is used in this work.

B. *R_{ON} before and after 15.000 thermal cycles*

To perform active power cycling, the current of SW1L was controlled step-wise between 0 A and 21.5 A, with a period of 4 s and a duty-cycle of 50%.

After 15,000 of such cycles (17 hours circa), the module was characterized again, obtaining a new temperature map $\vartheta_J\ (I_{DS},\ R_{ON})$ and 15A curve $R_{ON}\ (I_{DS} = 15\text{A},\ \vartheta_{DBC})$. Having the new temperature map permits to evaluate the R_{ON} increase after 15,000 cycles. Fig. 12 shows the R_{ON} before and after thermal cycling as a function of junction temperature, at 15 A. The R_{ON} increase is circa constant, independently from the junction temperature, equal to 1.6 mΩ.

Fig. 13 compares the 15A-commissioning results before and after aging, i.e. the dependency of R_{ON} respect to DBC temperature at 15 A. The clearance between the red and blue curves in this case is amplified and not constant along the temperature axis. In turn, for the same DBC temperature the R_{ON} increase provokes a loss increase that reflects on the junction temperature, further increasing the resistance and loss.

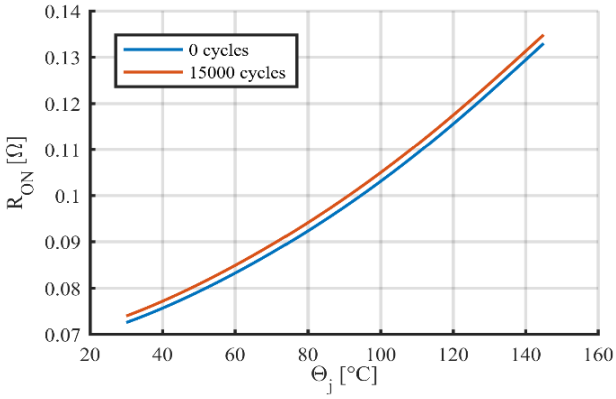

Fig. 12. : R_{ON} as a function of junction temperature at 15 A.

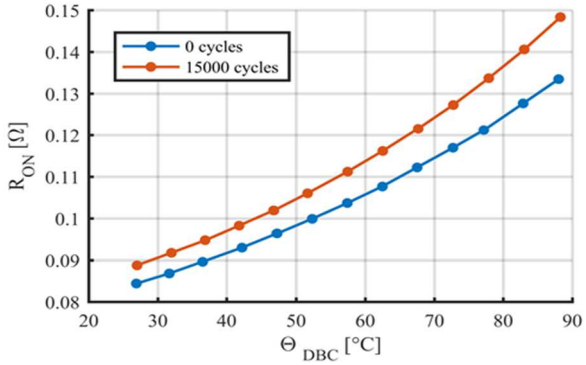

Fig. 13. 15A-test commisioning results $R_{ON}\ (I_{DS} = 15A,\ \vartheta_{DBC})$.

C. Effect of Aging on Temperature Monitoring

After aging, the online junction temperature monitoring becomes overestimated, if the initial R_{ON} map is still used for temperature estimation. Fig. 14 shows the junction temperature estimate of the aged component, during a test with a rectangular wave load current, using the initial temperature map and the one re-evaluated after 15,000 thermal cycles. The output of the "after 15,000 cycles LUT" (violet line) stands for the correct junction temperature, whereas the output of the initial look-up-table (0 cycles LUT, yellow line) overestimates the device temperature by 4.5°C to 6°C in the conditions of this example.

Although the R_{ON} increase due to aging and related temperature overestimate are modest, they allow the real-time temperature monitoring to be on the safe side of warning the supervisory control about possible risk of overheating. Moreover, the temperature estimation based on the initial commissioning will become more and more pessimistic as the aging of the devices proceeds.

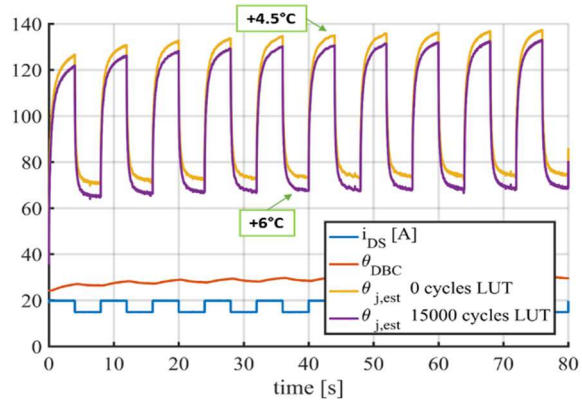

Fig. 14. Junction temperature estimation after 15,000 cycles aging.

D. Effect of Aging on Closed-Loop Temperature Limitation

In Fig. 15 the online junction temperature estimation is used for the close-loop limitation of the junction temperature. The maximum reference current of the converter is limited according to the estimated junction temperature. Using this closed-loop temperature limitation technique, the effect of aging will be to over limit the converter's current, leading this to progressively underperform. In this case, the user is being made aware that the power module show signs of aging, and can decide to run a new temperature commissioning test to re-establish the accurate temperature estimation.

In turn, although becoming progressively inaccurate, the online temperature monitoring is inherently a precursor of failure, either in open- or closed-loop (Fig. 14 and Fig. 15 respectively).

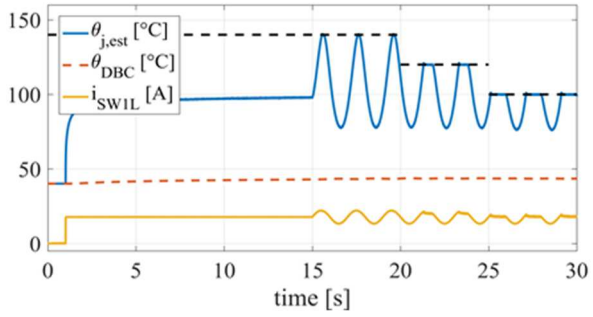

Fig. 15. Estimation and limitation of the junction temperature. The black dashed line represents the maximum allowable juntion temperature set by the user.

E. Quick Test for Evaluation of Aging

As said, the aging effect is more evident when comparing the R_{ON} versus DBC curves $R_{ON}\ (I_{DS} = 15\text{A},\ \vartheta_{DBC})$, already shown in Fig. 13 before and after aging. The former curve (in blue) comes from the initial commissioning of the module, and it is used here as the benchmark of initial life conditions. The proposed quick test to evaluate aging is called the "**15A-test**" after the "**15A-commissioning**" described before. During the idle time of the converter, the same current of 15 A

used for commissioning is imposed and the R_{ON} is sampled after 10 s, as showed in Fig. 16 (red cross in the bottom subplot). This quick test refers to a DBC temperature of around 58°C. The same red cross in Fig. 17 puts in evidence a +5 mΩ difference after 15,000 thermal cycles, with respect to the benchmark curve. Such +5 mΩ difference before and after aging is a very evident precursor of failure for the module. The quick 15A test can be performed any time between operation and operation, independently from the current DBC temperature.

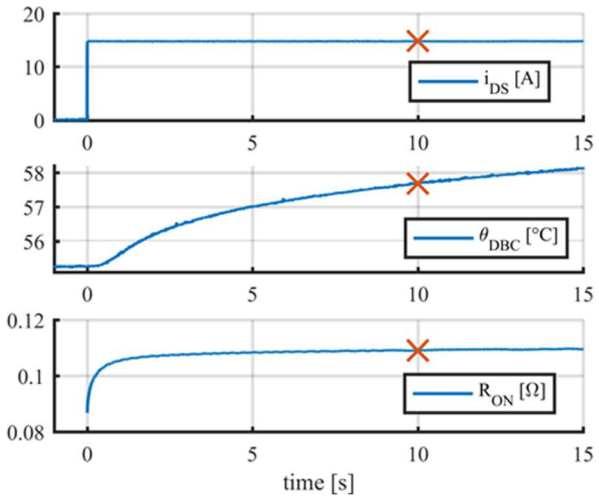

Fig. 16. 15A-test after 15,000 thermal cycles.

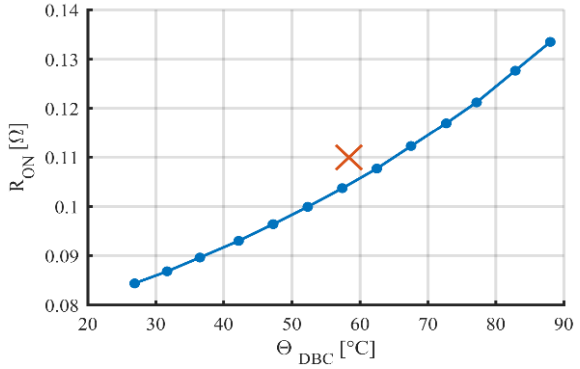

Fig. 17. : R_{ON} ($I_{DS} = 15A$, ϑ_{DBC}) after 0 thermal cycles vs current step test after 15,000 thermal cycles.

F. Discussion About the 15 A Commissioning and Test

Fig. 16 shows the evolution of ϑ_{DBC} during the 15A-test. The 10 s duration of the test was chosen to ensure that the first thermal transient between junction and DBC is extinguished. Two thermal time constants are noticeable: the initial thermal transient that has a time constant of circa 1 s, represents the junction to DBC thermal transient. After 5 s from the load current step, this first transient is extinguished and the junction to DBC temperature difference can be considered in steady-state. This explains why the R_{ON} is sampled after 10 s, both in the initial identification and in the quick assessment of aging during life.

The choice of the 15 A current amplitude is circa half way respect to the 28 A range used for identification of the junction temperature map. As a rule, this current should not be too low not to make the evaluation of R_{ON} too noisy and not too high not to damage the module during the identification.

The 15A-test should be performed regularly throughout the life of the component, in the idle time of the converter. The starting heatsink temperature is not relevant, since the benchmark curve of Fig. 11 is known in a large range of DBC temperatures.

The NTC thermistor embedded in the module provides a local measurement of the DBC temperature: in the module under test the NTC is placed in the left lower corner (Fig. 3). During the 15A-commissioning and 15A-test, the temperature gradient across the DBC is not negligible. To be able to use the benchmark table profitably as in Fig. 17, it is mandatory to recreate the same temperature gradient across the DBC, i.e. the same test conditions. Power losses between the four MOSFETs inside the power module, during the 15A-commissioning should be distributed likewise the losses in the 15A-test. For example, if during the 15A-commisioning it is necessary to command duty LEG1=0 and duty LEG2= 0.1 to impose 15A to the load, also during the 15A-test the two legs should work with analogous duty cycles.

The thermal connection with heatsink influences the temperature distribution across the DBC during the tests. For this reason, it is important to have the same thermal path during both tests. Upon noticing a significant mismatch between the 15A-test measurement and the benchmark value referred to healthy conditions, the user can either decide to stop the power converter for maintenance or to run a new R_{ON} mapping of the module, for updating the junction temperature map.

According to [12] where the same module has been tested, a substantial increase in the R_{ON} value is expected before the component fails, though not all failure mechanisms have the same impact on the increase of R_{ON}. For example, according to [14], wire bonds' damages will cause a relatively low increase of the resistance of the component, because they constitute only a small part of the total ON resistance. Nevertheless, the proposed technique covers all those failure mechanisms which impact on the increase of R_{ON}.

V. Conclusion

This paper demonstrates that inserting the V_{ON} measurement on board of a power converter permits a highly dynamic online estimation of the junction temperature and the assessment of the state of health of the power device. The presented methodology is applicable to commercial converters, provided that the V_{ON} measurement is embedded inside the gate drivers with little impact on the cost of the components. The current weakness of the proposed method is that the initial commissioning tests rely on the passive heating of the heatsink, and that the heatsink temperature is taken to high values, of the same order of the maximum junction temperature. Solutions using active heating and reduced heatsink temperature are currently under study and seem feasible, although requiring a deeper understanding of the physics of ON resistance variation. The ability to "measure" the health status of power semiconductors can justify the additional cost that the converter or module manufacturer might sustain for inserting the V_{ON} pick-up on board, especially in all the applications that are subjected to strict safety regulations. The possibility to monitor and on-line limit the maximum junction temperature, joint to a prognostic

capability can be of paramount importance for increasing the power converters reliability. The presented prognostic method need further development: so far, it can indicate that the health status of the device has changed, without giving a precis forecast of the residual lifetime. Further tests will be conducted to investigate the impact of different failure mechanisms have on the R_{ON}. It is also reasonable to suppose that each families of devices will present peculiar behaviours.

REFERENCES

[1] C. Neeb, L. Boettcher, M. Conrad and R. W. De Doncker, "Innovative and Reliable Power Modules: A Future Trend and Evolution of Technologies," in IEEE Industrial Electronics Magazine, vol. 8, no. 3, pp. 6-16, Sept. 2014.

[2] Wang, Huai, Marco Liserre, and Frede Blaabjerg. "Toward reliable power electronics: Challenges, design tools, and opportunities." IEEE Industrial Electronics Magazine 7.2 (2013): 17-26.

[3] E. Wolfgang, “Examples for failures in power electronics systems,”presented at ECPE Tutorial ‘Rel. Power Electron. Syst.’, Nuremberg, Germany, Apr. 2007.

[4] Y. Avenas, L. Dupont and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters-A Review," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3081-3092, June 2012.

[5] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," in IEEE Transactions on Power Electronics, vol. 25, no. 11, pp. 2734-2752, Nov. 2010.

[6] N. Baker, M. Liserre, L. Dupont and Y. Avenas, "Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods," in IEEE Industrial Electronics Magazine, vol. 8, no. 3, pp. 17-27, Sept. 2014.

[7] K. Ma, A. S. Bahman, S. Beczkowski and F. Blaabjerg, "Complete Loss and Thermal Model of Power Semiconductors Including Device Rating Information," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2556-2569, May 2015.

[8] L. A. Navarro et al., "Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap Semiconductor Devices and Harsh Environment Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2261-2271, May 2014.

[9] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," 2015 IEEE International Electric Machines & Drives Conference (IEMDC), Coeur d'Alene, ID, 2015.

[10] A. M. Aliyu and A. Castellazzi, "Prognostic System for Power Modules in Converter Systems Using Structure Function," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 595-605, Jan. 2018.

[11] [7] H. Chen, B. Ji, V. Pickert and W. Cao, "Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects," in IEEE Transactions on Device and Materials Reliability, vol. 14, no. 1, pp. 220-228, March 2014.

[12] H. Luo, F. Iannuzzo, F. Blaabjerg, M. Turnaturi and E. Mattiuzzo, "Aging precursors and degradation effects of SiC-MOSFET modules under highly accelerated power cycling conditions," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017, pp. 2506-2511.

[13] F. Stella, G. Pellegrino, E. Armando and D. Daprà, “Advanced Testing of SiC Power MOSFET Modules for Electric Motor Drives”, 2017 International Electric Machines and Drives Conference (IEMDC), Miami, 2017.

[14] C. Durand, M. Klingler, D. Coutellier and H. Naceur, "Power Cycling Reliability of Power Module: A Survey," in IEEE Transactions on Device and Materials Reliability, vol. 16, no. 1, pp. 80-97, March 2016.

[15] F. Stella, G. Pellegrino, E. Armando and D. Dapra, "On-line Junction Temperature Estimation of SiC Power MOSFETs through On-state Voltage Mapping," in IEEE Transactions on Industry Applications. doi: 10.1109/TIA.2018.2812710