A Zero-Timing Overhead SET Mitigation Approach for Flash-based FPGAs

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Sarah Azimi, Boyang Du, Luca Sterpone

Dipartimento di Automatica e Informatica
Politecnico di Torino
Torino, Italy

***Abstract*—Mitigation techniques for SET effects introduce severe timing penalties to the hardened circuit. In this paper, we develop a new SET mitigation approach not introducing timing degradation. Experimental results on Flash-based FPGAs demonstrate its effectiveness.**

***Key words*—Flash-based FPGAs, Transient effects, Multiple Event effects.**

I. Introduction

ADVANCED digital circuits play an important role in a growing number of applications. When used in mission critical application, digital circuits require a special attention to the dependability aspect. In fact, one of the most critical environment aspects that could lead to the failure of modern integrated technologies and systems is radiation. When a charged particle hits the target device, it may cause a voltage glitch, i.e. Single Event Transient (SET), in the circuit when can then propagate as a normal signal. During the propagation of SET, if it reaches a memory element, e.g. Flip Flop or Memory, depending on the arrive time and duration of the SET pulse, it may be sampled and corrupting the data stored inside.

Considering the reprogrammable devices such as Flash-based FPGAs, device technology scaling makes them more prone to be affected by a charged particle [1]. The increasing of clock frequency demanded by complex designs also increases the probability of SET be sampled, making situation even worse. Therefore, study, analysis and mitigation of SET phenomena have attracted a lot of attentions in recent years.

Several studies have been dedicated to the analysis of SET propagation. Most of those studies focus on electrical modeling where physical simulation allows to characterize and validate the propagation of SET pulse shape [2]. However, electrical modeling did not take into account the broadening/filtering effect of the SET pulse traversing logics and routing known as Pulse Induced Propagation Broadening (PIPB) [13]. In addition, these approaches are time consuming, which cannot be directly applied in an industrial design flow.

On the other hand, several mitigation solutions have been proposed in the past. Mitigation solutions based on filtering structure insertion have been proposed [3], which are effective against SET, but also introduce heavy performance and hardware resource overhead. There are mitigation solutions based on modification of physical layout or re-timing of the routing without modification of the placement of combinational gates or FFs. However, these solutions require the reconfiguration of the resources which means the modification of logic and routing segment, affecting the overall circuit performances.

This work presents a new design flow based on charge sharing gate insertion into the circuit netlist able to decrease the sensitivity of nodes w.r.t. the SET pulse propagation. The main contribution consists on the first approach able to implement SET on Flash-based FPGAs without any timing penalty. The effectiveness of the proposed algorithm has been evaluated on several benchmark circuits by means of SET fault injection using a Flash-based FPGA development board and an improvement of resiliency of 4 times with respect to state of the art solution can be observed. Furthermore, the experiments show that circuit mitigated with our approach do not have any timing degradation.

The paper is organized as follows: Section II provides an overview of the related works; Section III presents the proposed methodology for mitigation without timing penalty. Section IV presents the experimental results. Finally, conclusions and future works are discussed in Section V.

II. Related Works

Many works have been investigating SET effects in digital circuits. For the studies carried out with Flash-based FPGA as target device, since the Flash-based configuration cells are immune to bit-flips when struck by charged particles, SET in user logic and routing resources is the main focus. Characterizations of radiation induced SETs in different circuits in order to identify the type of SET generated within the silicon structure of Flash-based FPGA regarding various radiation sources have been carried out [6][7]. Further studies focusing on the SET influence on the logic and routing structure demonstrated the efficiency of the mitigation of SET based on electrical filtering [8]. There are also studies reporting radiation test experiments and electrical fault injections of SET propagation on custom circuits designed specifically to observe SETs [9]. In [14], authors proposed internal electrical injection approach to analyze the SET phenomena regarding propagation characteristics when traversing through logics and routing.

Meanwhile, several SET mitigation solutions have been proposed. One traditional method is redundancy based such as Triple Modular Redundancy (TMR) [10], along with some other techniques using time or spatial redundancy [11].

However, since methods based on replication fundamentally introduces significant resource and performance overhead, methods perform sensitivity analysis of the circuits and applied mitigation to the identified sensitive nodes and selectively mitigate them [12] have been proposed. However, timing overhead is still a critical issue for this kind of solutions.

III. Proposed Design Flow

To mitigate the SET induced by radiation particles striking silicon structure of Flash-based FPGA devices, the proposed design flow is illustrated in Fig. 1.

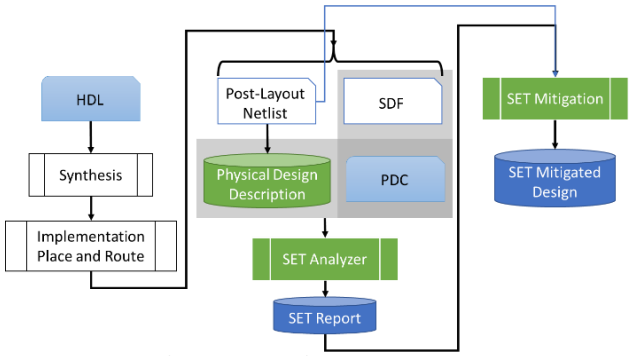

Figure 1. Overview of the developed flow including SET analysis and charge sharing mitigation.

The flow starts from the output files from commercial/standard FPGA design flow, which includes the Post-Layout Netlist, SDF and the Physical Design Constraints (PDC). First, the Post-Layout Netlist is converted to a format designed in-house named Physical Design Description (PDD) file which stores the circuit in a graph representation; then with the timing information extracted from the SDF and the placement information within the PDC, the SET Analyzer tool SETA [17] is executed, generating a SET report which contains the information regarding SET sensitivity for each Flip-Flop in the design, the worst case SET pulse width taking into account the PIPB effects and so on; finally, the zero-timing SET mitigation algorithm, illustrated in Fig. 2, is executed to generate the final SET mitigated design. Please note that the SET mitigation step can be carried out with extra user constraints declaring specifically to include or exclude certain part of the design for charge sharing structure insertion.

For nanometer Flash-based FPGAs, the decreasing size of device nodes results in higher probability of charge collection in multiple logic switches when a single particle strike the device. This phenomena results in different transient pulse shapes related to the LET absorbed by the switch junction. The key idea of the mitigation algorithm relies on insertion of extra charge sharing structures into the design so to reduce the possible SET pulse amplitude and width when it traverse the logic paths.

Since the insertion of charge sharing structures increases the fan-out of the selected nodes, the algorithm also controls the threshold for insertion to avoid introduce extra delay in the path, i.e. performance degradation. This has been done by exploiting the lower buffering threshold level provided in FPGA routing node: if the fan-out is below that threshold, the delay of the traversing signal is not affected. Instead, the added charge sharing structure will reduce the PIPB effect thus nullifying the SET effect before reaching a memory element (e.g., Latch, Flip-Flop or IO block).

```
//Initialization Phase
Netlist_orig = Verilog_load();
Netlist_sol = {0};
∀ Node n ∈ Netlist_orig -> PIPB [node] = SET_Report[n];
∀ Path p ∈ {FF_I, FF_o} -> RC_node(p) = {0};
//1. RC load computation
∀n ∈ P do
  for i ∈ output_nets(n)
    if i is not buffered
      N_NB(i) = Time_Unbuffered(n, Netlist_orig);
    else
      N_BU(i) = Time_Buffered(n, Netlist_orig);

  RC_node(n)= (∑ N_NB(i) + N_BU(i))/Fan_out(n);
//2. Charge Sharing Computation
∀ Node n ∈ Netlist_orig -> CS [node] = {0};
V_path[n] = {0};
for p ∈ P : CS[node] = V_path
  ∀ n ∈ P -> G(n) = interpolate(PIPB[n], RC_node[n]);
  PIPB_min = Max(PIPB(p));
  H_min = Max(RC_node(p));
  for i ∈ n generate binary permutation S
    H = card(G(n));
    PB = global_PIPB(p,S);
    If PB < original_PIPB(p) && H <= original_card(p)
       H_min = H; V_path = S;
//3. Modify Netlist
∀ Node n ∈ Netlist_orig
   Netlist_sol = add_CS_structure(V_path);
//4. Export Verilog netlist
Export_Verilog(Netlist_sol);
```

Figure 2. The Charge sharing mitigation algorithm for Flash-based FPGAs.

The mitigation algorithm starts with loading the Post-Layout Netlist and the SET report generated by the SETA tool. The mitigation is performed in three phases:

1. It computes the Resistive Capacitive (RC) load for each circuit node within the original netlist. The computation is done adding the timing of buffered or un-buffered nets connected to the output pins of a considered node. The coefficient of the RC load is obtained dividing the timing by the fan-out of each node.
2. It selects the suitable nodes for the logic charge sharing insertion. The selection is done by interpolating the PIPB values considering the original RC load and obtaining the expected size of charge sharing structure for each node in terms of number of gates. The selection of the node where to apply charge sharing gates is determined by combinational permutation identifying the solution that minimize the PIPB effect while limiting overall number of added gates per circuit logical path. In Fig. 3, it reports an example of interpolation data, where it is possible to notice that when charge sharing structure contains less than 40 gates it is possible to achieve a reduction of the PIPB coefficient, i.e. filtering of SET, without affecting the timing characteristics of the node.
3. It modifies the netlist adding charge-sharing structure of proper size to the selected logic nodes. Finally, the

algorithm exports the modified netlist and placement constraints file. The two files then can be imported in the commercial FPGA design flow to generate the final design implementation.

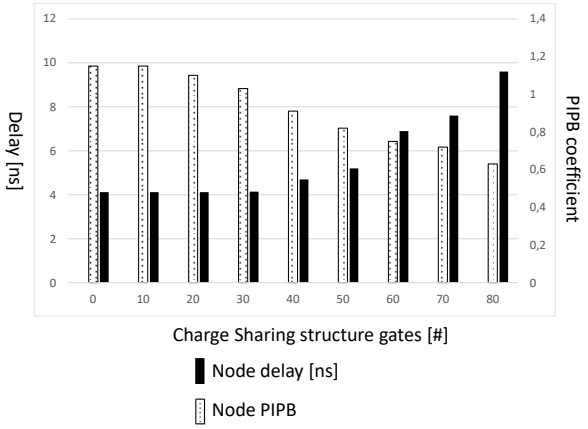

Figure 3. Charge sharing number of gates per logic nodes with respect to the routing delay and PIPB coefficient.

An example of the application of charge sharing mitigation algorithm is illustrated in Fig. 4. In details, considering the original netlist A where three SETs pulses having width of 0.3, 0.6 and 0.8 ns can broaden up to 0.38, 0.81 and 1.08 ns since PIPB coefficients of all gates are positive. Considering the application of the charge sharing structure at the netlist B, an electrical masking or reduction of all the SET pulses is noticeable.

IV. Experimental Results

The proposed design flow has been experimentally evaluated by means of SET static analysis and electrical injection platform [15] using an A3P250 Flash-based FPGA manufactured by Microsemi having 6,144 logic VersaTiles. We used the Libero SoC commercial design flow to generate the PDC, SDF and Post-Layout netlist in Verilog for evaluating the mitigation algorithm. Several circuits with different complexities have been selected: 4 circuits from the ITC'99 benchmark collection [4], a Cordic core and a RISC microprocessor [5]. The characteristics of the original circuits without any mitigation approach are reported in Table I indicating the number of VersaTiles configured as Logic function or Flip-Flop and the maximal working frequency.

We analyzed the circuits SET sensitivity using the SETA tool, for the purpose of our experiments, considering three types of SETs (0.3, 0.6 and 0.8 ns). Please note that SET width lower than 1 ns corresponds to the most probable events generated by heavy ion strike on the Flash-based FPGA 130 nm technology [11]. The analysis results are reported in Table II indicating the number of FF in following categories:

1. *logical masked*: no SET in the input cone could reach the FF due to logic mask;
2. *filtered*: no SET in the input cone are totally filtered;
3. *partially filtered*: SET in input cone could reach the FF but with a reduced width;
4. *broadened*: SET in the input cone could reach the FF with a broadened width.

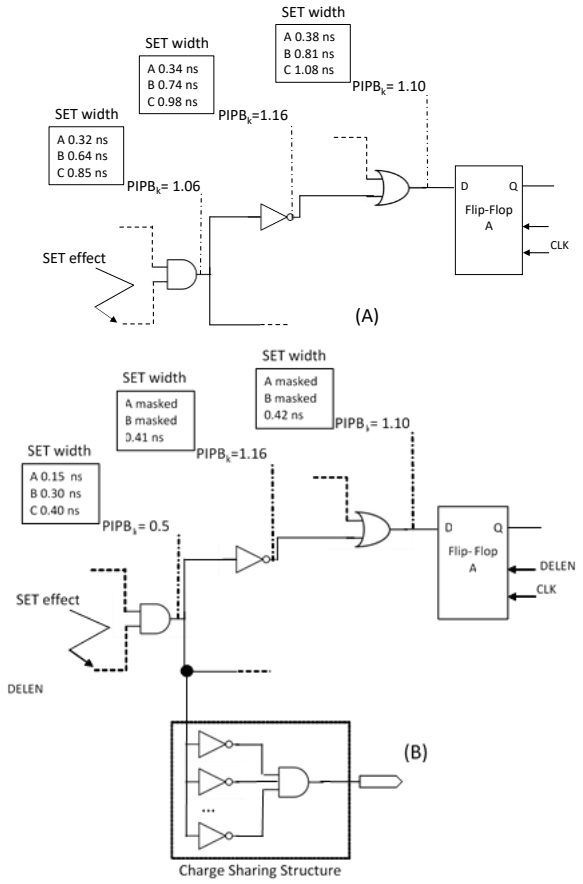

Figure 4. The key concept of the Charge Sharing mitigation algorithm.

TABLE I
CHARACTERISTICS OF THE ORIGINAL BENCHMARK CIRCUITS

Circuits	Versatile [#]	FFs [#]	Frequency [MHz]
B05	415	66	47
B09	493	67	46
B12	565	123	48
B13	162	50	52
CORDIC	956	240	45
RISC	1,401	1,156	42

TABLE II
COMPREHENSIVE FF SET SENSITIVITY USING THE STATIC ANALYSIS TOOL

Circuit	SET width lower than 1 ns			
	Logical Masked [#]	Filtered [#]	Partially Filtered [#]	Broadened [#]
B05	46	9	3	8
B09	47	3	6	11
B12	102	1	7	13
B13	21	14	8	7
CORDIC	161	12	28	39
RISC	572	204	184	196

Furthermore, two versions of circuits with SET mitigation solutions have been generated: 1) place and route and guard-gate techniques proposed in [16] using a maximal guard-gate filtering of 1ns, noted as P&R-GG; 2) proposed method, without excluding FFs in the design during SET mitigation. Please note that for both versions, Synopsys Synplify TMR has

been applied exclusively on the FFs as in real design, mitigation solutions for SEU would be usually adopted even SET is the main target in this work.

We used the electrical pulse injection platform to inject in random sensitive nodes of the circuits. We injected 5,000 SETs lower than 1 ns for each circuit and report the results in Table III where we show the percentage of *wrong answers*, when the circuit produces at least one output data different from the expected one. It is possible to observe that by applying our method, the percentage of wrong answers decrease drastically, with an noticeable improvement comparing the results achieved with the solution [16].

TABLE III
SET FAULT INJECTION WRONG ANSWERS COMPARISON

Circuit	Wrong Answers [%]		
	Plain	P&R-GG	Proposed Method
B05	68.5	12.2	4.3
B09	72.6	8.4	2.6
B12	83.2	9.4	3.1
B13	54.8	16.5	4.1
CORDIC	89.4	19.6	4.3
RISC	94.6	21.6	4.8

In Table IV, it reports the timing and area overhead, in terms of max frequency degradation percentage and number of VersaTiles respectively, of the two SET mitigation solutions against original version. As can be observed, there is no timing overhead while the area overhead is slightly less than the P&R-GG method.

TABLE IV
TIMING AND AREA OVERHEAD FOR EACH METHOD

Circuit		B05	B09	B12	B13	CORDIC	RISC
Timing [%]	P&R-GG	12	13	15	16	19	18
	Proposed Method	0	0	0	0	0	0
Area [#]	P&R-GG	27	28	28	27	32	31
	Proposed Method	25	27	25	24	28	27

V. CONCLUSIONS AND FUTURE WORKS

In this paper, we present a mitigation approach for SET affecting Flash-based FPGAs, which is capable to drastically reduce the sensitivity against SET without affecting the timing of the implemented circuit and lower area overhead comparing to previously proposed method. The developed solution has been validated with electrical fault injection of SET pulses typical for device under heavy ion strikes.

As future research, we plan to evaluate the power consumption overhead and more resources are introduced into the circuit increasing dynamic power consumption; secondly, we plan to perform radiation test analysis and to address the recent fourth generation of Flash-based FPGAs.

VI. ACKNOWLEDGMENTS

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